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1982 CATALOG

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Printed in the United States of America

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Microcomputer Division

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NEC Electronics U.S.A. Inc.

Microcomputer Division

GENERAL INFORMATION 2

MEMORY SELECTION GUIDE

DEVICE	SIZE	PROCESS	ACCESS TIME	CYCLE	SUPPLY VOLTAGE	PACKAGE	
						MATERIAL	PINS
DYNAMIC RANDOM ACCESS MEMORIES							
μPD416	16K x 1 TS	NMOS	120 ns	320 ns	+12, +5, −5	C/D	16
μPD4164	64K x 1 TS	NMOS	120 ns	270 ns	+5	C/D	16
STATIC RANDOM ACCESS MEMORIES							
μPD5101L	256 x 4 TS	CMOS	450 ns	450 ns	+5	C	22
μPD444	1K x 4 TS	CMOS	200 ns	200 ns	+5	C/D	18
μPD446	2K x 8 TS	CMOS	150 ns	150 ns	+5	C/D	24
μPD449	2K x 8 TS	CMOS	150 ns	150 ns	+5	C/D	24
μPD4016	2K x 8 TS	NMOS	150 ns	150 ns	+5	C/D	24
μPD4104	4K x 1 TS	NMOS	200 ns	310 ns	+5	C	18
μPD2114L	1K x 4 TS	NMOS	150 ns	150 ns	+5	C	18
μPD2147	4K x 1 TS	NMOS	25 ns	25 ns	+5	D	18
μPD2149	1K x 4 TS	NMOS	35 ns	35 ns	+5	D	18
μPD2167	16K x 1 TS	NMOS	55 ns	55 ns	+5	D	20
FIELD PROGRAMMABLE READ ONLY MEMORIES							
(Bipolar)							
μPB406	1K x 4 OC	BIPOLAR	50 ns	50 ns	+5	C/D	18
μPB426	1K x 4 TS	BIPOLAR	50 ns	50 ns	+5	C/D	18
μPB409	2K x 8 OC	BIPOLAR	50 ns	50 ns	+5	C/D	24
μPB429	2K x 8 TS	BIPOLAR	50 ns	50 ns	+5	C/D	24
(Bipolar Logic Array)							
μPB450	9216 bit	BIPOLAR	200 ns	200 ns	+5	D	48
(U.V. Erasable)							
μPD2716	2K x 8 TS	NMOS	450 ns	450 ns	+5	D	24
μPD2732	4K x 8 TS	NMOS	450 ns	450 ns	+5	D	24
μPD2732A	4K x 8 TS	NMOS	250 ns	250 ns	+5	D	24
μPD2764	8K x 8 TS	NMOS	250 ns	250 ns	+5	D	28
MASK PROGRAMMED READ ONLY MEMORIES							
μPD2316E/ EA8316E	2K x 8 TS	NMOS	450 ns	450 ns	+5	C	24
μPD2316E/ EA8316E-1	2K x 8 TS	NMOS	350 ns	350 ns	+5	C	24
μPD2332A/B/ EA8332A/B	4K x 8 TS	NMOS	450 ns	450 ns	+5	C	24
μPD2332A/B-1/ EA8332A/B-1	4K x 8 TS	NMOS	350 ns	350 ns	+5	C	24
μPD2364/ EA8264	8K x 8 TS	NMOS	450 ns	450 ns	+5	C	24
μPD23128/ EA8364	16K x 8 TS	NMOS	250 ns	350 ns	+5	C	28

Notes: OC = Open Collector; C = Plastic Package; D = Hermetic Package; TS = 3-State

MICROCOMPUTER SELECTION GUIDE

SINGLE CHIP 4-BIT MICROCOMPUTERS

DEVICE	FAMILY	ROM	RAM	I/O	PROCESS	OUTPUT	FEATURES	SUPPLY VOLTAGE	PINS
μPD546	μCOM-43	2000 x 8	96 x 4	35	PMOS	O.D.		−10	42
μPD553	μCOM-43H	2000 x 8	96 x 4	35	PMOS	O.D.	A	−10	42
μPD557L	μCOM-43SL	2000 x 8	96 x 4	21	PMOS	O.D.	A	−8	28
μPD650	μCOM-43C	2000 x 8	96 x 4	35	CMOS	push-pull		+5	42
μPD547	μCOM-44	1000 x 8	64 x 4	35	PMOS	O.D.		−10	42
μPD547L	μCOM-44L	1000 x 8	64 x 4	35	PMOS	O.D.		−8	42
μPD552	μCOM-44H	1000 x 8	64 x 4	35	PMOS	O.D.	A	−10	42
μPD651	μCOM-44C	1000 x 8	64 x 4	35	CMOS	push-pull		+5	42/52
μPD550	μCOM-45	640 x 8	32 x 4	21	PMOS	O.D.	A	−10	28
μPD550L	μCOM-45L	640 x 8	32 x 4	21	PMOS	O.D.	A	−8	28
μPD554	μCOM-45	1000 x 8	32 x 4	21	PMOS	O.D.	A	−10	28
μPD554L	μCOM-45L	1000 x 8	32 x 4	21	PMOS	O.D.	A	−8	28
μPD652	μCOM-45C	1000 x 8	32 x 4	21	CMOS	push-pull		+5	28
μPD556	μCOM-43	External	96 x 4	35	PMOS	O.D.	B	−10	64
MC-430P	μCOM-43	2000 x 8 UV EPROM	96 x 4	35	PMOS	O.D.	G	−10	42
μPD7500	μPD7500 Series	External	256 x 4	46	CMOS	O.D.	C	+2.7 to 5.5	64
μPD7501	μPD7500 Series	1024 x 8	96 x 4	24	CMOS	O.D.	D	+2.7 to 5.5	64
μPD7502	μPD7500 Series	2048 x 8	128 x 4	23	CMOS	O.D.	D	+2.7 to 5.5	64
μPD7503	μPD7500 Series	4096 x 8	224 x 4	23	CMOS	O.D.	D	+2.7 to 5.5	64
μPD7506	μPD7500 Series	1024 x 8	64 x 4	22	CMOS	O.D.		+2.7 to 5.5	28
μPD7507	μPD7500 Series	2048 x 8	128 x 4	32	CMOS	O.D.		+2.7 to 5.5	40/52
μPD7508	μPD7500 Series	4096 x 8	224 x 4	32	CMOS	O.D.		+2.7 to 5.5	40/52
μPD7508A	μPD7500 Series	4096 x 8	208 x 4	32	CMOS	O.D.	A	+2.7 to 5.5	40
μPD7519	μPD7500 Series	4096 x 8	256 x 4	28	CMOS	O.D.	F	+2.7 to 5.5	64
μPD7520	μPD7500 Series	768 x 8	48 x 4	24	PMOS	O.D.	E	−6 to −10	28

Notes: A = −35V VF Display Drive
B = μCOM-4 Evaluation Chip
C = μPD750X Evaluation Chip
D = LCD Controller/Driver
E = LED Display Controller/Driver
F = VF Display Controller/Driver
G = Pin-Compatible with μPD546
O.D. = Open Drain

MICROCOMPUTER SELECTION GUIDE

SINGLE CHIP 8-BIT MICROPROCESSORS

DEVICE	SPECIAL FEATURES	ROM	RAM	I/O	PROCESS	OUTPUT	CYCLE	SUPPLY VOLTAGE	PINS
μPD8021	Zero-Cross Detector	1024 x 8	64 x 8	21	NMOS	BD	3.6 MHz	+5	28
μPD8022	On-Chip A/D Converter	2048 x 8	64 x 8	26	NMOS	BD	3.6 MHz	+5	40
μPD8035L	μPD8048 w/External Memory	External	64 x 8	27	NMOS	TS,BD	6 MHz	+5	40
μPD8039L	μPD8049 w/External Memory	External	128 x 8	27	NMOS	TS,BD	11 MHz	+5	40
μPD8041	Peripheral Interface w/Slave Bus	1024 x 8	64 x 8	18	NMOS	TS,BD	6 MHz	+5	40
μPD8041A	Enhanced μPD8041	1024 x 8	64 x 8	18	NMOS	TS,BD	6 MHz	+5	40
μPD8048	Expansion Bus	1024 x 8	64 x 8	27	NMOS	TS,BD	6 MHz	+5	40
μPD8049	High Speed μPD8048	2048 x 8	128 x 8	27	NMOS	TS,BD	11 MHz	+5	40
μPD8741A	UV-EPROM μPD8041A	1024 x 8	64 x 8	18	NMOS	TS,BD	6 MHz	+5	40
μPD8748	UV-EPROM μPD8048	1024 x 8	64 x 8	27	NMOS	TS,BD	6 MHz	+5	40
μPD80C35	CMOS 8035	External	64 x 8	27	CMOS	TS,BD	6 MHz	+2.7 to 5.5	40
μPD80C48	CMOS 8048	1024 x 8	64 x 8	27	CMOS	TS,BD	6 MHz	+2.7 to 5.5	40
μPD80C39	CMOS 8039	External	128 x 8	27	CMOS	TS,BD	6 MHz	+2.7 to 5.5	40
μPD80C49	CMOS 8049	2048 x 8	128 x 8	27	CMOS	TS,BD	6 MHz	+2.7 to 5.5	40
μPD7800	Development Chip	External	128 x 8	48	NMOS	TS,BD	4 MHz	+5	64
μPD7801	8080 Expansion Bus 64K Memory Address Space	4096 x 8	128 x 8	48	NMOS	TS,BD	4 MHz	+5	64
μPD7802	Expanded μPD7801	6144 x 8	64 x 8	48	NMOS	TS,BD	4 MHz	+5	64
μPD78C05	CMOS Microprocessor	External	128 x 8	46	CMOS	TS,BD	4 MHz	+5	64
μPD78C06	CMOS Microcomputer	4096 x 8	128 x 8	46	CMOS	TS,BD	4 MHz	+5	64
μPD7810	Powerful Microprocessor	External	256 x 8	44	NMOS	TS,BD	10 MHz	+5	64
μPD7811	8 Channel A/D	4096 x 8	128 x 8	44	NMOS	TS,BD	10 MHz	+5	64

MICROPROCESSORS

DEVICE	PRODUCT	SIZE	PROCESS	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD780	Microprocessor	8-bit	NMOS	3-State	4.0 MHz	+5	40
μPD8080AF	Microprocessor	8-bit	NMOS	3-State	2.0 MHz	+12 ± 5	40
μPD8080AF-2	Microprocessor	8-bit	NMOS	3-State	2.5 MHz	+12 ± 5	40
μPD8080AF-1	Microprocessor	8-bit	NMOS	3-State	3.0 MHz	+12 ± 5	40
μPD8085A	Microprocessor	8-bit	NMOS	3-State	3.0 MHz	+5	40
μPD8085A-2	Microprocessor	8-bit	NMOS	3-State	5.0 MHz	+5	40
μPD8086	Microprocessor	16-bit	NMOS	3-State	5.0 MHz	+5	40

MICROCOMPUTER SELECTION GUIDE

SYSTEM SUPPORT

DEVICE	PRODUCT	SIZE	PROCESS	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD765AC	Double Sided/Double Density Floppy Disk Controller	8-bit	NMOS	3-State	8 MHz	+5	40
μPD781	Dot Matrix Printer Controller-Epson 500 Printer	8-bit	NMOS	3-State	6 MHz	+5	40
μPD782	Dot Matrix Printer Controller-Epson 200 Printer	8-bit	NMOS	3-State	6 MHz	+5	40
μPD7001	8-Bit A/D Converter	8-bit	CMOS	Open Collector Serial	10 kHz Conversion Time	+5	16
μPD7002	10-Bit A/D Converter	8-bit	CMOS	3-State	400 Hz Conversion Time	+5	28
μPD7201	Multi-Protocol Serial Controller	8-bit	NMOS	3-State	4 MHz	+5	40
μPD7210	IEEE Controller (Talker, Listener, Controller)	8-bit	NMOS	3-State	8 MHz	+5	40
μPD7220	Color Graphic Display Controller	8-bit	NMOS	3-State	5 MHz	+5	40
μPD7225	Alpha Numeric LCD Controller/Driver	8-bit	CMOS	–	–	2.7 to 5.5	52
μPD7227	Dot Matrix LCD Controller/Driver	8-bit	CMOS	–	–	2.7 to 5.5	64
μPD7720	Signal Processor	16-bit	NMOS	3-State	8 MHz	+5	28
μPD8155	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPD8155-2	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPD8156	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPD8156-2	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPB8212	I/O Port	8-bit	Bipolar	3-State	–	+5	24
μPB8214	Priority Interrupt Controller	3-bit	Bipolar	Open Collector	3 MHz	+5	24
μPB8216	Bus Driver Non-Inverting	4-bit	Bipolar	3-State	–	+5	16
μPB8224	Clock Generator Driver	2 phase	Bipolar	High Level Clock	3 MHz	+12 ± 5	16
μPB8226	Bus Driver Inverting	4-bit	Bipolar	3-State	–	+5	16
μPB8228	System Controller	8-bit	Bipolar	3-State	–	+5	28
μPD8243	I/O Expander	4 x 4 bits	NMOS	3-State	–	+5	24
μPD8251	Programmable Communications Interface (Async/Sync)	8-bit	NMOS	3-State	A-9.6K baud S-56K baud	+5	28
μPD8251A	Programmable Communications Interface (Async/Sync)	8-bit	NMOS	3-State	A-9.6K baud S-64K baud	+5	28
μPD8253-5	Programmable Timer	8-bit	NMOS	3-State	4.0 MHz	+5	24
μPD8255A-5	Peripheral Interface	8-bit	NMOS	3-State	–	+5	40
μPD8257-5	Programmable DMA Controller	8-bit	NMOS	3-State	4 MHz	+5	40
μPD8279-5	Programmable Keyboard/ Display Interface	8-bit	NMOS	3-State	–	+5	40
μPB8282/ 8283	8-Bit Latches		Bipolar	3-State	5 MHz	+5	20
μPB8284	Clock Driver		Bipolar	3-State	5 MHz	+5	18
μPB8286/ 8287	8-Bit Bus Transceivers		Bipolar	3-State	5 MHz	+5	20
μPB8288	Bus Controller		Bipolar	3-State	5 MHz	+5	20
μPD8355	2048 x 8 ROM with I/O Ports	8-bit	NMOS	3-State	–	+5	40
μPD8755A	2048 x 8 EPROM with I/O Ports	8-bit	NMOS	3-State	–	+5	40

MICROCOMPUTER ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
AMD	AM8080A/9080A	Microprocessor (2.0 MHz)	μPD8080AF
	AM8080A-2/9080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	AM8080A-1/9080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	AM8085A	Microprocessor (3.0 MHz)	μPD8085A
	AM8155	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155
	AM8156	Programmable Peripheral Interface with 256 x 8 RAM	μPD8156
	AM8212	I/O Port (8-Bit)	μPB8212
	AM8214	Priority Interrupt Controller	μPB8214
	AM8216	Bus Driver, Inverting	μPB8216
	AM8224	Clock Generator/Driver	μPB8224
	AM8226	Bus Driver, Non-Inverting	μPB8226
	AM8228	System Controller	μPB8228
	AM8251	Programmable Communications Interface	μPD8251
	AM8255	Programmable Peripheral Interface	μPD8255
	AM8257	Programmable DMA Controller	μPD8257
	AM8355	Programmable Peripheral Interface with 2048 x 8 ROM	μPD8355
	AM8048	Single Chip Microcomputer	μPD8048
INTEL	8080A	Microprocessor (2.0 MHz)	μPD8080AF
	8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	8021	Microcomputer with ROM	μPD8021
	8022	Microcomputer with A/D Converter	μPD8022
	8035L	Microprocessor	μPD8035L
	8039L	Microprocessor	μPD8039L
	8041A	Programmable Peripheral Controller with ROM	μPD8041A
	8048	Microcomputer with ROM	μPD8048
	8049	Microcomputer with ROM	μPD8049
	8085A	Microprocessor (3.0 MHz)	μPD8085A
	8085A-2	Microprocessor (5.0 MHz)	μPD8085A-2
	8086	Microprocessor (16-Bit)	μPD8086
	8155/8155-2	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155/8155-2
	8156/8156-2	Programmable Peripheral Interface with 256 x 8 RAM	μPD8156/8156-2
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8224	Clock Generator/Driver	μPB8224
	8226	Bus Driver, Inverting	μPB8226
	8228	System Controller	μPB8228
	8243	I/O Expander	μPD8243
	8251	Programmable Communications Interface (Async/Sync)	μPD8251

MICROCOMPUTER ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
INTEL (CONT.)	8251A	Programmable Communications Interface (Async/Sync)	μPD8251A
	8253-5	Programmable Timer	μPD8253-5
	8255A-5	Programmable Peripheral Interface	μPD8255A-5
	8257-5	Programmable DMA Controller	μPD8257-5
	8259A	Programmable Interrupt Controller	μPD8259A
	8272	Double Sided/Double Density Floppy Disk Controller	μPD765
	8279-5	Programmable Keyboard/Display Interface	μPD8279-5
	8282/8283	8-Bit Latches	μPB8282/8283
	8284	Clock Driver	μPB8284
	8286/8287	8-Bit Transceivers	μPB8286/8287
	8288	Bus Controller	μPB8288
	8355	Programmable Peripheral Interface with 2048 x 8 ROM	μPD8355
	8741A	Programmable Peripheral Controller with EPROM	μPD8741A
	8748	Microcomputer with EPROM	μPD8748
	8755A	Programmable Peripheral Interface with 2K x 8 EPROM	μPD8755A
	8274	Multiprotocol Serial Controller	μPD7201
NATIONAL	INS8048	Microcomputer with ROM	μPD8048
	INS8049	Microcomputer with ROM	μPD8049
	INS8080A	Microprocessor (2.0 MHz)	μPD8080AF
	INS8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	INS8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8224	Clock Generator/Driver	μPB8224
	8226	Bus Driver, Inverting	μPB8226
	8228	System Controller	μPB8228
	INS8251	Programmable Communications Interface	μPD8251A
	INS8253	Programmable Timer	μPD8253-5
	INS8255	Programmable Peripheral Interface	μPD8255A-5
	INS8257	Programmable DMA Controller	μPD8257-5
	INS8259	Programmable Interrupt Controller	μPD8259A
T.I.	TMS8080A	Microprocessor (2.0 MHz)	μPD8080AF
	TMS8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	TMS8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	SN74S412	I/O Port (8-Bit)	μPB8212
	SN74LS424	Clock Generator/Driver	μPB8224
	SN74S428	System Controller	μPB8228

ROM-BASED PRODUCTS ORDERING PROCEDURE

The following NEC products fall under the guidelines set by the ROM-Based Products Ordering Procedure:

μPD7801	μPD80C49	μPD554	μPD7506
μPD7802	μPD8355	μPD554L	μPD7507
μPD7811	μPD546	μPD557L	μPD7507S
μPD8021	μPD547	μPD650	μPD7508
μPD8022	μPD547L	μPD651	μPD7508A
μPD8041A	μPD550	μPD652	μPD7519
μPD8048	μPD550L	μPD7501	μPD7520
μPD80C48	μPD552	μPD7502	μPD7720
μPD8049	μPD553	μPD7503	

NEC Electronics U.S.A., Inc., Microcomputer Division is able to accept mask patterns in a variety of formats to facilitate the transferral of ROM mask information. These are intended to suit various customer needs and minimize the turnaround time. Always enclose a listing of the code and the code submittal form. The following is a list of valid media for code transferral.

- PROM/EPROM equivalent to ROM parts
- Sample ROMs or ROM-based microcomputers
- Paper Tape
- Timesharing Files
- ISIS-II compatible disks
- Other (Contact NEC Electronics U.S.A., Inc., Microcomputer Division for arrangements.)

Thoroughly tested verification procedures protect against unnecessary delays or costly mistakes. NEC Electronics U.S.A., Inc., Microcomputer Division will return the ROM mask patterns to the customer in the most convenient format. Unprogrammed EPROMs, if sent with the ROM code, can be programmed and returned for verification.

Earth satellites and the world-wide GE Mark III timesharing systems provide reliable and instant communication of ROM patterns to the factory. Customers with access to GE-TSS may further reduce the turnaround time by transferring files directly to NEC Electronics U.S.A., Inc., Microcomputer Division.

The following is an example of a ROM mask transferral procedure. The μPD8048 is used here; however, the process is the same for the other ROM-based products.

1. The customer contacts NEC Electronics U.S.A., Inc., Microcomputer Division's Sales Representative, concerning a ROM pattern for the μPD8048 that he would like to send.

2. Since an EPROM version of that part is available, the μPD8748 is proposed as a code transferral medium, or a paper tape and listing may be used.

3. Two programmed μPD8748's are sent to NEC Electronics U.S.A., Inc., Microcomputer Division with a listing, a code submittal form, and a paper tape as back-up.

4. NEC Electronics U.S.A., Inc., Microcomputer Division compares the media provided and enters the code into GS-TSS. The GE-TSS file is accessed at the NEC factory and a copy of the code is returned to NEC Electronics U.S.A., Inc., Microcomputer Division for verification. One of the μPD8748's is erased and reprogrammed with the customer's code as the NEC factory has it. Both μPD8748's and a listing are returned to the customer for his final verification.

5. Once the customer notifies NEC Electronics U.S.A., Inc., Microcomputer Division in writing that the code is verified and provides the mask charge and hard copy of the purchase order, work begins immediately on developing his μPD8048's.

Please contact your local Sales Representative for assistance with all ROM-based product orders, Mask Programmed ROM products other than those listed above are marketed by Electronic Arrays Division; refer to Section 5 for Electronic Arrays' ordering procedures.

NOTES

NEC

NEC Electronics U.S.A. Inc.

Microcomputer Division

MEMORIES

RANDOM ACCESS MEMORIES

3

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

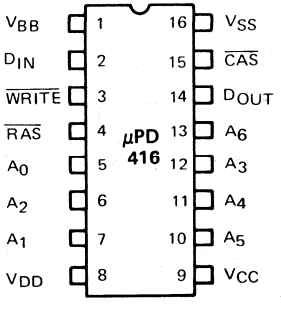
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, −5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 20 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 5 Performance Ranges:

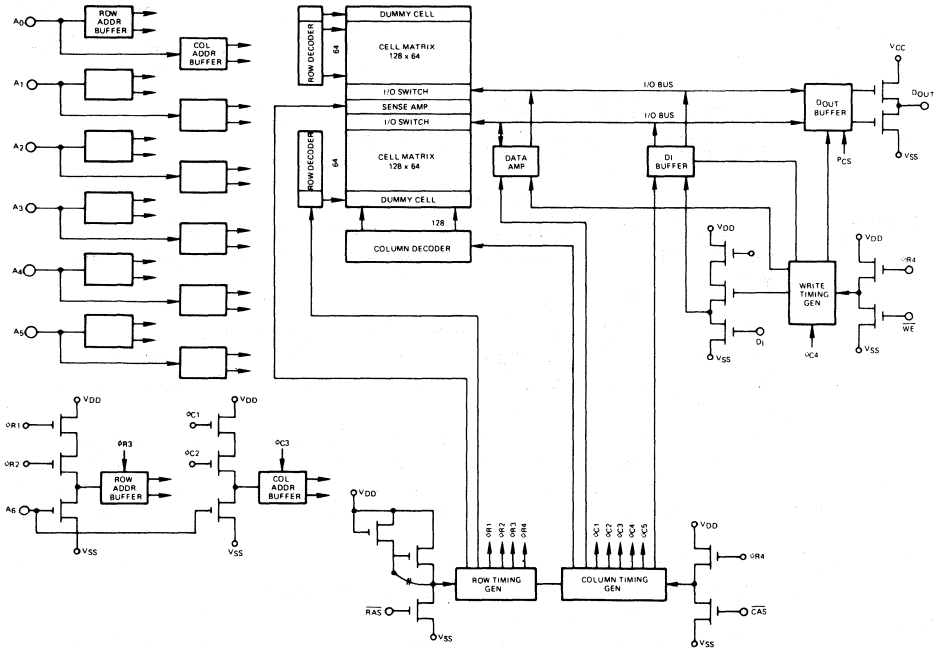
	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	575 ns
μPD416-1	250 ns	410 ns	465 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	320 ns	320 ns
μPD416-5	120 ns	320 ns	320 ns

PIN CONFIGURATION



A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	-0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	-0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	-1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}
$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

$T_a = 0°C$ to $70°C$, $V_{DD} = +12V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{CC} = +5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

DC CHARACTERISTICS

T_a = 0°C to +70°C①, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	②
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	② ③
Supply Voltage	V_{SS}	0	0	0	V	②
Supply Voltage	V_{BB}	−4.5	−5.0	−5.5	V	②
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	②
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	②
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0		0.8	V	②
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min. ④
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{DD} Current — All Speeds except μPD416-5	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns ④
Refresh V_{DD} Current — μPD416-5	I_{DD3}			27	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns ④
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns ④
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns ⑤
Standby V_{CC} Current	I_{CC2}	−10		10	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	−10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = 225 ns ⑤
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	−10		10	μA	V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = −5 mA ③
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: ① T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

② All voltages referenced to V_{SS}.

③ Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

④ I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

⑤ I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD416 MIN	μPD416 MAX	μPD416-1 MIN	μPD416-1 MAX	μPD416-2 MIN	μPD416-2 MAX	μPD416-3 MIN	μPD416-3 MAX	μPD416-5 MIN	μPD416-5 MAX	UNIT	TEST CONDITIONS
Random read or write cycle time	t_{RC}	510		410		375		320		320		ns	③
Read-write cycle time	t_{RWC}	575		465		375		375		320		ns	③
Page mode cycle time	t_{PC}	330		275		225		170		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150		120	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		165		135		100		80	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	60	0	50	0	40	0	35	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		150		120		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	10,000	250	10,000	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		165		135		100		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	165	10,000	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		−20		−20		0		ns	
Row address set-up time	t_{ASR}	0		0		0		0		0		ns	
Row address hold time	t_{RAH}	40		35		25		20		15		ns	
Column address set-up time	t_{ASC}	−10		−10		−10		−10		−10		ns	
Column address hold time	t_{CAH}	90		75		55		45		40		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		80		ns	
Read command set-up time	t_{RCS}	0		0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		80		ns	
Write command pulse width	t_{WP}	90		75		55		45		40		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		85		70		50		50		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		85		70		50		50		ns	
Data-in set-up time	t_{DS}	0		0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		40		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		80		ns	
CAS precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		60		ns	
Refresh period	t_{REF}		2		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−20		−20		−20		−20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	140		125		95		70		80		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	240		200		160		120		120		ns	⑩

① AC measurements assume t_T = 5 ns.

② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}

③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑥ Measured with a load equivalent to 2 TTL loads and 100 pF.

⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}

⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) $\geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

DERATING CURVES

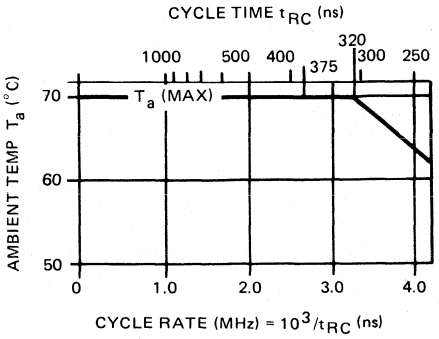


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375 ns) is determined by T_a (max) [°C] = 70 – 9.0 x (cycle rate [MHz] –2.66). For μPD416-5, it is T_a (max) [°C] = 70 – 9.0 (cycle rate [MHz] – 3.125).

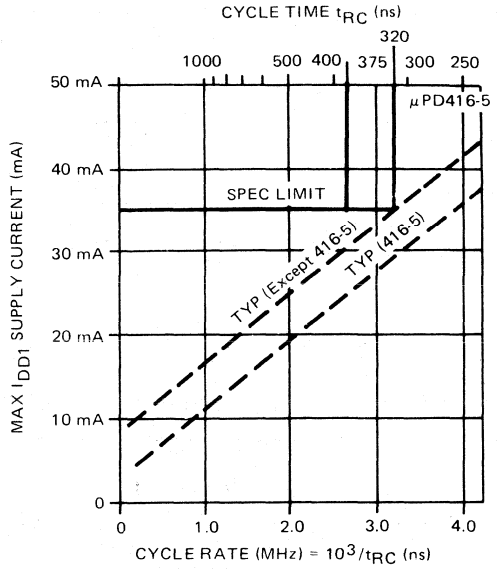


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

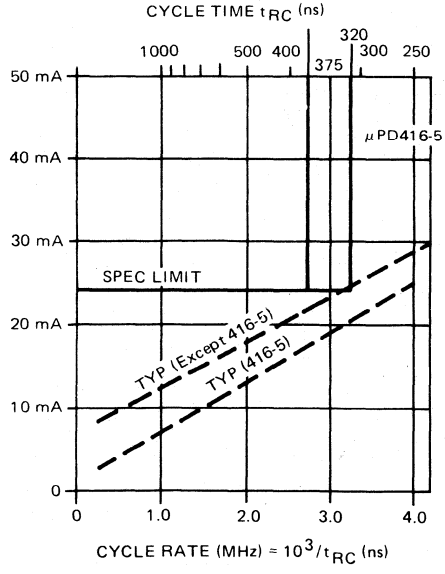


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

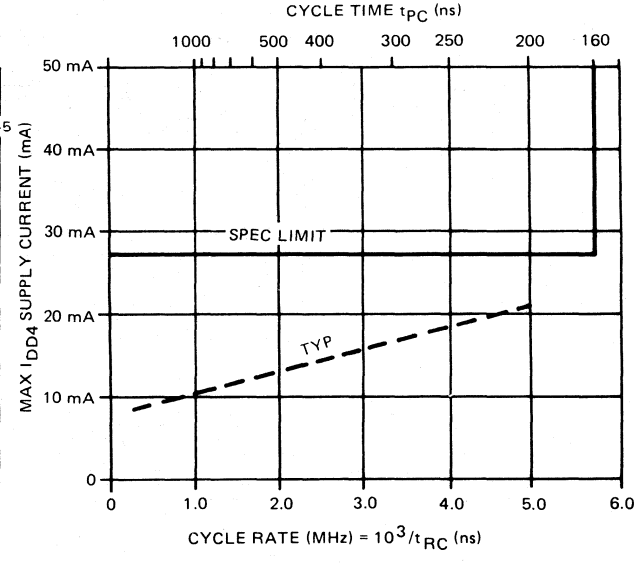
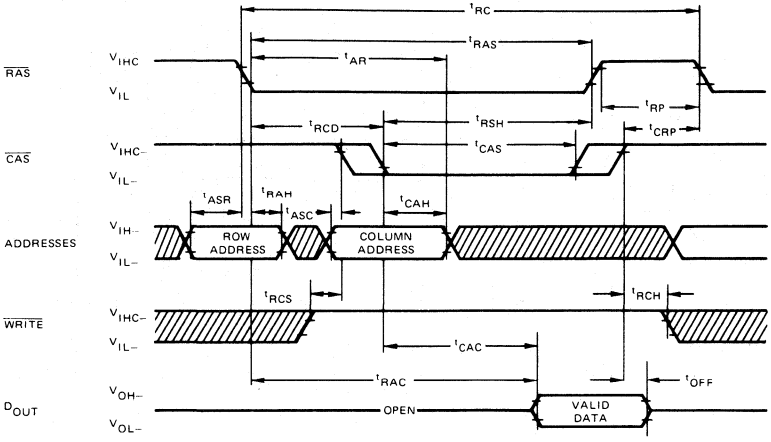


FIGURE 4

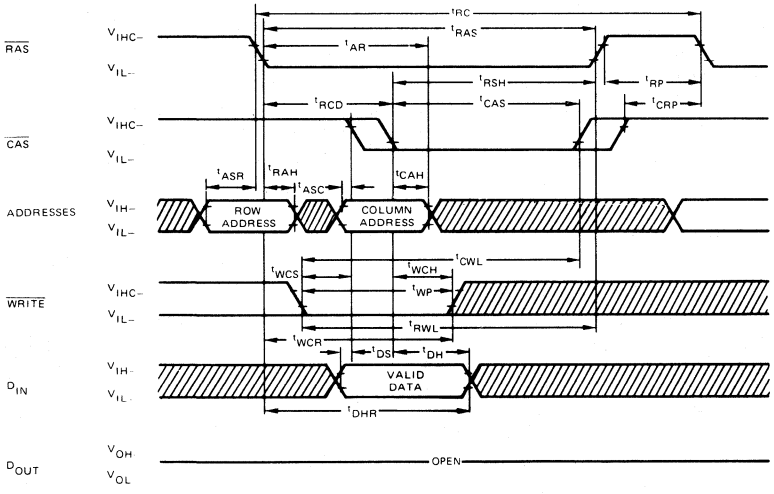
Maximum I_{DD4} versus cycle rate for device operation in page mode.

TIMING WAVEFORMS

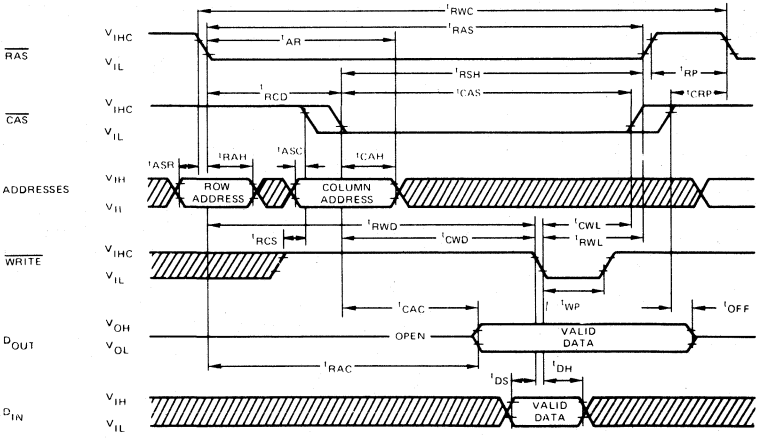
READ CYCLE



WRITE CYCLE

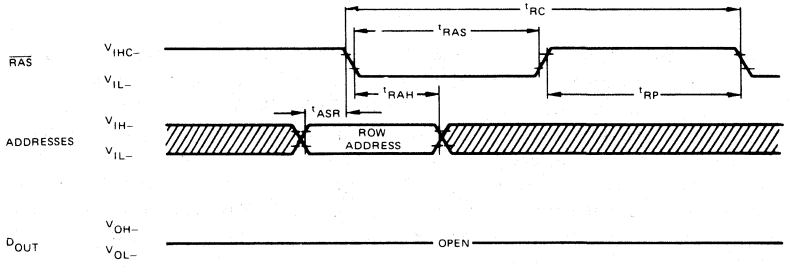


READ-WRITE/READ-MODIFY-WRITE CYCLE



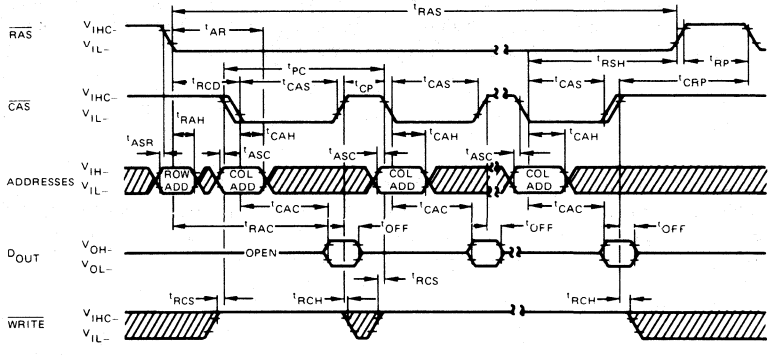
TIMING WAVEFORMS (CONT.)

"RAS-ONLY" REFRESH CYCLE

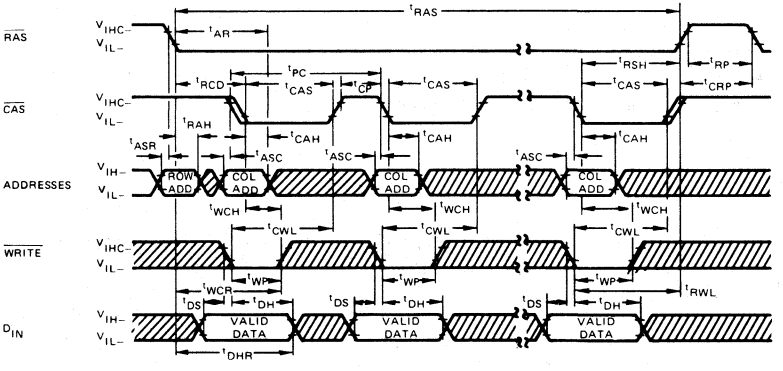


Note: $\overline{CAS}$ = V_{IHC-}, $\overline{WRITE}$ = Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only" cycles can be used for simple refreshing operation.

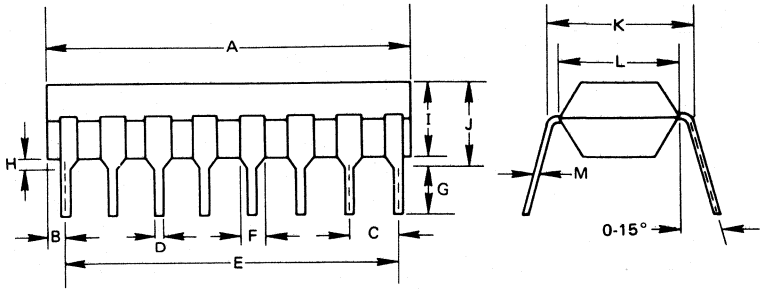
CHIP SELECTION

Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

POWER SEQUENCING

In order to assure long term reliability, V_{BB} should be applied first during power up and removed last during power down.

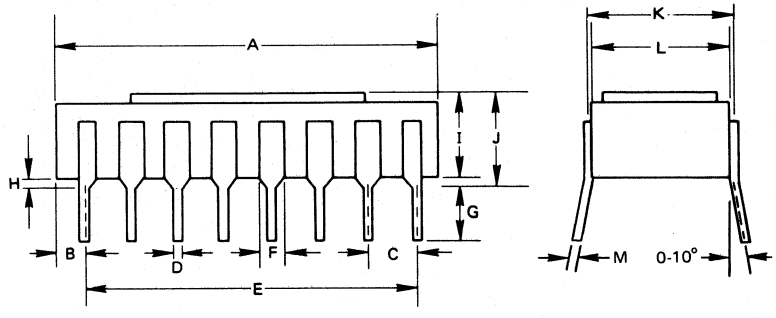
PACKAGE OUTLINES
μPD416C
PLASTIC



Plastic

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

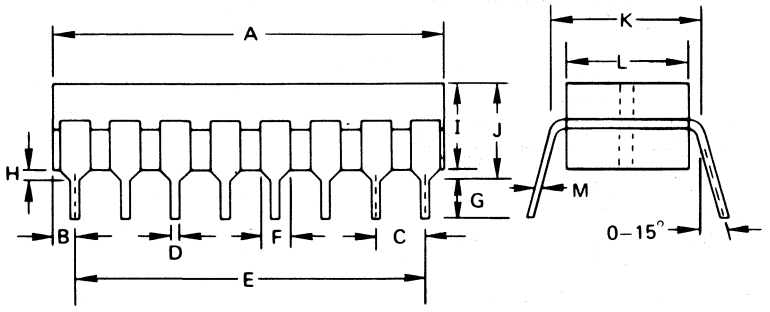
μPD416D
CERAMIC



Ceramic

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

PACKAGE OUTLINE
μPD416D
CERDIP



Cerdip

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

65,536 x 1 BIT DYNAMIC RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD4164 is a 65,536 words by 1 bit Dynamic N-Channel MOS RAM designed to operate from a single +5V power supply. The negative-voltage substrate bias is internally generated — its operation is both automatic and transparent.

The μPD4164 utilizes a double-poly-layer N-channel silicon gate process which provides high storage cell density, high performance and high reliability.

The μPD4164 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers, which assures that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between Dynamic RAM generations.

The μPD4164 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The μPD4164 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$ only refresh cycles.

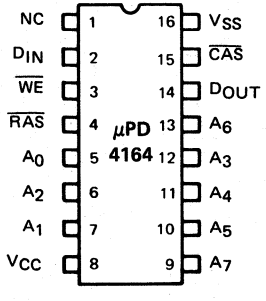
Refreshing is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2 ms period.

Multiplexed address inputs permit the μPD4164 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

FEATURES

- High Memory Density
- Multiplexed Address Inputs
- Single +5V Supply
- On Chip Substrate Bias Generator
- Access Time: μPD4164-1 — 250 ns
  μPD4164-2 — 200 ns
  μPD4164-3 — 150 ns
- Read, Write Cycle Time: μPD4164-1 — 410 ns
  μPD4164-2 — 335 ns
  μPD4164-3 — 270 ns
- Low Power Dissipation: 250 mW (Active); 28 mW (Standby)
- Non-Latched Output is Three-State, TTL Compatible
- Read, Write, Read-Write; Read-Modify-Write, RAS Only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Input Capacitance
- 128 Refresh Cycles (A_0-A_6 Pins for Refresh Address)
- CAS Controlled Output Allows Hidden Refresh
- Available in Both Ceramic and Plastic 16 Pin Packages

PIN CONFIGURATION



PIN NAMES

A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

Rev/1

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . -55°C to +150°C
(Plastic Package) . . . . . -55°C to +125°C
Supply Voltages On Any Pin Except V_{CC} . . . . . -1 to +7 Volts ①
Supply Voltage V_{CC} . . . . . -0.5 to +7 Volts ①
Short Circuit Output Current . . . . . 50 mA
Power Dissipation . . . . . 1 Watt

Note: ① Relative to V_{SS}

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0° to 70°C ① ; V_{CC} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}		4.5	5.0	5.5	V	All Voltages Referenced to V_{SS}
	V_{SS}		0	0	0	V	
High Level Input Voltage, ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	V_{IHC}		2.4		5.5	V	
High Level Input Voltage, All Inputs Except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IH}		2.4		5.5	V	
Low Level Input Voltage, All Inputs	V_{IL}		-2.0		0.8	V	
Operating Current Average Power Supply Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = t_{RC} (Min.)	I_{CC1}	μPD4164-1			45	mA	②
		μPD4164-2			50		
		μPD4164-3			60		
Standby Current Power Supply Standby Current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = Hi-Impedance)	I_{CC2}				5.0	mA	
Refresh Current Average Power Supply Current, Refresh Mode; $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = t_{RC} (Min.)	I_{CC3}	μPD4164-1			35	mA	②
		μPD4164-2			40		
		μPD4164-3			45		
Page Mode Current Average Power Supply Current, Page Mode Operation $\overline{RAS}$ = V_{IL}; $\overline{CAS}$ Cycling t_{PC} = t_{PC} (Min.)	I_{CC4}	μPD4164-1			35	mA	②
		μPD4164-2			40		
		μPD4164-3			45		
Input Leakage Current Any Input V_{IN} = 0 to +5.5 Volts, All Other Pins Not Under Test = 0V	$I_{I(L)}$		-10		10	μA	
Output Leakage Current D_{OUT} is Disabled, V_{OUT} = 0 to +5.5 Volts	$I_{O(L)}$		-10		10	μA	
Output Levels High Level Output Voltage (I_{OUT} = 5 mA)	V_{OH}		2.4		V_{CC}	V	
Low Level Output Voltage (I_{OUT} = 4.2 mA)	V_{OL}		0		0.4	V	

Notes: ① T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met.
② I_{CC1}, I_{CC3} and I_{CC4} depend on output loading and cycle rates. Specified rates are obtained with the output open.

AC CHARACTERISTICS

T_a = 0° to +70°C ①; V_{CC} = +5V ± 10%; V_{SS} = 0V ③ ④

PARAMETER	SYMBOL	LIMITS μPD4164-1 MIN	μPD4164-1 MAX	μPD4164-2 MIN	μPD4164-2 MAX	μPD4164-3 MIN	μPD4164-3 MAX	UNIT	TEST CONDITIONS
Random Read or Write Cycle Time	t_{RC}	410		335		270		ns	⑤
Read Write Cycle Time	t_{RWC}	465		335		270		ns	⑥
Page Mode Cycle Time	t_{PC}	275		225		170		ns	
Access Time from $\overline{RAS}$	t_{RAC}		250		200		150	ns	⑥ ⑧
Access Time from $\overline{CAS}$	t_{CAC}		165		135		100	ns	⑦ ⑧
Output Buffer Turn-Off Delay	t_{OFF}	0	60	0	50	0	40	ns	⑨
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	④
$\overline{RAS}$ Precharge Time	t_{RP}	150		120		100		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	250	10,000	200	10,000	150	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	165		135		100		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	165	10,000	135	10,000	100	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	250		200		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	35	85	30	65	25	50	ns	⑩
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		0		ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	35		30		25		ns	
$\overline{CAS}$ Precharge Time (For Page Mode Cycle Only)	t_{CP}	100		80		60		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	0		0		0		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	25		20		15		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	75		55		45		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	160		120		95		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	30		25		20		ns	⑬
Read Command Hold Time	t_{RCH}	0		0		0		ns	⑬
Write Command Hold Time	t_{WCH}	75		55		45		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	160		120		95		ns	
Write Command Pulse Width	t_{WP}	75		55		45		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	100		55		45		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	100		55		45		ns	
Data-In Set-Up Time	t_{DS}	0		0		0		ns	⑪
Data-In Hold Time	t_{DH}	75		55		45		ns	⑪
Data-In Hold Time Referenced to $\overline{RAS}$	t_{DHR}	160		120		95		ns	
Refresh Period	t_{REF}		2		2		2	ms	
$\overline{WRITE}$ Command Set-Up Time	t_{WCS}	−20		−20		−20		ns	⑫
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	115		80		60		ns	⑫
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	200		145		110		ns	⑫

Notes:
① T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.

② An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

③ AC measurements assume t_T = 5 ns.

④ V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

⑤ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle times at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

⑥ Assumes that $t_{RCS} \leq t_{RCD}$ (max). If t_{RCS} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑦ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑧ Measured with a load equivalent to 2 TTL loads and 100 pF.

⑨ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

⑩ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

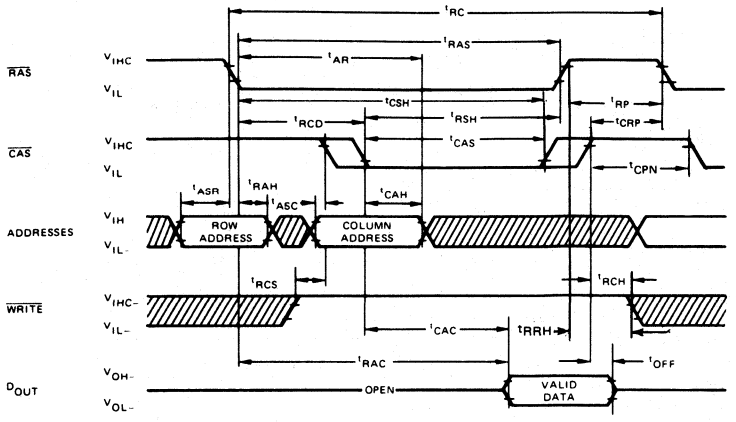
⑪ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

⑫ t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

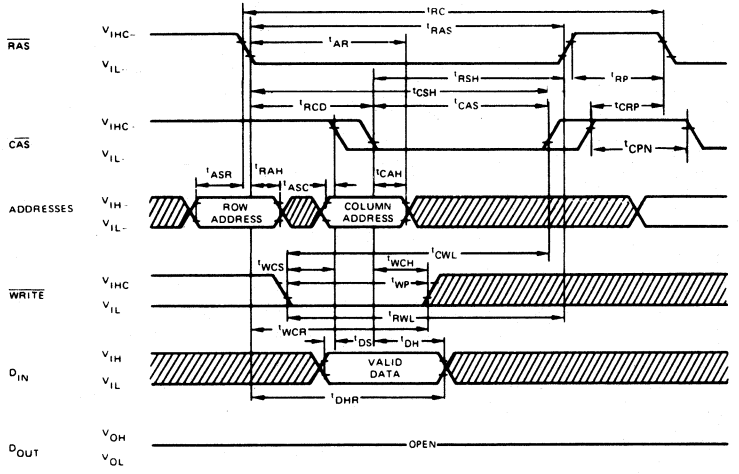
⑬ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

TIMING WAVEFORMS

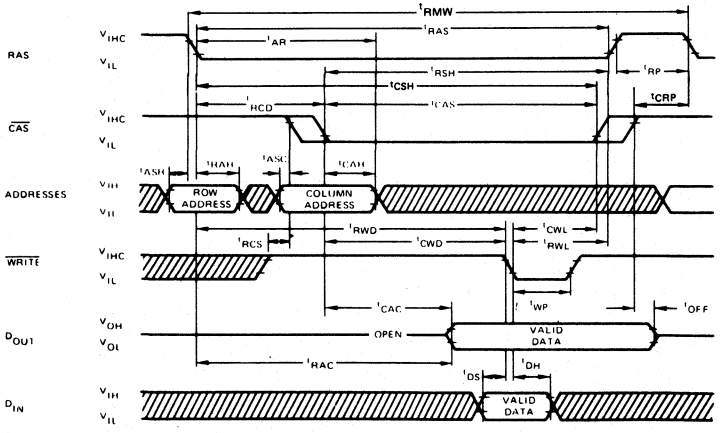
READ CYCLE



WRITE CYCLE (EARLY WRITE)

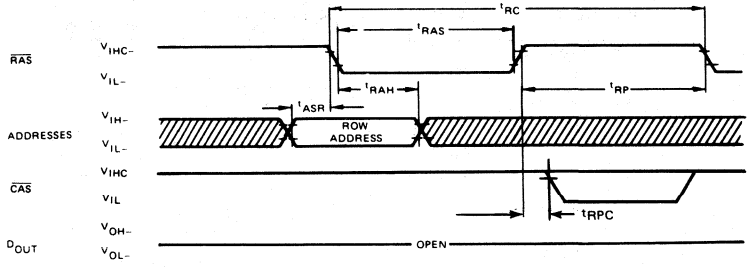


READ-WRITE/READ-MODIFY-WRITE CYCLE

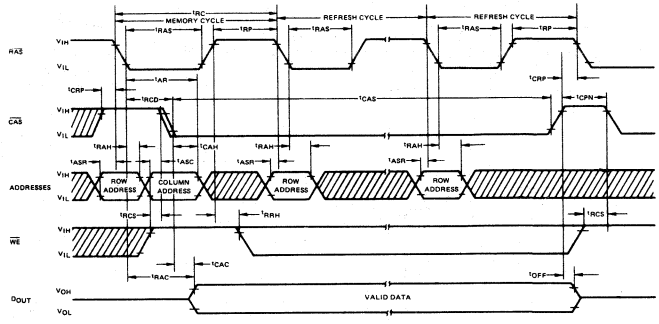


TIMING WAVEFORMS
(CONT.)

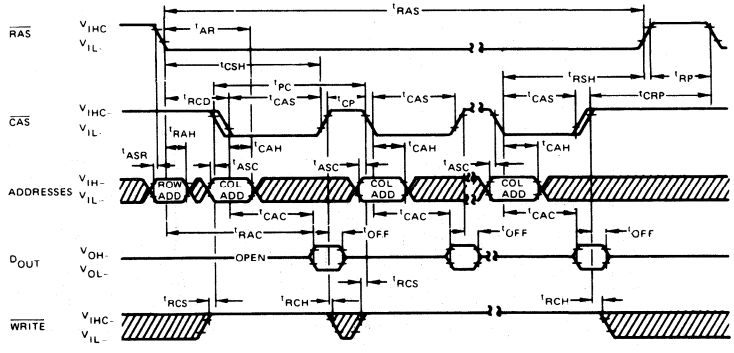
"RAS-ONLY" REFRESH CYCLE



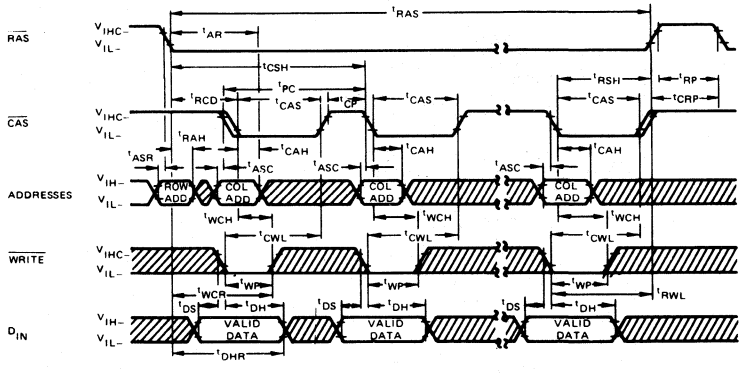
HIDDEN REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



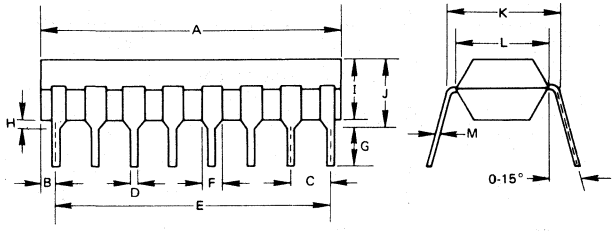
CAPACITANCE

$T_a = 0°$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_7), D_{IN}	C_{I1}			5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}			10	pF	
Output Capacitance (D_{OUT})	C_O			7	pF	

PACKAGE OUTLINES

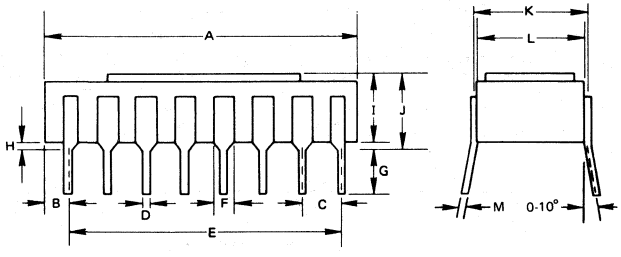
μPD4164C



Plastic

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

μPD4164D



Ceramic

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

4096 × 1 STATIC NMOS RAM

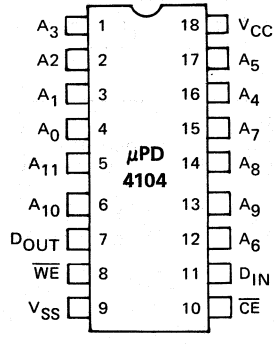
DESCRIPTION

The μPD4104 is a high performance 4K static RAM. Organized as 4096 x 1, it uses a combination of static storage cells with dynamic input/output circuitry to achieve high speed and low power in the same device. Utilizing NMOS technology, the μPD4104 is fully TTL compatible and operates with a single +5V ± 10% supply.

FEATURES

- Fast Access Time – 200 ns (μPD4104-2)
- Very Low Stand-By Power – 28 mW Max.
- Low V_{CC} Data Retention Mode to +3 Volts.
- Single +5V ±10% Supply.
- Fully TTL Compatible.
- Available in 18 Pin Plastic and Ceramic Dual-in-Line Packages.
- 3 Performance Ranges:

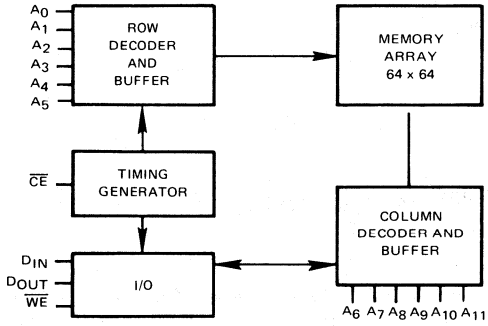
	ACCESS TIME	R/W CYCLE	SUPPLY CURRENT		
			ACTIVE	STANDBY	LOW V_{CC}
μPD4104	300 ns	460 ns	21 mA	5 mA	5 mA
μPD4104-1	250 ns	385 ns	21 mA	5 mA	3.3 mA
μPD4104-2	200 ns	310 ns	25 mA	5 mA	3.3 mA



PIN NAMES

A_0-A_{11}	Address Inputs
$\overline{CE}$	Chip Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{SS}	Ground
V_{CC}	Power (+5V)
$\overline{WE}$	Write Enable

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−1 to +7 Volts ①
Power Dissipation	1 Watt
Short Circuit Output Current	50 mA

Note: ① With respect to V_{SS}

$T_a = 25°C$

* COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS ① ⑥

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	①
Logic "1" Voltage All Inputs		V_{IH}	2.2	−3	7.0	V	
Logic "0" Voltage All Inputs		V_{IL}	−1.0		0.8	V	
Average V_{CC} Power Supply Current	μPD4104	I_{CC1}			21	mA	②
	μPD4104-1	I_{CC1}			21	mA	
	μPD4104-2	I_{CC1}			25	mA	
Standby V_{CC} Power Supply Current		I_{CC2}			5	mA	③
Input Leakage Current (Any Input)		I_{IL}	−10		10	μA	④
Output Leakage Current		I_{OL}	−10		10	μA	③ ⑤
Output Logic "1" Voltage I_{OUT} −500 μA		V_{OH}	2.4			V	
Output Logic "0" Voltage I_{OUT} 5mA		V_{OL}			0.4	V	

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	⑦
Output Capacitance	C_{OUT}		6	7	pF	⑦

Notes: ① All voltages referenced to V_{SS}

② I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by

$$I_{CC1} \text{ (ma)} = (5t_p + 13\,(t_C - t_p) + 3420)\ t_C$$

where t_p and t_C are expressed in nanoseconds. Equation is referenced to the **−2 device**, other devices derate to the same curve.

③ Output is disabled (open circuit), $\overline{CE}$ is at logic 1.

④ All device pins at 0 volts except pin under test at 0. $V_{IN} = 5.5$ volts.

⑤ $0V \leq V_{OUT} \leq +5.5V$.

⑥ During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.

⑦ Effective capacitance calculated from the equation $C = \frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.

AC CHARACTERISTICS ② ⑦

T_a = 0°C to +70°C, V_{CC} = +5V ± 10% ①

PARAMETER	SYMBOL	LIMITS 4104 MIN	4104 MAX	4104-1 MIN	4104-1 MAX	4104-2 MIN	4104-2 MAX	UNIT	TEST CONDITIONS
Read or Write Cycle Time	t_C	460		385		310		ns	⑧
Random Access	t_{AC}		300		250		200	ns	③
Chip Enable Pulse Width	t_{CE}	300	10,000	250	10,000	200	10,000	ns	
Chip Enable Precharge Time	t_P	150		125		100		ns	
Address Hold Time	t_{AH}	165		135		110		ns	
Address Set-Up Time	t_{AS}	0		0		0		ns	
Output Buffer Turn-Off Delay	t_{OFF}	0	75	0	65	0	50	ns	⑨
Read Command Set-Up Time	t_{RS}	0		0		0		ns	④
Write Enable Set-Up Time	t_{WS}	−20		−20		−20		ns	④
Data Input Hold Time Referenced to $\overline{WE}$	t_{DIH}	25		25		25		ns	
Write Enabled Pulse Width	t_{WW}	90		75		60		ns	
Modify Time	t_{MOD}	0	10,000	0	10,000	0	10,000	ns	⑤
$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	t_{WPL}	105		85		70		ns	⑥
Data Input Set-Up Time	t_{DS}	0		0		0		ns	
Write Enable Hold Time	t_{WH}	225		185		150		ns	
Transition Time	t_T	5	50	5	50	5	50	ns	
Read-Modify-Write Cycle Time	t_{RMW}	565		470		380		ns	⑩

Notes: ① All voltages referenced to V_{SS}

② During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.

③ Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.

④ If $\overline{WE}$ follows $\overline{CE}$ by more than t_{WS} then data out may not remain open circuited.

⑤ Determined by user. Total cycle time cannot exceed t_{CE} max.

⑥ Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.

⑦ AC measurements assume t_T = 5 ns. Timing points are taken as V_{IL} = 0.8V and V_{IH} = 2.2V on the inputs and V_{OL} = 0.4V and V_{OH} = 2.4V on the output waveform.

⑧ $t_C = t_{CE} + t_P + 2t_T$.

⑨ The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.

⑩ $t_{RMW} = t_{AC} + t_{WPL} + t_P + 3t_T + t_{MOD}$.

STANDBY CHARACTERISTICS

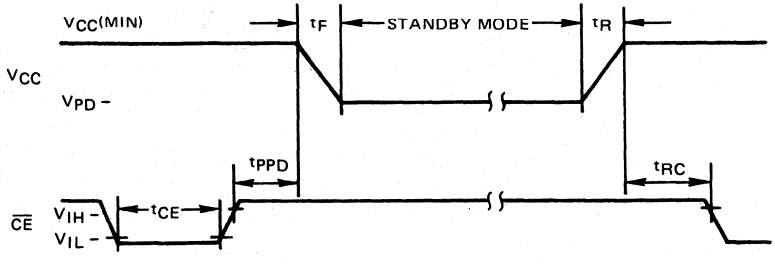
T_a = 0°C to +70°C

PARAMETER	SYMBOL	LIMITS 4104 MIN	4104 MAX	4104-1 MIN	4104-1 MAX	4104-2 MIN	4104-2 MAX	UNIT	TEST CONDITIONS
V_{CC} In Standby	V_{PD}	3.0		3.0		3.0		V	
Standby Current	I_{PD}		5.0		3.3		3.3	mA	①
Power Supply Fall Time	T_F	100		100		100		μs	
Power Supply Rise Time	T_R	100		100		100		μs	
Chip Enable Pulse $\overline{CE}$ Width	T_{CE}	300		250		200		μs	
Chip Enable Precharge to Power Down Time	T_{PPD}	150		125		100		ns	
"I" Level $\overline{CE}$ Min Level	V_{IH}	2.2		2.2		2.2		V	
Standby Recovery Time	T_{RC}	500		500		500		μs	

Note: ① Maximum value for V_{PD} minimum value (= 3 V).

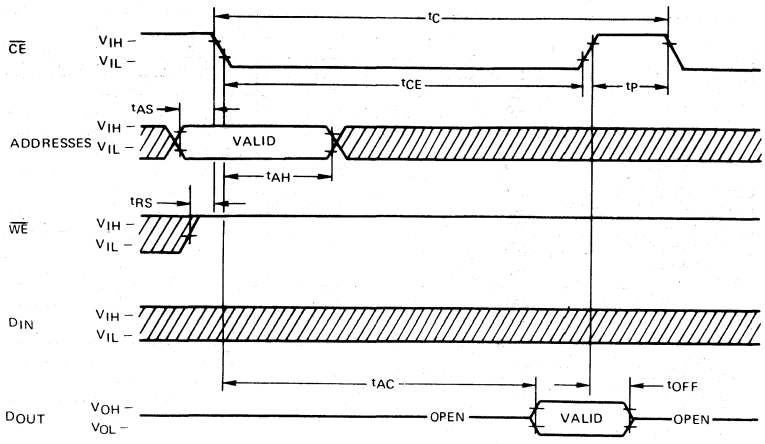
TIMING WAVEFORMS

POWER DOWN

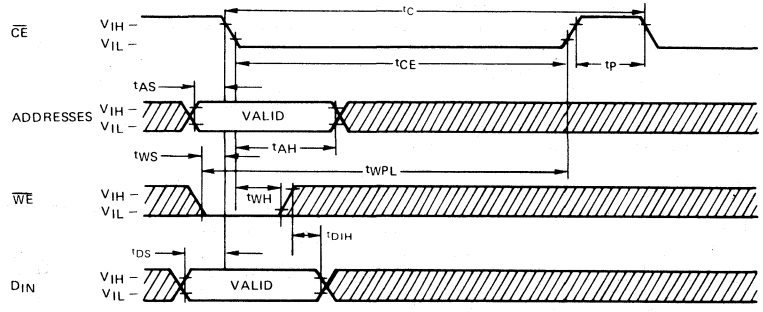


TIMING WAVEFORMS (CONT.)

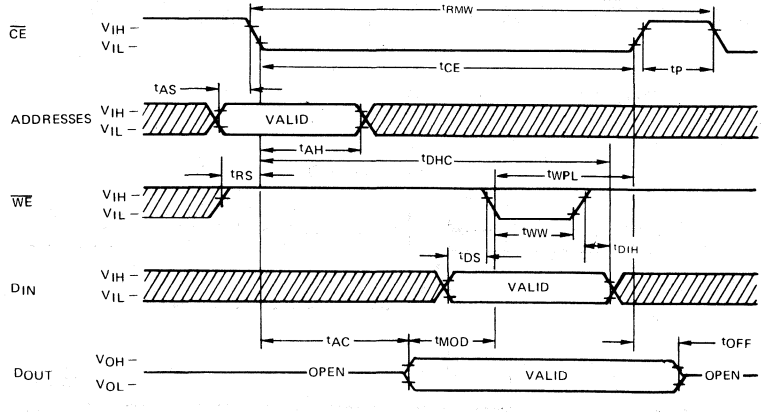
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



OPERATIONAL DESCRIPTION

READ CYCLE

The selection of one of the possible 4096 bits is made by virtue of the 12 address bits presented at the inputs. These are latched into the chip by the negative going edge of chip enable ($\overline{CE}$). If the write enable ($\overline{WE}$) input is held at a high level (V_{IH}) while the $\overline{CE}$ input is clocked to a low level (V_{IL}), a read operation will be performed. At the access time (t_{AC}), valid data will appear at the output. Since the output is unlatched by a positive transition of $\overline{CE}$, it will be in the high impedance state from the previous cycle until the access time. It will go to the high impedance state again at the end of the current cycle when $\overline{CE}$ goes high.

The address lines may be set up for the next cycle any time after the address hold time has been satisfied for the current cycle.

WRITE CYCLE

Data to be written into a selected cell is latched into the chip by the later negative transition of $\overline{CE}$ or $\overline{WE}$. If $\overline{WE}$ is brought low before $\overline{CE}$, the cycle is an "Early Write" cycle, and data will be latched by $\overline{CE}$. If $\overline{CE}$ is brought low before $\overline{WE}$, as in a Read-Modify-Write cycle, then data will be latched by $\overline{WE}$.

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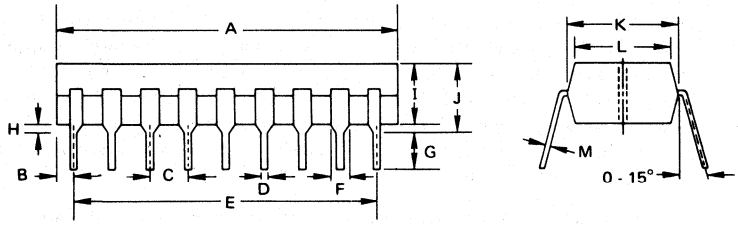
If the cycle is an "Early Write" cycle, the output will remain in the high impedance state. For a Read-Modify-Write cycle; the output will be active for the Modify and Write portions of the memory cycle until $\overline{CE}$ goes high. If $\overline{WE}$ is brought low after $\overline{CE}$ but before the access time, the state of the output will be undefined. The desired data will be written into the cell if data-in is valid on the leading edge of $\overline{WE}$, t_{DIH} is satisfied, and $\overline{WE}$ occurs prior to $\overline{CE}$ going high by at least the minimum lead time (t_{WPL}).

READ-MODIFY-WRITE

Read and Write cycles can be combined to allow reading of a selected location and then modifying that data within the same memory cycle. Data is read at the access time and modified during a period defined by the user. New data is written between $\overline{WE}$ low and the positive transition of $\overline{CE}$. Data out will remain valid until the rising edge of $\overline{CE}$. A minimum R-M-W cycle time can be calculated by $t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3\,t_T$; where t_{RMW} is the cycle time, t_{AC} is the access time, t_{MOD} is the user defined modify time, t_{WPL} is the $\overline{WE}$ to $\overline{CE}$ lead time, t_P is the $\overline{CE}$ high time, and t_T is one transition time.

POWER DOWN MODE

In power down, data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leqslant$4.5V) $\overline{CE}$ must be taken high (V_{IH} = 2.2V) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, $\overline{CE}$ must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.



PACKAGE OUTLINES
μPD4104C

Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

4096 BIT (1024 × 4 BITS) STATIC RAM

DESCRIPTION

The NEC μPD2114L is a 4096 bit static Random Access Memory organized as 1024 words by 4 bits using N-channel Silicon-gate MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding. It therefore requires no clocks or refreshing to operate and simplifies system design. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

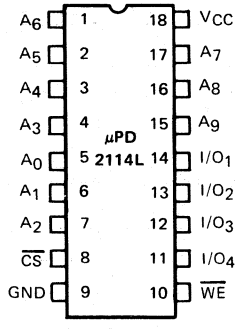
The μPD2114L is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The μPD2114L is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-Tied.

FEATURES

- Access Time: Selection from 150-450 ns
- Single +5 Volt Supply
- Directly TTL Compatible — All Inputs and Outputs
- Completely Static — No Clock or Timing Strobe Required
- Low Operating Power — Typically 0.06 mW/Bit
- Identical Cycle and Access Times
- Common Data Input and Output using Three-State Output
- High Density 18-pin Plastic and Ceramic Packages
- Replacement for 2114L and Equivalent Devices

PIN CONFIGURATION

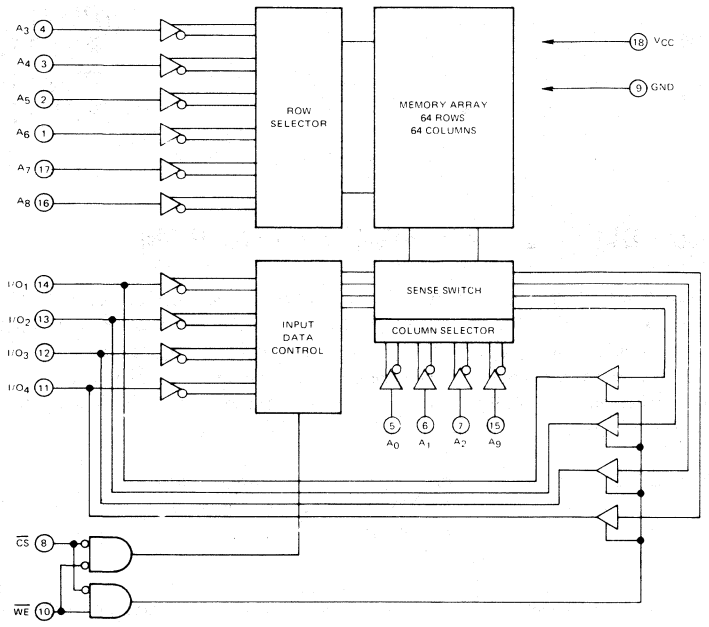


PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

Rev/2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +80°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on any Pin . . . . . −0.5 to 7 Volts ①

Note: ① With respect to ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 10\%$ unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	$V_{IN} = 0$ to 5.5V
I/O Leakage Current	I_{LO}			10	μA	$\overline{CS} = 2V$, $V_{I/O} = 0.4V$ to V_{CC}
Power Supply Current	I_{CC1}			65	mA	$V_{IN} = 5.5V$, $I_{I/O} = 0$ mA, $T_a = 25°C$
Power Supply Current	I_{CC2}			70	mA	$V_{IN} = 5.5V$, $I_{I/O} = 0$ mA, $T_a = 0°C$
Input Low Voltage	V_{IL}	−3.0		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Current	I_{OL}	3.2			mA	$V_{OL} = 0.4V$
Output High Current	I_{OH}			-1.0	mA	$V_{OH} = 2.4V$, $V_{CC} = 4.75V$
						$V_{OH} = 2.2V$, $V_{CC} = 4.5V$

CAPACITANCE

$T_a = 25°C$; f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input/Output Capacitance	$C_{I/O}$			8	pf	$V_{I/O} = 0V$
Input Capacitance	C_{IN}			5	pf	$V_{IN} = 0V$

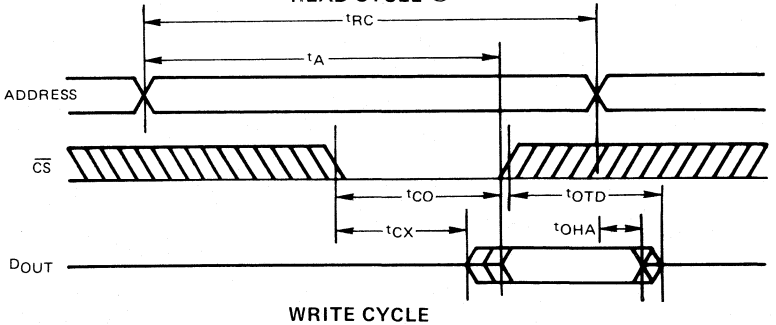
AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

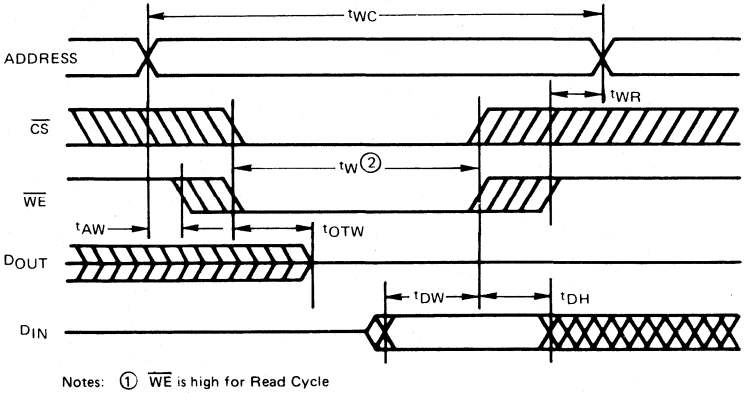
PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		2114L		2114L-1		2114L-2		2114L-3		2114L-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
Read Cycle Time	t_{RC}	450		300		250		200		150		ns	$t_T = t_r = t_f = 10$ ns
Access Time	t_A		450		300		250		200		150	ns	$C_L = 100$ pF
Chip Selection to Output Valid	t_{CO}		120		100		80		70		60	ns	Load = 1 TTL gate
Chip Selection to Output Active	t_{CX}	20		20		20		20		20		ns	Input Levels = 0.8 and 2.0V
Output 3-State from Deselection	t_{OTD}		100		80		70		60		50	ns	$V_{ref} = 1.5$V
Output Hold from Address Change	t_{OHA}	50		50		50		50		50		ns	
WRITE CYCLE													
Write Cycle Time	t_{WC}	450		300		250		200		150		ns	$t_T = t_r = t_f = 10$ ns
Write Time	t_W	200		150		120		120		80		ns	$C_L = 100$ pF
Write Release Time	t_{WR}	0		0		0		0		0		ns	Load = 1 TTL gate
Output 3-State from Write	t_{OTW}		100		80		70		60		50	ns	Input Levels = 0.8 and 2.0V
Data to Write Time Overlap	t_{DW}	200		150		120		120		80		ns	$V_{ref} = 1.5$V
Data Hold from Write Time	t_{DH}	0		0		0		0		0		ns	
Address to Write Setup Time	t_{AW}	0		0		0		0		0		ns	

TIMING WAVEFORMS

READ CYCLE ①



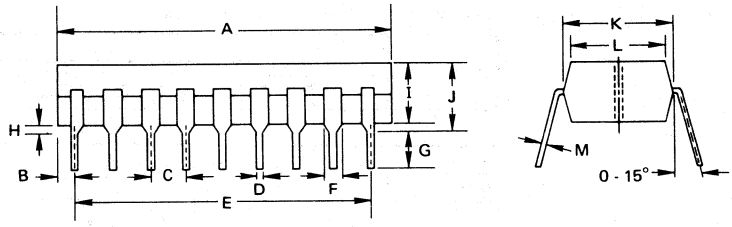
WRITE CYCLE



Notes: ① $\overline{WE}$ is high for Read Cycle

② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

PACKAGE OUTLINES
μPD2114LC



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

4096 x 1 BIT STATIC RAM

DESCRIPTION

The μPD2147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit. Using a scaled NMOS technology, it incorporates an innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. The result is low standby power dissipation without the need for clocks, address setup and hold times. In addition, data rates are not reduced due to cycle times that are longer than access times.

$\overline{CS}$ controls the power down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the μPD2147 — the part automatically reduces its power requirements and remains in this lower power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The μPD2147 is placed in an 18-pin ceramic package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data. A data input and a separate three-state output are used.

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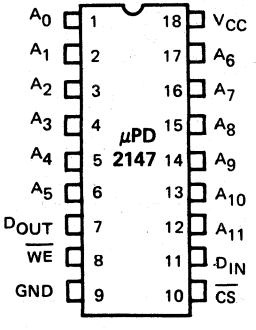
FEATURES

- Scaled NMOS Technology
- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- Automatic Power-Down
- High Density 18-Pin Package
- Directly TTL Compatible — All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Available in a Standard 18-Pin Ceramic Package
- 2 Performance Ranges:

	MAX ACCESS TIME	SUPPLY CURRENT	
		ACTIVE	STANDBY
μPD2147-2	70 ns	160 mA	20 mA
μPD2147-3	55 ns	160 mA	20 mA
μPD2147-5	45 ns	160 mA	20 mA

PIN CONFIGURATION



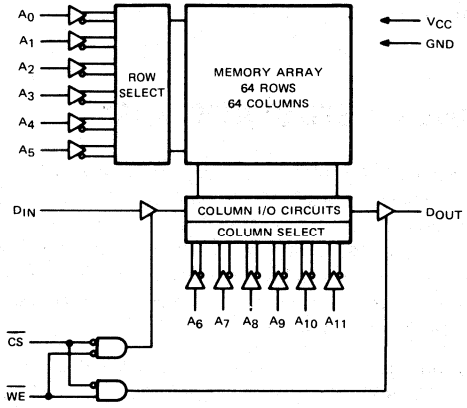
PIN NAMES

A_0-A_{11}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -10°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin . . . . . -3.5V to +7 Volts ①
DC Output Current . . . . . 20 mA
Power Dissipation . . . . . 1.2 W

Note: ① with respect to ground

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$, unless otherwise noted. ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ②	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}		0.01	10	μA	V_{CC} = Max, V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}		0.01	10	μA	$\overline{CS}$ = V_{IH}, V_{CC} = Max, V_{OUT} = GND to V_{CC}
Operating Current	I_{CC}		120	150	mA	$T_a = 25°C$; V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open
				160	mA	$T_a = 0°C$
Standby Current	I_{SB}		12	20	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}
Peak Power-On Current	I_{PO} ③		25	50	mA	V_{CC} = GND to V_{CC} = Min, $\overline{CS}$ = Lower of V_{CC} or V_{IH}Min
Input Low Voltage	V_{IL}	-3.0		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -4.0 mA
Output Short Circuit Current	I_{OS}	-150		+150	mA	V_{OUT} = GND to V_{CC}

Notes: ① The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
② Typical limits are V_{CC} = 5V, T_a = +25°C, and specified loading.
③ I_{CC} exceeds I_{SB} maximum during power on. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

CAPACITANCE

$T_a = 25°C$; f = 1.0 MHz ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			6	pF	V_{OUT} = 0V

Note: ① This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels . . . . . Gnd to 3.0 Volts
Input Rise and Fall Times . . . . . .5 ns
Input and Output Timing Reference Levels . . . . . 1.5 Volts
Output Load . . . . . See Figure 1

AC CHARACTERISTICS READ CYCLE

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$ unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD2147-5 MIN	LIMITS μPD2147-5 MAX	LIMITS μPD2147-3 MIN	LIMITS μPD2147-3 MAX	LIMITS μPD2147-2 MIN	LIMITS μPD2147-2 MAX	UNIT	TEST CONDITIONS
Read Cycle Time	t_{RC} ①	45		55		70		ns	
Address Access Time	t_{AA}		45		55		70	ns	
Chip Select Access Time	t_{ACS1}		45		55		70	ns	
Chip Select Access Time	t_{ACS2}		45		55		70	ns	
Output Hold From Address Change	t_{OH}	5		5		5		ns	
Chip Select to Output in Low Z	t_{CZ} ②	10		10		10		ns	③
Chip Deselection to Output in High Z	t_{HZ} ②	0	30	0	30	0	40	ns	④
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns	
Chip Selection to Power-Down Time	t_{PD}		20		20		30	ns	

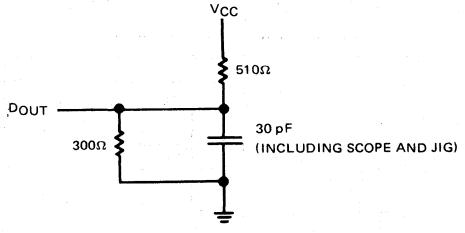
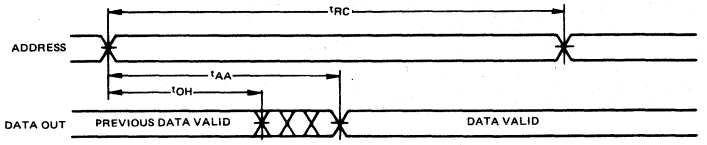


Figure 1

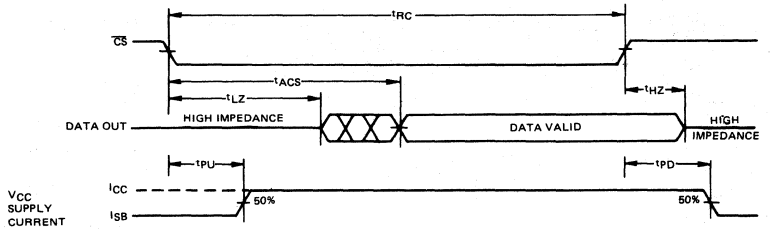
Notes: ① All Read Cycle timings are referenced from the last valid address to the first transitioning address.
② At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min. both for a given device and from device to device.
③ Transition is measured ±200 mV from steady state voltage with specified loading.
④ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading.

TIMING WAVEFORMS
READ CYCLE

READ CYCLE NO. 1 ⑤⑥



READ CYCLE NO. 2 ⑤⑦



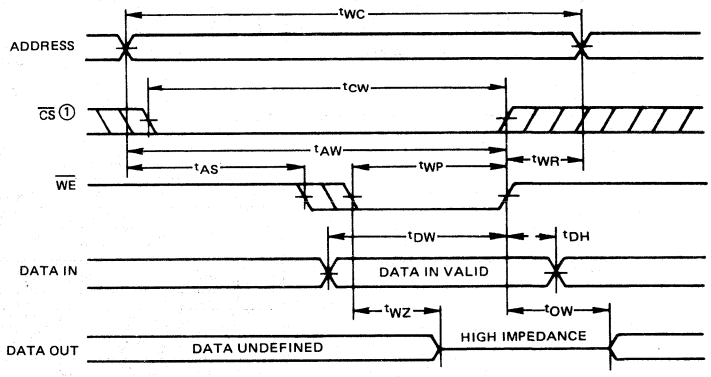
AC CHARACTERISTICS
WRITE CYCLE

PARAMETER	SYMBOL	LIMITS μPD2147-5 MIN	μPD2147-5 MAX	μPD2147-3 MIN	μPD2147-3 MAX	μPD2147-2 MIN	μPD2147-2 MAX	UNIT	TEST CONDITIONS
Write Cycle Time ②	t_{WC}	45		55		70		ns	
Chip Select to End of Write	t_{CW}	45		45		55		ns	
Address Valid to End of Write	t_{AW}	45		45		55		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	25		25		40		ns	
Write Recovery Time	t_{WR}	0		10		15		ns	
Data Valid to End of Write	t_{DW}	25		25		30		ns	
Data Hold Time	t_{DH}	10		10		10		ns	
Write Enabled to Output with Z	t_{WZ}	0	25	0	25	0	35	ns	③
Output Active From End of Write	t_{OW}	0		0		0		ns	④

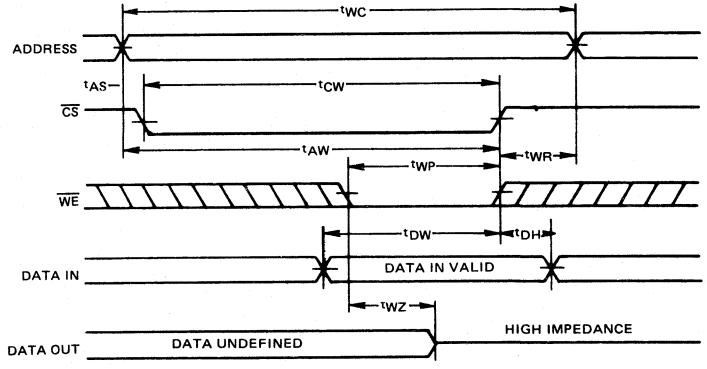
Notes: ① All Read Cycle timings are referenced from the last valid address to the first transitioning address.
② At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min. both for a given device and from device to device.
③ Transition is measured ±200 mV from steady state voltage with specified loading.
④ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading.
⑤ WE is high for Read Cycles.
⑥ Device is continuously selected, $\overline{CS} = V_{IL}$.
⑦ Addresses valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORMS
WRITE CYCLE

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) ⑤

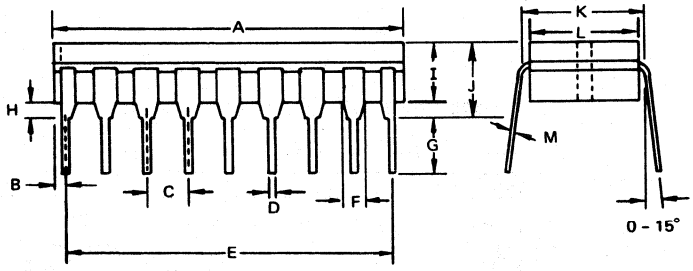


WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) ⑤



Notes: ① If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
② All Write Cycle timings are referenced from the last valid address to the first transitioning address.
③ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading.
④ Transition is measured ±200 mW from steady state voltage with specified loading.
⑤ $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

PACKAGE OUTLINE
μPD2147D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX	0.91 MAX
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	4.6 MAX	0.18 MAX
J	5.1 MAX	0.2 MAX
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

4096 (1024x4) BIT STATIC RAM

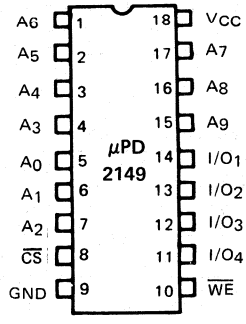
DESCRIPTION

The μPD2149 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits. Using a scaled NMOS technology, it incorporates an innovative design approach which provides the ease-of-use features associated with non-clocked static memories.

The μPD2149 is encapsulated in an 18-pin ceramic package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data.

FEATURES

- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times, Faster Chip Select Access
- Single +5V Supply
- High Density 18-Pin Package
- Directly TTL Compatible — All Inputs and Outputs
- Common Input and Output
- Three-State Output
- Access Time: 35-55 ns MAX (From Address)
  15-25 ns MAX (From Chip Select)
- Power Dissipation: 180 mA MAX



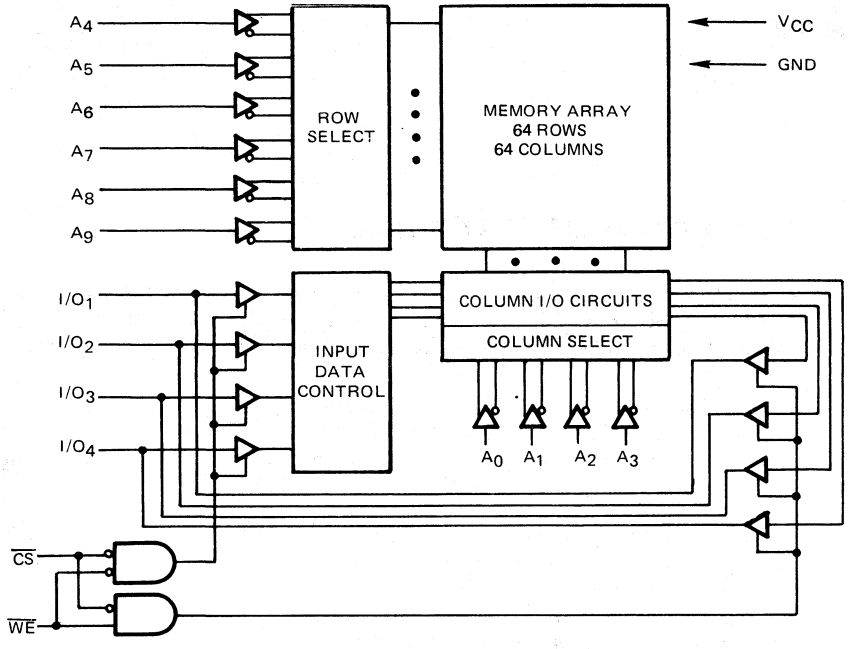
PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O
H	X	Not Selected	High Z
L	L	Write	D_{IN}
L	H	Read	D_{OUT}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−1.5V to +7V ①
DC Output Current	20 mA
Power Dissipation	1.2W

Note: ① with respect to ground

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}		+10	μA	V_{IN} = GND to V_{CC}
Ouput Leakage Current	I_{LO}		+50	μA	CS = V_{IH} V_{OUT} = GND to 4.5V
Power Supply Current	I_{CC}		180	MA	V_{IN} = V_{CC}, I/O = open
Input Low Voltage	V_{IL}		0.8	V	
Input High Voltage	V_{IH}	2.1	V_{CC}	V	
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 MA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −4 MA
Output Short Circuit Current	I_{OS}		±200	MA	V_{OUT} = GND to V_{CC}

Note: The operating temperature range is guaranteed with transverse air flow exceeding 400 feet per minute.

CAPACITANCE

T_a = 25°C; f = 1.0 MHz ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			7	pF	V_{OUT} = 0V

Note: ① This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels . . . . . Gnd to 3.0V
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

AC CHARACTERISTICS READ CYCLE ①

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	2149-2 MIN	2149-2 MAX	2149-1 MIN	2149-1 MAX	2149 MIN	2149 MAX	UNIT	TEST CONDITIONS
Read Cycle Time	T_{RC}	35		45		55		ns	
Access Time	T_A		35		45		55	ns	
Chip Selection to Output Valid	T_{CO}		15		20		25	ns	
Chip Selection to Output Active	T_{CX}	5		5		5		ns	
Output 3-State From Deselection	T_{OTD}		10		15		20	ns	②
Output Hold From Address Change	T_{OH}	5		5		5		ns	

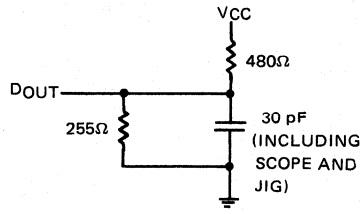


Figure 1

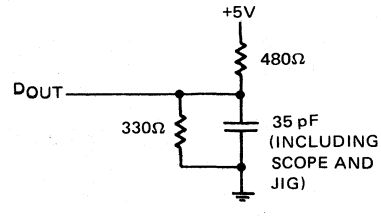


Figure 2

Notes: ① $\overline{WE}$ is high for read cycle.

② Transition is measured ±500 MV from steady state with load of Figure 2. This parameter is sampled and not 100% tested.

AC CHARACTERISTICS WRITE CYCLE

PARAMETER	SYMBOL	μPD2149-2		μPD2149-1		μPD2149		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	35		45		55		ns	
Chip Selection to End of Write	t_{CW}	30		40		50		ns	
Address Valid to End of Write	t_{AW}	30		40		50		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	30		35		40		ns	
Write Recovery Time	t_{WR}	5		5		5		ns	
Data Valid to End of Write	t_{DW}	20		20		20		ns	
Data Hold Time	t_{DH}	5		5		5		ns	
Write Enabled to Output in High Z	t_{WZ}	0	10	0	15	0	20	ns	①
Output Active from End of Write	t_{OW}	0		0		0		ns	②

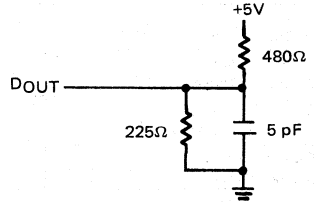


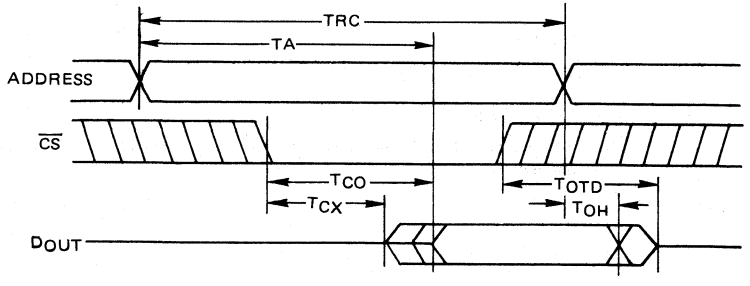
Figure 3

Notes: ① WE or CS must be high during all address transitions.

② Transition is measured +500 MV from steady state with load of Figure 3. This parameter is sampled and not 100% tested.

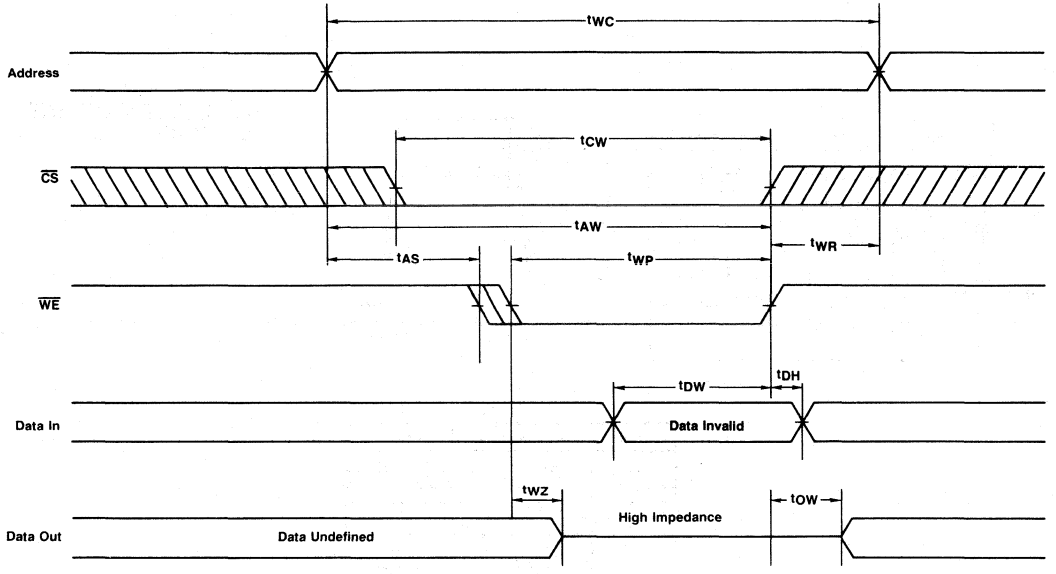
TIMING WAVEFORMS

READ CYCLE ① ②

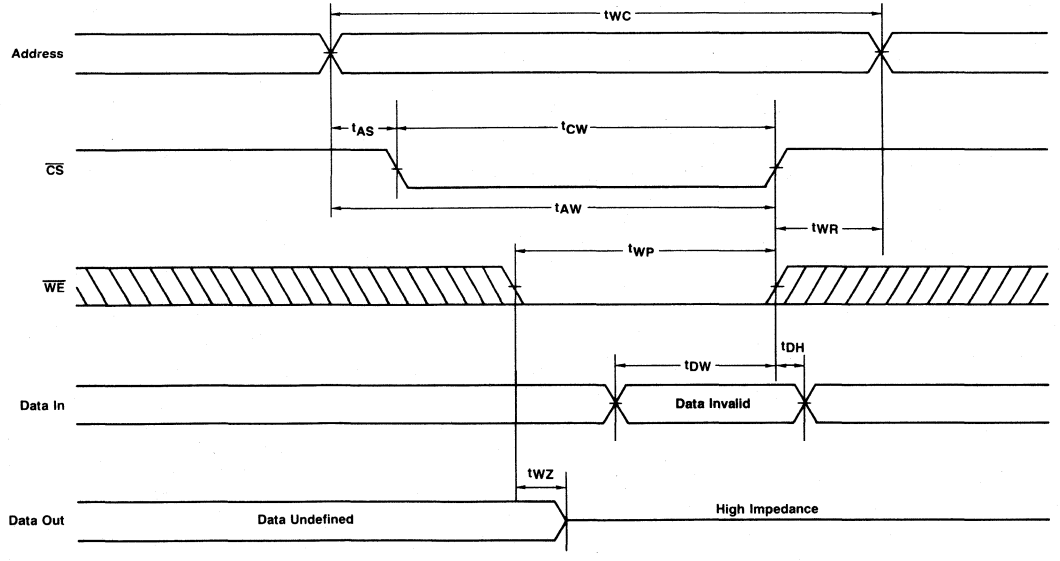


TIMING WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)

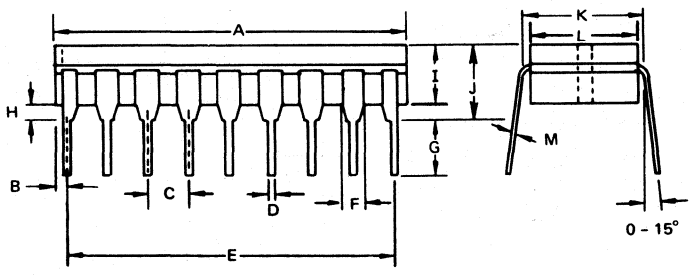


WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



Note: ① Transition is measured ±500 mV from steady state with Load B.
This parameter is sampled and not 100% tested.

PACKAGE OUTLINE
μPD2149D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX	0.91 MAX
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	4.6 MAX	0.18 MAX
J	5.1 MAX	0.2 MAX
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPD2167-2
μPD2167-3
16,384 x 1-BIT STATIC RAM

Description

The μPD2167 is a 16,384-word by 1-bit static MOS RAM. Using a scaled-NMOS technology, its design provides the easy-to-use features associated with non-clocked static memories.

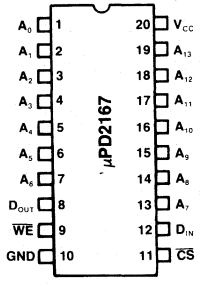
The μPD2167 has a three-state output and offers a standby mode that features an 83% savings in power consumption. The μPD2167 requires a single +5 volt supply and is fully TTL-compatible. It features equal access and cycle times and, because of its fully static operation, it requires no external clocks or timing strobes. It is packaged in a standard 20-pin, 300 mil DIP.

Features

- ☐ 16384 x 1 organization
- ☐ Fully static memory — no clock or timing strobe required
- ☐ Equal access and cycle times
- ☐ Single + 5v supply
- ☐ Automatic power-down
- ☐ Standard 20-pin DIP, 300 mil
- ☐ All inputs and output directly TTL-compatible
- ☐ Separate data input and output
- ☐ Three-state output
- ☐ Power dissipation: 180 mA max (active)
  30 mA max (standby)

	Access time	R/W Cycle time
μPD2167-2	55ns	55ns
μPD2167-3	70ns	70ns

Pin Configuration

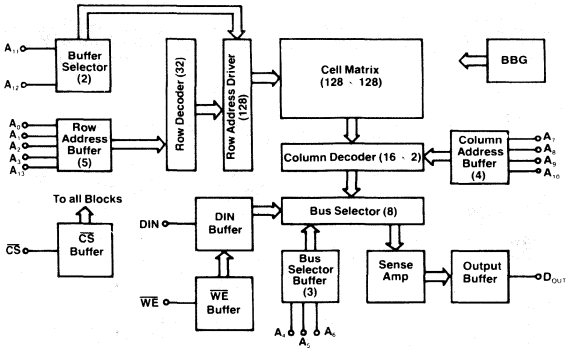


Pin Names

A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5v)
V_{SS}	Ground

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	not selected	High Z	Standby
L	L	write	High Z	Active
L	H	read	D_{OUT}	Active



Absolute Maximum Ratings*

T_a = 25°C

Temperature under bias	−10°C to +85°C
Storage temperature	−65°C to +150°C
Voltage on any pin with respect to ground	−3.5v to +7v
D.C. output current	20mA
Power dissipation	1.2w

*Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C, f = 1.0 MHz

Parameter	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	V_{IN} = OV
Output Capacitance	C_{OUT}	6	pF	V_{OUT} = OV

This parameter is sampled and not 100% tested.

DC Characteristics
T_a = 0°C to +70°C, V_{CC} = +5v ± 10%

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Input load current all input pins	I_{LI}			10	μA	V_{CC} = max, V_{IN} = GND to V_{CC}
Output leakage current	I_{LO}		0.1	50	μA	$\overline{CS}$ = V_{IH}, V_{CC} = max, V_{OUT} = GND to V_{CC}
Operating current	I_{CC}			170	mA	T_A = 25°C; V_{CC} = max, $\overline{CS}$ = V_{IL}, output open
				180	mA	T_A = 0°C; V_{CC} = max, $\overline{CS}$ = V_{IL}, output open
Standby current	I_{SB}			30	mA	V_{CC} = min to max, $\overline{CS}$ = V_{IH}
Peak Power-On current	I_{PO}①		35	70	mA	V_{CC} = GND to V_{CC} min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} min.
Input low voltage	V_{IL}	−3.0		0.8	V	
Input high voltage	V_{IH}	2.0		6.0	V	
Output low voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4			V	I_{OH} = −4 mA
Output short circuit current	I_{OS1}		−150		mA	V_{OUT} = GND
Output short circuit current	I_{OS2}		150		mA	V_{OUT} = V_{CC}

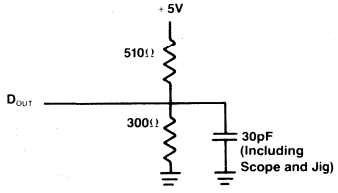


Figure 1 – Output Load

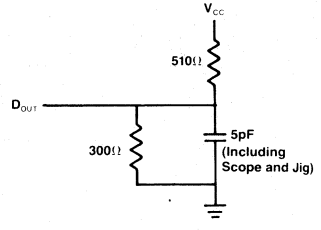


Figure 2 – Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

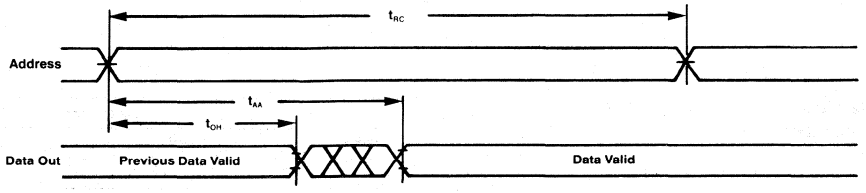
AC Characteristics
T_a = 0°C to +70°C, V_{CC} = +5V ±10%

Parameter	Symbol	μPD2167-3 min	μPD2167-3 typ	μPD2167-3 max	μPD2167-2 min	μPD2167-2 typ	μPD2167-2 max	Unit	Notes
Read Cycle									
Read cycle time	t_{RC}	55			70			ns	
Address access time	t_{AA}			55			70	ns	①
Chip select access time	t_{ACS}			55			70	ns	②
Output hold from address change	t_{OH}	5			5			ns	
Chip select to output in low Z	t_{LZ}	10			10			ns	
Chip deselect to output in high Z	t_{HZ}	0		40	0		40	ns	
Chip select to power up time	t_{PU}	0			0			ns	
Chip deselect to power down time	t_{PD}		30			30		ns	
Write Cycle									
Write cycle time	t_{WC}	55			70			ns	
Chip select to end of write	t_{CW}	45			55			ns	
Address valid to end of write	t_{AW}	45			55			ns	
Address setup time	t_{AS}	0			0			ns	
Write pulse	t_{WP}	35			40			ns	
Write recovery time	t_{WR}	10			15			ns	
Data valid to end of write	t_{DW}	25			30			ns	
Data hold time	t_{DH}	10			10			ns	
Write enabled to output in high Z	t_{WZ}	0		30	0		35	ns	
Output active from end of write	t_{OW}	0			0			ns	

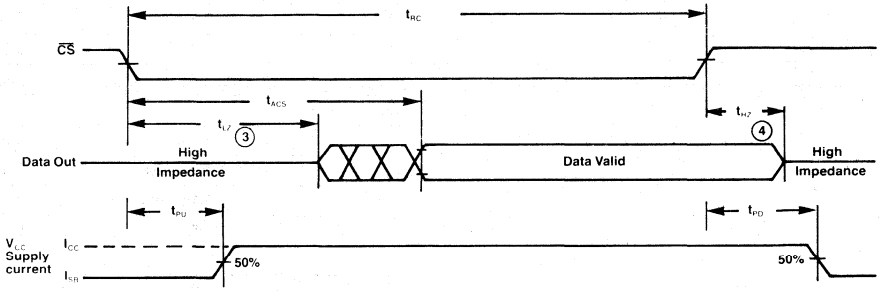
Notes:
① $\overline{CS}$ valid prior to or coincident with address transition
② Address valid prior to or coincident with $\overline{CS}$ transition low

Timing Waveforms

Read Cycle 1 ⑤⑥



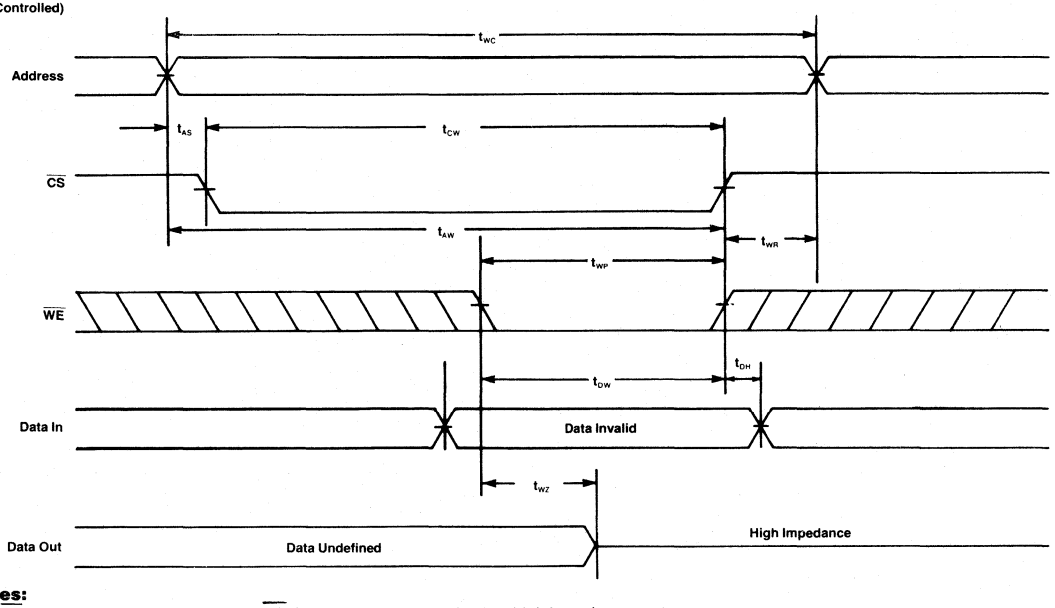
Read Cycle 2 ⑤⑦



Notes:
① All Read Cycle timings are referenced from the last valid address to the first address in transition.
② At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
③ Transition is measured +200mV from steady state voltage with specified loading in Figure 2.
④ Transition is measured at V_{OL} +200mV and V_{OH} −200mV with specified loading in Figure 2.
⑤ $\overline{WE}$ is high for Read Cycles.
⑥ Device is continuously selected, $\overline{CS} = V_{IL}$.
⑦ Addresses valid prior to or coincident with $\overline{CS}$ transition low.

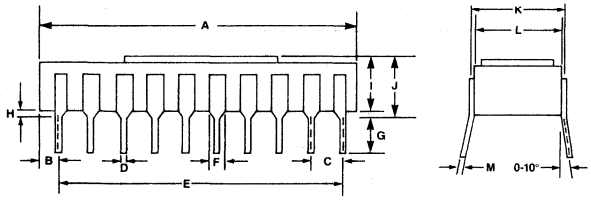
Write Cycle

(CS Controlled)



Notes:
① If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
② All Write Cycle timings are referenced from the last valid address to the first transitioning address.
③ Transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with specified loading in Figure 2.
④ Transition is measured ±200 mV from steady state voltage with specified loading in Figure 2.

Package Outline
μPD2167D (ceramic)



Ceramic		
Item	**Millimeters**	**Inches**
A	25.14 max	0.96 max
B	1.14	0.04
C	2.54	0.1
D	0.5	0.02
E	22.86	0.9
F	1.3	0.05
G	3.2 min	0.13 min
H	0.5 min	0.20 min
I	3.01 max	0.12 max
J	4.15 max	0.16 max
K	7.6	0.3
L	7.3	0.29
M	0.27	0.01

PRELIMINARY

μPD4016-1
μPD4016-2
μPD4016-3
2048 × 8-BIT STATIC RAM

Description

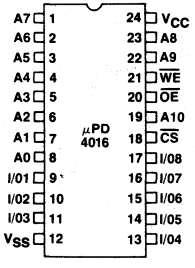
The μPD4016 is a 16384-bit static Random Access Memory device organized as 2048 words by 8 bits. Using a scaled NMOS technology, its design provides the ease-of-use features associated with non-clocked static memories. The μPD4016 has a three-state output and offers a stand-by mode with an attendant 75% savings in power consumption. It features equal access and cycle times and provides an output enable function that eliminates the need for external bus buffers. The μPD4016 is packaged in a standard 24-pin dual-in-line package and is plug-compatible with 16K EPROMS.

Features

- ☐ Scaled NMOS technology
- ☐ Completely static memory: no clock, no refresh
- ☐ Equal access and cycle times
- ☐ Single +5V supply
- ☐ Automatic power-down
- ☐ All inputs and outputs directly TTL-compatible
- ☐ Common I/O capability
- ☐ $\overline{OE}$ eliminates need for external bus buffers
- ☐ Three-state outputs
- ☐ Plug-compatible with 16K 5V EPROMS
- ☐ Low power dissipation in standby mode
- ☐ Available in a standard 24-pin dual-in-line package

	Access Time	R/W Cycle
μPD4016-1	250 ns	250 ns
μPD4016-2	200 ns	200 ns
μPD4016-3	150 ns	150 ns

Pin Configuration

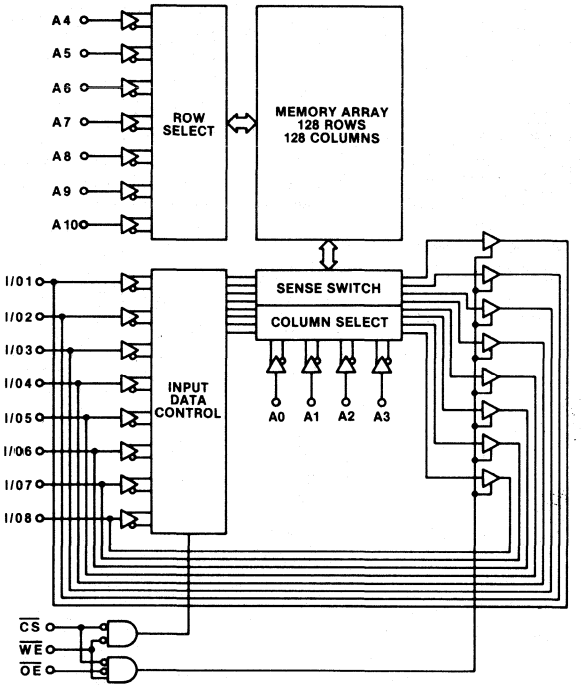


Pin Names	
A0 - A10	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/01 - I/08	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
H	X	X	Not Selected	High-Z	Standby
L	L	H	Read	Dout	Active
L	H	L	Write	Din	Active
L	L	L	Write	Din	Active

Block Diagram



Absolute Maximum Ratings*

T_a = 25°C

Temperature Under Bias ..... −10°C to 85°C
Storage Temperature ..... −65°C to 150°C
Voltage on any pin with respect to Ground −0.5V to 7V
D.C. Output Current 20mA
Power Dissipation 1W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C, f = 1 MHz

Parameter	Symbol	LIMITS Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			5	pF	V_{IN} = OV
I/O Capacitance	$C_{I/O}$			7	pF	$V_{I/O}$ = OV
This parameter is sampled and not 100% tested.						

DC Characteristics

T_a = 0°C to 70°C, V_{CC} = 5V ± 10%

Parameter	Symbol	LIMITS Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}			10	μA	VCC = Max VIN = GND to VCC
Output Leakage Current	I_{LO}			10	μA	VCC = Max, $\overline{CS}$ = VIH VOUT = GND to VCC
Operating Current	I_{CC}			60	mA	VCC = Max, $\overline{CS}$ = VIL Outputs Open
Standby Current	I_{SB}			15	mA	VCC = Min to Max $\overline{CS}$ = VIH
Input Low Voltage	V_{IL}	-1.5		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	IOL = 4mA
Output High Voltage	V_{OH}	2.4			V	IOH = 1mA
Output Short Circuit Current	I_{OS}	TBD		TBD	mA	VOUT = GND to VCC

AC Test Conditions

Input Pulse Levels ..... 0.8V to 2.2V
Input Rise and Fall Times 10nsec
Input Timing Reference Levels 1.5V
Output Timing Reference Levels 1.5V

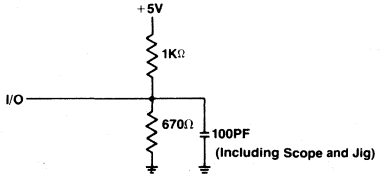


Figure 1 – Output Load

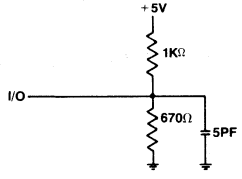


Figure 2 - Transition Load

AC Characteristics

Read Cycle

T_a = 0°C to 70°C, V_{CC} 5V ± 10%

Parameter	Symbol	LIMITS μPD4016-3 Min	Max.	μPD4016-2 Min.	Max.	μPD4016-1 Min.	Max.	Unit	Notes
Read Cycle Time	t_{RC}	150		200		250		nsec	1
Address Access Time	t_{AA}		150		200		250	nsec	
Chip Select Access Time	t_{ACS}		150		200		250	nsec	2
Output Hold from Address Change	t_{OH}	10		10		10		nsec	
Chip Selection to Output in Low Z	t_{LZ}	10		10		10		nsec	3,4
Chip Deselection to Output in High Z	t_{HZ}		50		60		80	nsec	3,4
Output Enable to Output Valid	t_{OE}		70		90		110	nsec	
Output Enable to Output in Low Z	t_{OLZ}	10		10		10		nsec	3,4
Output Disable to Output in High Z	t_{OHZ}		50		60		80	nsec	3,4
Chip Selection to Power up Time	t_{PU}	0		0		0		nsec	4
Chip Deselection to Power down Time	t_{PD}		70		90		110	nsec	4

Write Cycle

T_a = 0°C to 70°C, V_{CC} 5V ± 10%

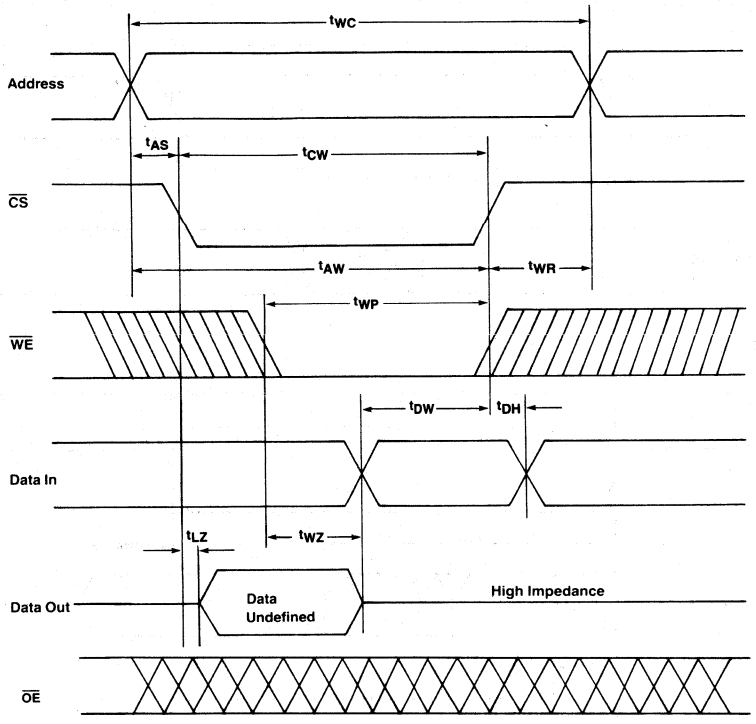
Parameter	Symbol	LIMITS μPD4016-3 Min	Max	μPD4016-2 Min	Max	μPD4016-1 Min	Max.	Unit	Notes
Write Cycle Time	t_{WC}	150		200		250		nsec	
Chip Selection to End of Write	t_{CW}	120		160		200		nsec	
Address Valid to End of Write	t_{AW}	90		120		150		nsec	
Address Setup Time	t_{AS}	0		0		0		nsec	
Write Pulse Width	t_{WP}	80		100		130		nsec	5
Write Recovery Time	t_{WR}	10		10		10		nsec	
Data Valid to End of Write	t_{DW}	50		60		80		nsec	
Data Hold Time	t_{DH}	0		0		0		nsec	
Write Enabled to Output in High-Z	t_{WZ}		50		60		80	nsec	6,7
Output Active from End of Write	t_{OW}	10		10		10		nsec	6,7

Notes:

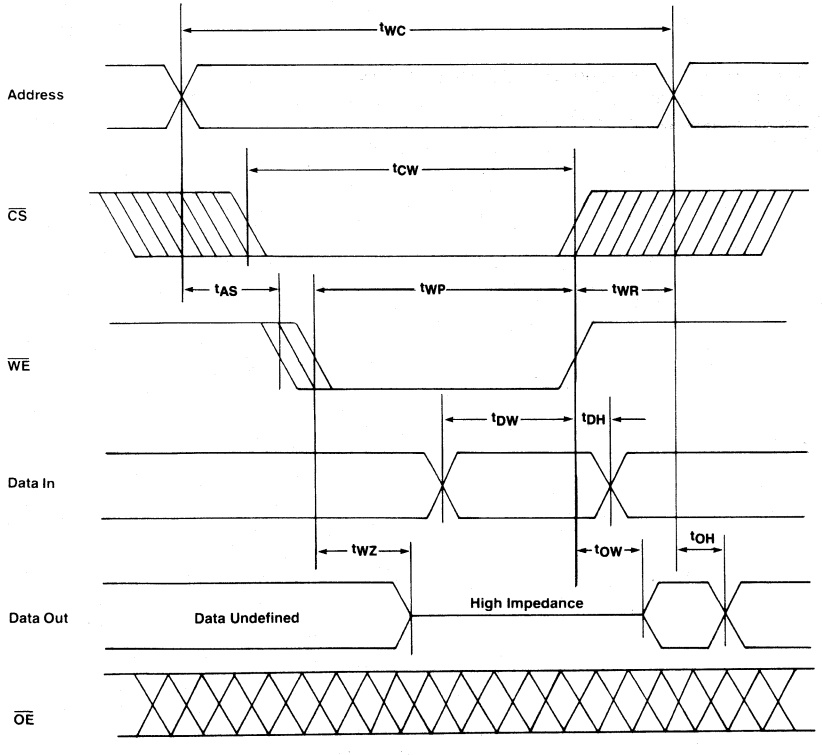
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ± 200mV from steady state voltage with specified load of Figure 1.
4. This parameter is sampled and not 100% tested.
5. If $\overline{CS}$ and $\overline{OE}$ are both low before write enabled, tWP = tWZ + DW
6. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
7. This parameter is sampled and not 100% tested.

Timing Waveforms

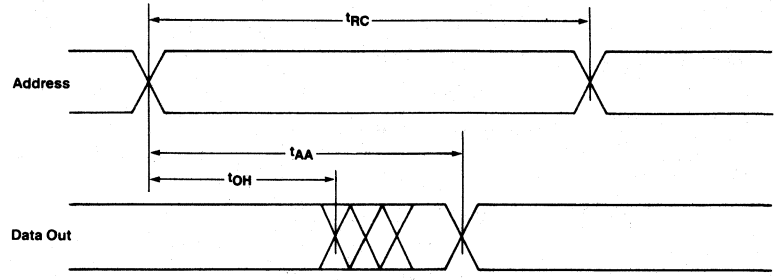
Write Cycle No. 1 ($\overline{WE}$ Controlled)



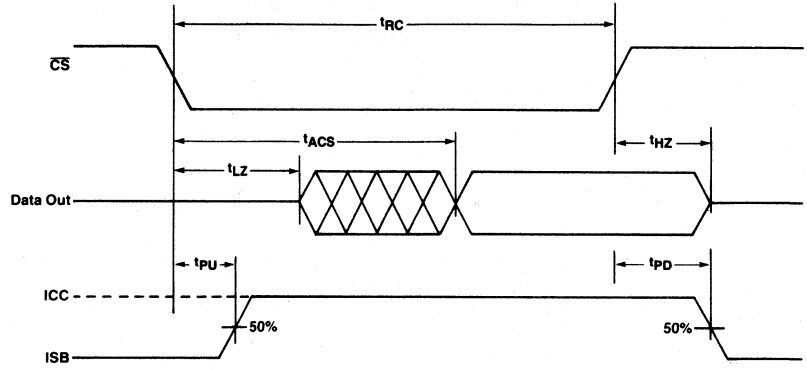
Write Cycle No. 2 ($\overline{CS}$ Controlled)



Read Cycle No. 1 ② ③ ④



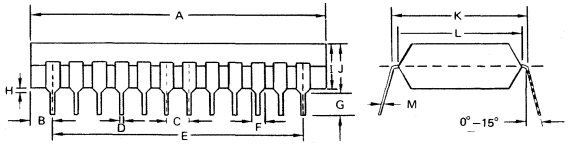
Read Cycle No. 2 ① ② ④



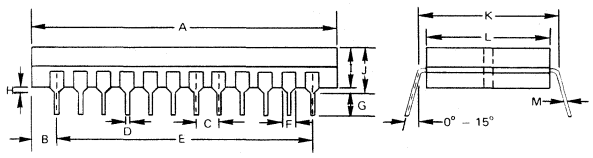
Read Cycle No. 3 ② ③

Notes: ① Address valid prior to or coincident with $\overline{CS}$ transition low.
② $\overline{WE}$ is high for Read Cycles.
③ Device is continuously selected, $\overline{CS}$ = VIL.
④ $\overline{OE}$ = VIL

Package Outlines
μPD4016C



μPD4016D



Plastic

Item	Millimeters	Inches
A	33 Max	1.3 Max
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 Min	0.1 Min
H	0.5 Min	0.02 Min
I	5.22 Max	0.205 Max
J	5.72 Max	0.225 Max
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

Cerdip

Item	Millimeters	Inches
A	33.5 Max	1.32 Max
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 Min	0.1 Min
H	0.5 Min	0.019 Min
I	4.58 Max	0.181 Max
J	5.08 Max	0.2 Max
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

3

1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION

The μPD5101L and μPD5101L-1 are very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memories. They meet the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

All inputs and outputs of the μPD5101L and μPD5101L-1 are TTL compatible. Two chip enables ($\overline{CE}_1$, CE_2) are provided, with the devices being selected when $\overline{CE}_1$ is low and CE_2 is high. The devices can be placed in standby mode, drawing 10 μA maximum, by driving $\overline{CE}_1$ high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

The μPD5101L and μPD5101L-1 have separate input and output lines. They can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is nondestructively read out. Read mode is selected by placing a high on the R/W pin. Either device is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

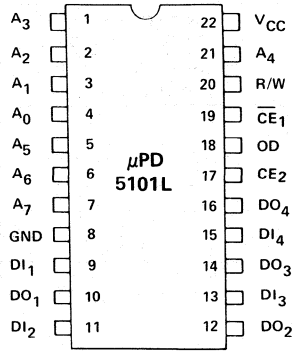
The μPD5101L and μPD5101L-1 are fabricated using NEC's silicon gate complementary MOS (CMOS) process.

3

FEATURES

- Directly TTL Compatible – All Inputs and Outputs
- Three-State Output
- Access Time – 650 ns (μPD5101L); 450 ns (μPD5101L-1)
- Single +5V Power Supply
- CE_2 Controls Unconditional Standby Mode
- For operation at +3V Power Supply, Contact the NEC Sales Office.

PIN CONFIGURATION

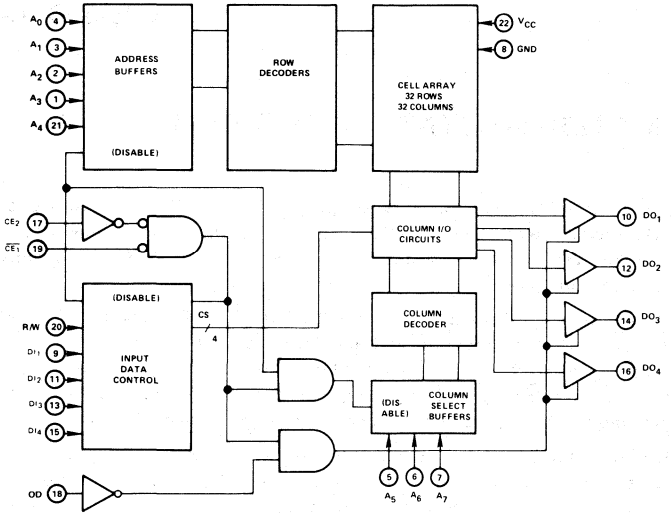


PIN NAMES

$DI_1 - DI_4$	Data Input
$A_0 - A_7$	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$, CE_2	Chip Enables
OD	Output Disable
$DO_1 - DO_4$	Data Output
V_{CC}	Power (+5V)

μPD5101L

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
Voltage On Any Pin With Respect to Ground . . . . . −0.3 Volts to V_{CC} +0.3 Volts
Power Supply Voltage . . . . . −0.3 to +7.0 Volts
T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP (1)	MAX	UNIT	TEST CONDITIONS
Input High Leakage	I_{LIH} (2)			1	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL} (2)			−1	μA	V_{IN} = 0V
Output High Leakage	I_{LOH} (2)			1	μA	$\overline{CE}_1$ = 2.2V, $V_{OUT} = V_{CC}$
Output Low Leakage	I_{LOL} (2)			−1	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.0V
Operating Current	I_{CC1}			22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Operating Current	I_{CC2}			27	mA	V_{IN} = 2.2V Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Standby Current	I_{CCL} (2)			10	μA	V_{IN} = 0 to 5.25V $CE_2 \leq$ 0.2V
Input Low Voltage	V_{IL}	−0.3		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
Output High Voltage	V_{OH2}	3.5			V	I_{OH} = −100 μA

Notes: (1) Typical values at T_a = 25°C and nominal supply voltage.
(2) Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance (All Input Pins)	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0V

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS 5101L MIN	5101L TYP	5101L MAX	5101L-1 MIN	5101L-1 TYP	5101L-1 MAX	UNIT	TEST CONDITIONS
Read Cycle	t_{RC}	650			450			ns	Input pulse amplitude: 0,65 to 2,2 Volts
Access Time	t_A			650			450	ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}			600			400	ns	Timing measurement reference level: 1,5 Volt
Chip Enable (CE_2) to Output	t_{CO2}			700			500	ns	Output load: I_{TTL}
Output Disable to Output	t_{OD}			350			250	ns	Gate and C_L = 100 pF
Data Output to High Z State	t_{DF}	0		150	0		130	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0			0			ns	
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0			0			ns	

WRITE CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS 5101L MIN	5101L TYP	5101L MAX	5101L-1 MIN	5101L-1 TYP	5101L-1 MAX	UNIT	TEST CONDITIONS
Write Cycle	t_{WC}	650			450			ns	Input pulse amplitude: 0,65 to 2,2 Volts
Write Delay	t_{AW}	150			130			ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Write	t_{CW1}	550			350			ns	Timing measurement reference level: 1,5 Volt
Chip Enable (CE_2) to Write	t_{CW2}	550			350			ns	Output load: I_{TTL}
Data Setup	t_{DW}	400			250			ns	Gate and C_L = 100 pF
Data Hold	t_{DH}	100			50			ns	
Write Pulse	t_{WP}	400			250			ns	
Write Recovery	t_{WR}	50			50			ns	
Output Disable Setup	t_{DS}	150			130				

LOW V_{CC} DATA RETENTION CHARACTERISTICS

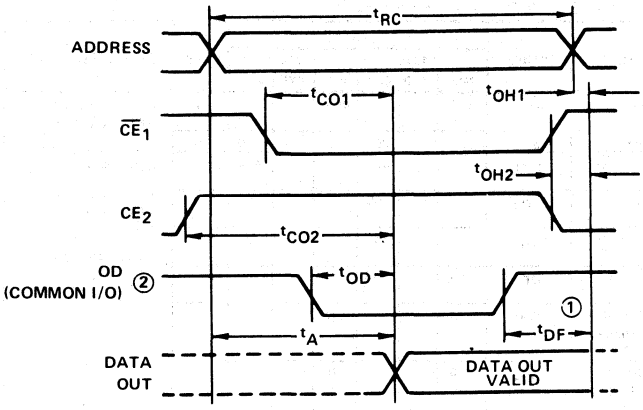
T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leq +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	V_{CCDR} = +2.0V $CE_2 \leq +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC}①			ns	

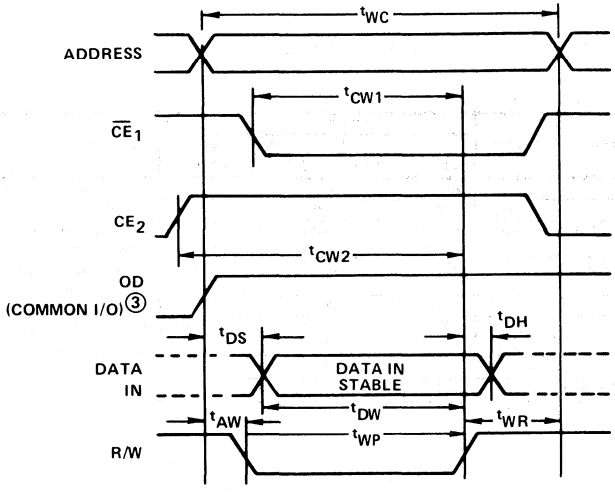
Note: ① t_{RC} = Read Cycle Time

TIMING WAVEFORMS

READ CYCLE

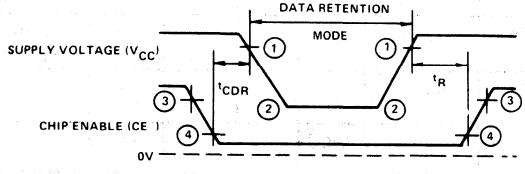


WRITE CYCLE



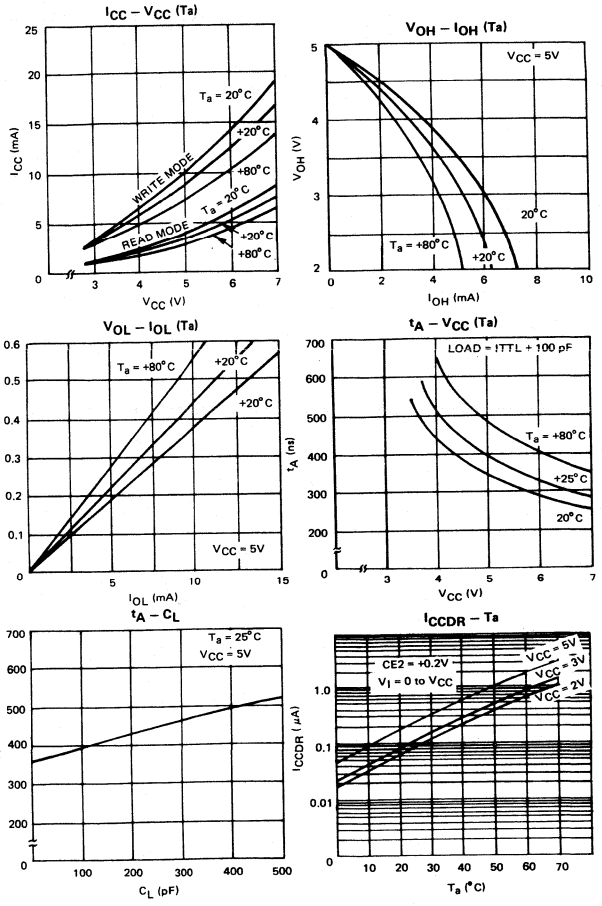
Notes: ① Typical values are for T_a = 25°C and nominal supply voltage.
② OD may be tied low for separate I/O operation.
③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

LOW V_{CC} DATA RETENTION

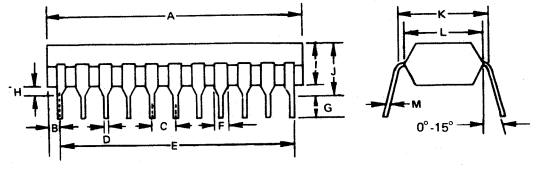


Notes: ① 4.75V
② V_{CCDR}
③ V_{IH}
④ 0.2V

TYPICAL OPERATING CHARACTERISTICS



PACKAGE OUTLINE μPD5101LC



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 0.10	0.02 0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

5101LDS-REV1-12-81-CAT

1024 x 4-BIT STATIC CMOS RAM

DESCRIPTION

The μPD444 is a high-speed, low power silicon gate CMOS 4096 bit static RAM organized 1024 words by 4 bits. It uses DC stable (static) circuitry throughout and therefore requires no clock or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out non-destructively and has the same polarity as the input data. Common input/output pins are provided.

$\overline{CS}$ controls the power down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the μPD444 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ is high. There is no minimum $\overline{CS}$ high time for device operation, although it will determine the length of time in the power down mode. When $\overline{CS}$ goes low, selecting the μPD444, the μPD444 automatically powers up.

The μPD444 is placed in an 18-pin plastic package for the highest possible density. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The μPD444 is pin-compatible with the μPD2114L NMOS Static RAM.

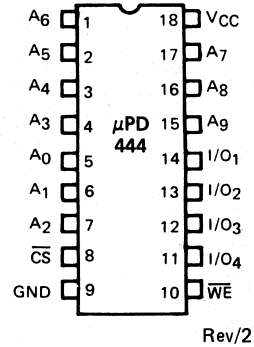
Data retention is guaranteed to 2 volts on all parts. These devices are ideally suited for low power applications where battery operation or battery backup for non-volatility is required.

3

FEATURES

- Low Power Standby — 1 μA Typ.
- Low Power Operation
- Data Retention — 2.0V Min.
- Capability of Battery Backup Operation
- Fast Access Time — 200-450 ns
- Identical Cycle and Access Times
- Single +5V Supply
- No Clock or Timing Strobe Required
- Completely Static Memory
- Automatic Power-Down
- Directly TTL compatible: All Inputs and Outputs
- Common Data Input and Output using Three-State Outputs
- Available in a Standard 18-Pin Plastic Package
- For Operation at +3V Power Supply, Contact the NEC Sales Office.

PIN CONFIGURATION

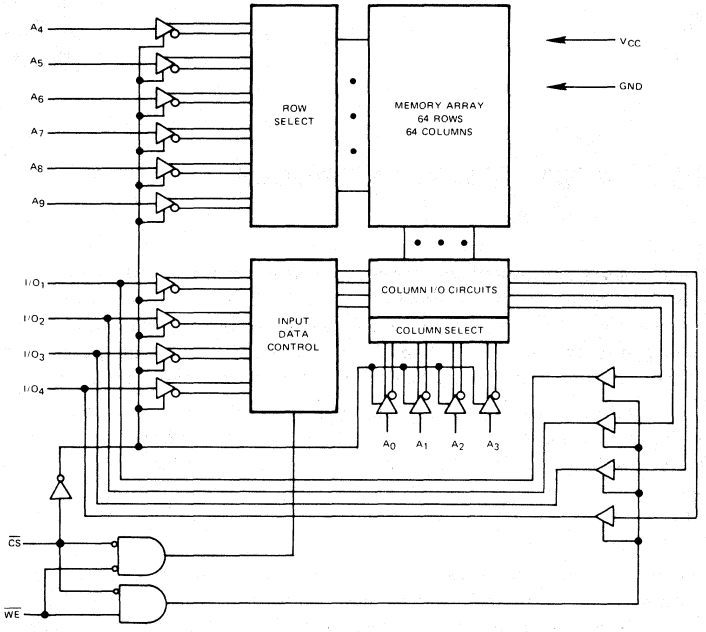


PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

Rev/2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −40°C to +85°C
Storage Temperature . . . . . −55°C to +125°C
All Input and Output Voltages . . . . . −0.3 to V_{CC} +0.3 Volts ①
Supply Voltage . . . . . +8.0 Volts

Note: ① With Respect to Ground

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −40°C to +85°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS 444-3 MIN	444-3 TYP	444-3 MAX	444-2 MIN	444-2 TYP	444-2 MAX	444-1 MIN	444-1 TYP	444-1 MAX	444 MIN	444 TYP	444 MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}	−1.0		1.0	−1.0		1.0	−1.0		1.0	−1.0		1.0	μA	V_{IN} = GND to V_{CC}
I/O Leakage Current	I_{LO}	−1.0		1.0	−1.0		1.0	−1.0		1.0	−1.0		1.0	μA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}
Operating Supply Current	I_{CCA1}		19	35		15	35		12	35		9	35	mA	$\overline{CS}$ = V_{IL}, V_{IN} = V_{CC}, Outputs Open
Operating Supply Current	I_{CCA2}		23	70		19	40		15	40		12	40	mA	$\overline{CS}$ = V_{IL}, V_{IN} = 2.4V, Outputs Open
Average Operating Supply Current	I_{CCA3}		10	20		9	20		8	20		7	20	mA	V_{IN} = GND or V_{CC}, Outputs Open f = 1 MHz, Duty 50%
Standby Supply Current	I_{CCS}		1	5		1	5		1	5		1	50	μA	$\overline{CS}$ = V_{CC}, V_{IN} = GND to V_{CC}
Input Low Voltage	V_{IL}	−0.3		0.8	−0.3		0.8	−0.3		0.8	−0.3		0.8	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	2.4		V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}			0.4			0.4			0.4			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			2.4			2.4			2.4			V	I_{OH} = −1.0 mA

CAPACITANCE

T_a = 25°C, f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input/Output Capacitance	$C_{I/O}$			10	pF	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V

Note: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

T_a = −40°C to +85°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS 444-3 MIN	444-3 MAX	444-2 MIN	444-2 MAX	444-1 MIN	444-1 MAX	444 MIN	444 MAX	UNIT	TEST CONDITIONS
READ CYCLE											
Read Cycle	t_{RC}	200		250		300		450		ns	Input Pulse Levels: +0.8 to +2.4 Volts
Address Access Time	t_{AA}		200		250		300		450	ns	Input Rise and Fall Times: 10 ns
Chip Select Access Time ①	t_{ACS1}		200		250		300		450	ns	Input and Output Timing Levels: 1.5 Volt
Chip Select Access Time ②	t_{ACS2}		250		300		350		500	ns	Output Load: 1 TTL
Output Hold from Address Change	t_{OH}	50		50		50		50		ns	Gate and C_L = 100 pF
Chip Selection to Output in Low Z	t_{LZ}	20		20		20		20		ns	
Chip Deselection to Output in High Z	t_{HZ}		60		70		80		100	ns	
WRITE CYCLE											
Write Cycle Time	t_{WC}	200		250		300		450		ns	Input Pulse Levels: +0.8 to +2.4 Volts
Chip Selection to End of Write	t_{CW}	180		230		250		350		ns	Input Rise and Fall Times: 10 ns
Address Valid to End of Write	t_{AW}	180		230		250		350		ns	Input and Output Timing Levels: 1.5 Volt
Address Setup Time	t_{AS}	0		0		0		0		ns	Output Load: 1 TTL
Write Pulse Width	t_{WP}	180		210		230		300		ns	Gate and C_L = 100 pF
Write Recovery Time	t_{WR}	0		0		0		0		ns	
Data Valid to End of Write	t_{DW}	120		140		150		200		ns	
Data Hold Time	t_{DH}	0		0		0		0		ns	
Write Enabled to Output in High Z	t_{WZ}		60		70		80		100	ns	
Output Active from End of Write	t_{OW}	0		0		0		0		ns	

Notes: ① Chip deselected for greater than 100 ns prior to selection.

② Chip deselected for a finite time that is less than 100 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)

LOW V_{CC} DATA RETENTION CHARACTERISTICS

T_a = −40°C to +85°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Data Retention Supply Voltage	V_{CCDR}	2.0			V	$\overline{CS}$ = V_{CC}, V_{IN} = V_{CC} to GND
Data Retention Supply Current	I_{CCDR}		0.01	②	μA	V_{CC} = 3V, $\overline{CS}$ = V_{CC} V_{IN} = V_{CC} to GND
Chip Deselect to Data Retention Time	t_{CDR}	0			ns	
Operation Recovery Time	t_R	t_{RC} ①			ns	

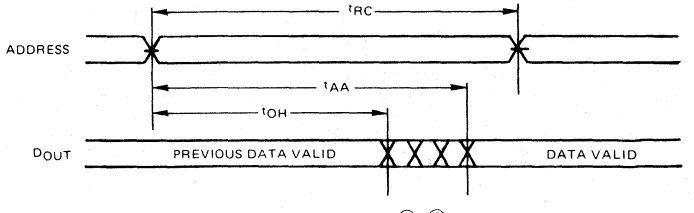
Notes: ① t_{RC} = Read Cycle Time

② 444-1, -2, -3: Value is 2 μA

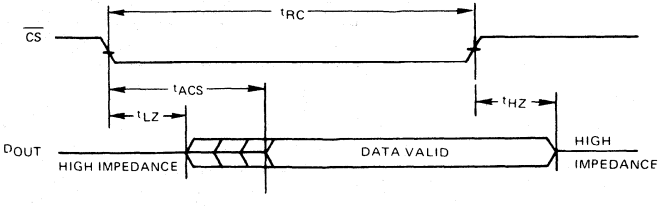
444 Value is 10 μA

TIMING WAVEFORMS

READ CYCLE ① ②

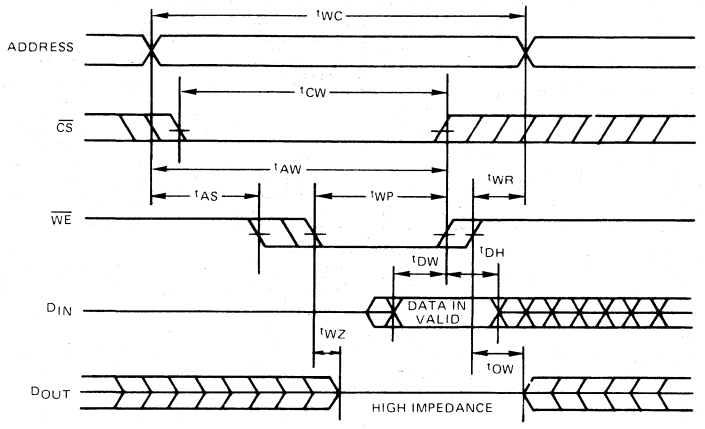


READ CYCLE ① ③



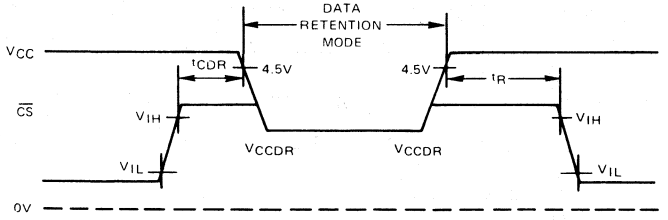
3

WRITE CYCLE ④ ⑤ ⑥

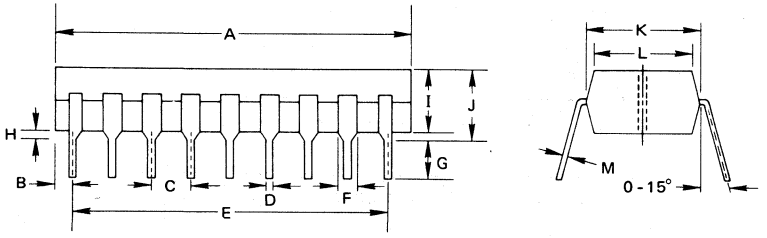


Notes: ① $\overline{WE}$ is high for Read Cycles.
② Device is continuously selected, $\overline{CS}$ = V_{IL}
③ Address valid prior to or coincident with $\overline{CS}$ transition low.
④ If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
⑤ $\overline{WE}$ must be high during all address transitions.
⑥ t_{WP} is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

LOW V_{CC} DATA RETENTION



PACKAGE OUTLINE
μPD444C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

2048 × 8-BIT STATIC CMOS RAM

DESCRIPTION

The μPD446 is a high speed, low power, 2048 word by 8 bit static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD446 a very low operating power device which requires no clock or refreshing to operate. Minimum standby power current is drawn by this device when $\overline{CS}$ equals V_{CC} independently of the other input levels.

Data retention is guaranteed at a power supply voltage as low as 2V.

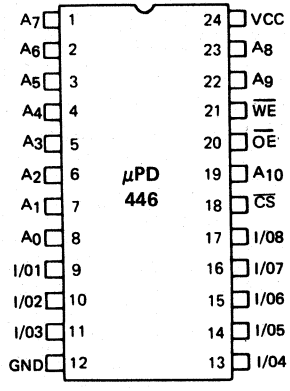
The μPD446 is packaged in a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

3

FEATURES

- Single +5V Supply
- Fully Static Operation – No Clock or Refreshing required
- TTL Compatible – All Inputs and Outputs
- Common I/O Using Three-State Output
- $\overline{OE}$ Eliminates Need for External Bus Buffers
- Max Access/Min Cycle Times Down to 150 ns
- Low power Dissipation, 18 mA Max Active/10 μA Max Standby/ 10 μA Max Data Retention
- Data Retention Voltage – 2V Min
- Standard 24-Pin Plastic and Ceramic Packages
- Plug-in Compatible with 16K EPROMs
- Operating Temperature Range – −40°C to +85°C

PIN CONFIGURATION



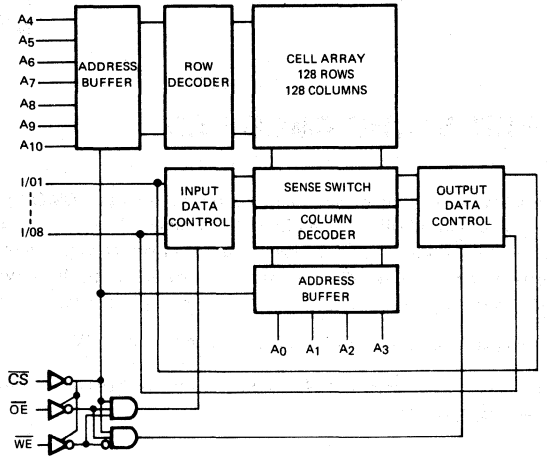
PIN NAMES

A_0-A_{10}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1-I/O8	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	ICC
H	X	X	NOT SELECTED	HZ	STANDBY
L	H	H	NOT SELECTED	HZ	ACTIVE
L	L	H	READ	D_{OUT}	ACTIVE
L	X	L	WRITE	D_{IN}	ACTIVE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	7.0V
Input or Output Voltage Supplied	−0.3 to V_{CC} + 0.3V
Storage Temperature Range	−55°C to 125°C
Operating Temperature Range	−40°C to +85°C

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −40°C to +85°C, V_{CC} = 5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	CONDITIONS
Input High Voltage	V_{IH}	2.2		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}	−1.0		1.0	μA	V_{IN} = 0 ~ V_{CC}
I/O Leakage Current	I_{LO}	−1.0		1.0	μA	V_{CS} = V_{IH} VI/O = 0 ~ V_{CC}
Operating Supply Current	I_{CCA1}		①	①	mA	V_{CS} = V_{IL} $I_{I/O}$ = 0 MIN TCYCLE
	I_{CCA2}		5	10	mA	V_{CS} = V_{IL} $I_{I/O}$ = 0 DC CURRENT
	I_{CCA3}		30	100	μA	V_{CS} = 0.2V $I_{I/O}$ = 0 V_{IN} = V_{CC} −0.2 OR 0.2V
Standby Current	I_{CCS}			10	μA	V_{CS} = V_{CC} −0.2 V_{IN} = 0 − V_{CC}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −1.0 mA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA

NOTE: ① μPD446: 12 mA TYP, 18 mA MAX
μPD446-1: 18 mA TYP, 26 mA MAX
μPD446-2: 20 mA TYP, 30 mA MAX
μPD446-3: 25 mA TYP, 38 mA MAX

CAPACITANCE

T_a = 25°C, f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O}$ = 0V

AC CHARACTERISTICS

READ CYCLE

V_{CC} = 5.0V ± 10%, T_a = −40°C to +85°C

PARAMETER	SYMBOL	LIMITS μPD446-3 MIN	μPD446-3 MAX	μPD446-2 MIN	μPD446-2 MAX	μPD446-1 MIN	μPD446-1 MAX	μPD446 MIN	μPD446 MAX	UNIT
Read Cycle Time	t_{RC}	150		200		250		450		ns
Address Access Time	t_{AA}		150		200		250		450	ns
Chip Select Access Time	t_{ACS}		150		200		250		450	ns
Output Enable to Output Valid	t_{OE}		75		100		120		150	ns
Output Hold from Address Change	t_{OH}	15		15		15		15		ns
Chip Enable to Output in LZ	t_{CLZ}	10		10		10		10		ns
Output Enable to Output in LZ	t_{OLZ}	5		5		5		5		ns
Chip Disable to Output in HZ	t_{CHZ}		50		60		80		100	ns
Output Disable to Output in HZ	t_{OHZ}		50		60		80		100	ns

WRITE CYCLE

V_{CC} = 5.0V ± 10%, T_a = −40°C to +85°C

PARAMETER	SYMBOL	LIMITS μPD446-3 MIN	μPD446-3 MAX	μPD446-2 MIN	μPD446-2 MAX	μPD446-1 MIN	μPD446-1 MAX	μPD446 MIN	μPD446 MAX	UNIT
Write Cycle Time	t_{WC}	150		200		250		450		ns
Chip Enable to End of Write	t_{CW}	120		150		180		210		ns
Address Valid to End of Write	t_{AW}	120		150		180		210		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Write Pulsewidth	t_{WP}	90		120		150		180		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Data Valid to End of Write	t_{DW}	50		60		80		100		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write Enable to Output in HZ	t_{WHZ}		50		60		80		100	ns
Output Active from End of Write	t_{OW}	10		10		10		10		ns

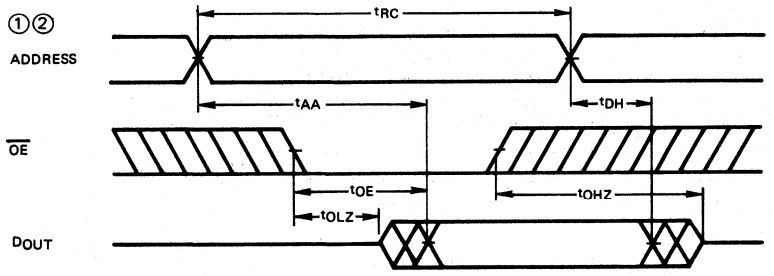
LOW V_{CC} DATA RETENTION

T_a = −40°C to +85°C

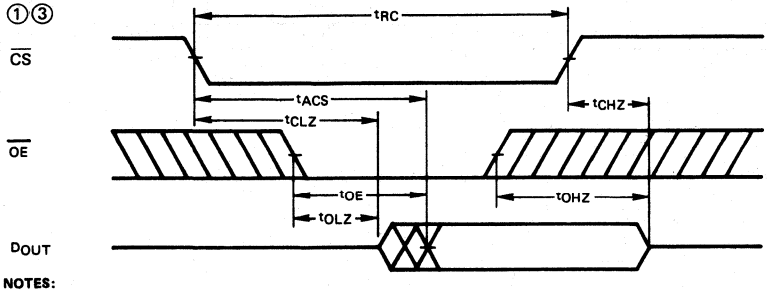
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
VCC for Data Retention	V_{CCDR}	V_{IN} = 0 ~ V_{CC}, $V_{\overline{CS}}$ = V_{CC}	2.0			V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, V_{IN} = 0 ~ V_{CC} $V_{\overline{CS}}$ = V_{CC}		0.01	10	μA
Chip Deselection to Data Retention Time	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

TIMING WAVEFORMS

READ CYCLE (1)



READ CYCLE (2)



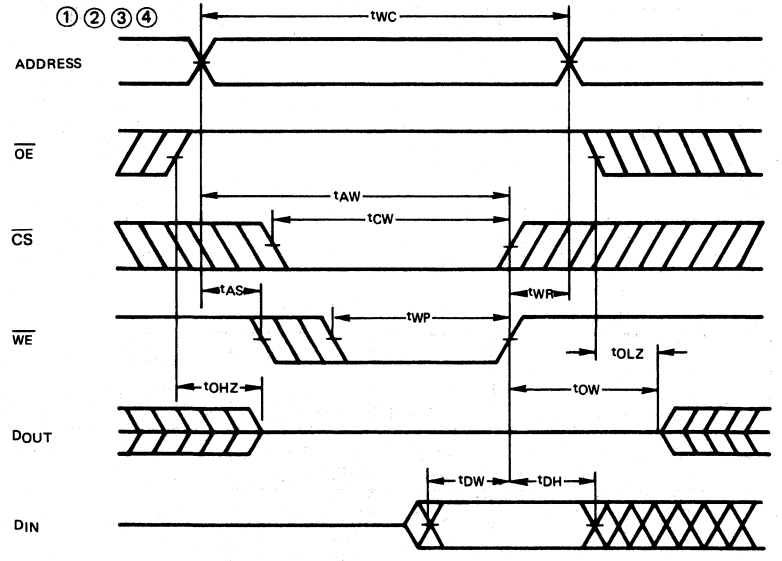
NOTES:

① $\overline{WE}$ is high for read cycles.

② Device is continuously selected, $\overline{CS} = V_{IL}$.

③ Address valid prior to or coincident with $\overline{CS}$ transition low.

WRITE CYCLE (1)



NOTES:

① $\overline{WE}$ must be high during all address transition.

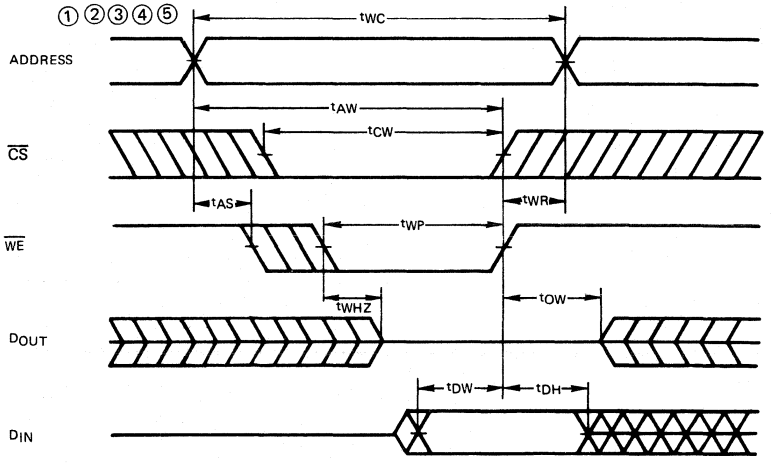
② A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

③ t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

④ If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, output buffers remain in a high impedance state.

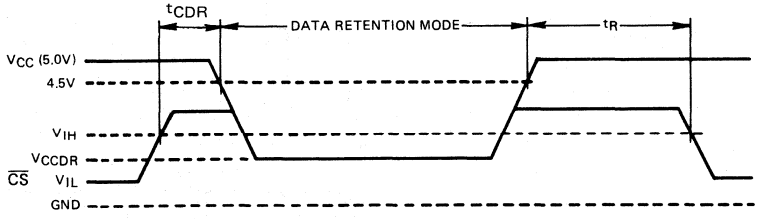
TIMING WAVEFORMS (CONT.)

WRITE CYCLE (2)



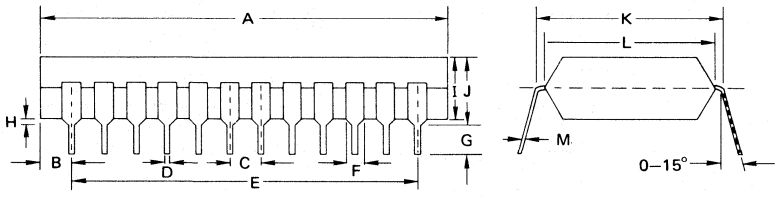
Notes:
① WE must be high during all address transition.
② A write occurs during the overlap of a low CS and a low WE.
③ t_{WR} is measured from the earlier of CS or WE going high to the end of write cycle.
④ If the CS low transition occurs simultaneously with or after the WE low transition, output buffers remain in a high impedance state.
⑤ OE is continuously low (OE – V_{IL}).

LOW V_{CC} DATA RETENTION TIMING CHART



AC TEST CONDITIONS

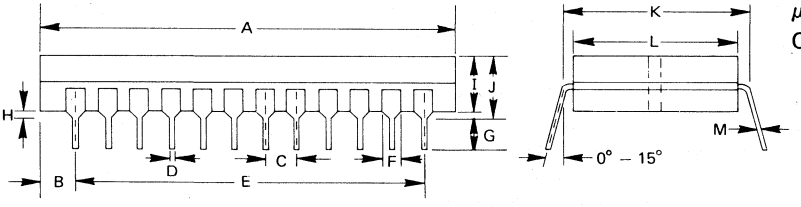
Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL + 100 pF



PACKAGE OUTLINE
μPD446C
PLASTIC

PLASTIC

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD446D
CERDIP

CERDIP

ITEM	MILLIMETERS	INCHES
A	33.5 MAX	1.32 MAX
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.2 MAX
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

2048 × 8-BIT STATIC CMOS RAM

DESCRIPTION

The μPD449 is a high speed, low power, 2048 word by 8-bit static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD449 a very low operating power device which requires no clock or refreshing to operate.

Since the device has two chip enable inputs, it is suited for battery backup applications. Minimum standby power current is drawn by this device when $\overline{CE}1$ or $\overline{CE}2$ equals V_{CC} independently of the other input levels.

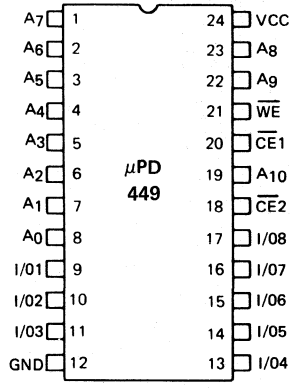
Data Retention is guaranteed at a power supply voltage as low as 2V.

The μPD449 is packaged in a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

FEATURES

- Single +5V Supply
- Fully Static Operation — No Clock or Refreshing required
- TTL Compatible — All Inputs and Outputs
- Common Data Input and Output Using Three-State Output
- Two Chip Enable Inputs for Battery Operation
- Max Access/Min Cycle Times Down to 150 ns
- Low Power Dissipation; 18 mA Max Active/10 μA Max Standby/10 μA Max Data Retention
- Data Retention Voltage — 2V Min
- Standard 24-Pin Plastic and Ceramic Packages
- Plug-in Compatible with 16K EPROMs
- Operating Temperature Range −40°C to +85°C

PIN CONFIGURATION



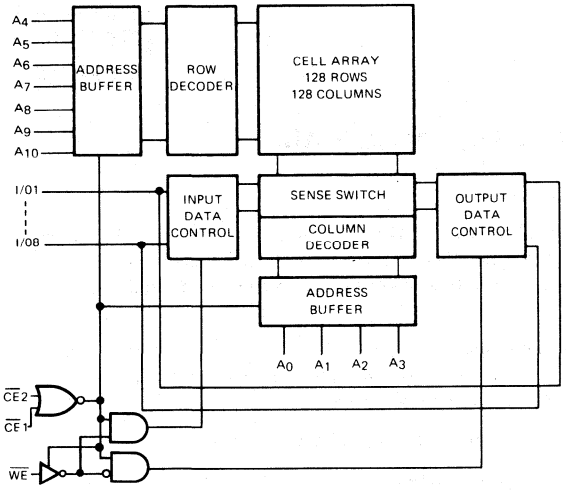
PIN NAMES

A_0-A_{10}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CE}1$-$\overline{CE}2$	Chip Enable Inputs
I/01-I/08	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CE}1$	$\overline{CE}2$	$\overline{WE}$	MODE	I/O	ICC
X	H	X	NOT SELECTED	HZ	STANDBY
H	L	X	NOT SELECTED	HZ	STANDBY
L	L	L	WRITE	D_{IN}	ACTIVE
L	L	H	READ	D_{OUT}	ACTIVE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 7.0V
Input or Output Voltage Supplied . . . . . −0.3 to V_{CC} + 0.3V
Storage Temperature Range . . . . . −55°C to 125°C
Operating Temperature Range . . . . . −40°C to +85°C

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a −40°C to +85°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.2		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}	−1.0		1.0	μA	V_{IN} = 0 ~ V_{CC}
I/O Leakage Current	I_{LO}	−1.0		1.0	μA	$V_{\overline{CE}1}$ or $V_{\overline{CE}2}$ = V_{IH} or V_{WE} = V_{IL} $V_{I/O}$ = 0 ~ V_{CC}
Operating Supply Current	I_{CCA1}		①	①	mA	$V_{\overline{CE}1}$ and $V_{\overline{CE}2}$ = V_{IL} $I_{I/O}$ = 0 MIN TCYCLE
	I_{CCA2}		5	10	mA	$V_{\overline{CE}1}$ and $V_{\overline{CE}2}$ = V_{IL} $I_{I/O}$ = 0 DC CURRENT
	I_{CCA3}		30	10	μA	$V_{\overline{CE}1}$ and $V_{\overline{CE}2}$ = 0.2V V_{IN} = V_{CC} −0.2V or 0.2V $I_{I/O}$ = 0
Standby Current	I_{CCS}			10	μA	$V_{\overline{CE}1}$ or $V_{\overline{CE}2}$ = V_{CC} −0.2V V_{IN} = 0 ~ V_{CC}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −1.0 mA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA

NOTE: ① μPD449: 12 mA TYP, 18 mA MAX
μPD449-1: 18 mA TYP, 26 mA MAX
μPD449-2: 20 mA TYP, 30 mA MAX
μPD449-3: 25 mA TYP, 38 mA MAX

CAPACITANCE

T_a = 25°C, f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O}$ = 0V

AC CHARACTERISTICS

READ CYCLE

V_{CC} = 5.0V ± 10%, T_a = −40°C to +85°C

PARAMETER	SYMBOL	LIMITS μPD449-3 MIN	μPD449-3 MAX	μPD449-2 MIN	μPD449-2 MAX	μPD449-1 MIN	μPD449-1 MAX	μPD449 MIN	μPD449 MAX	UNIT
Read Cycle Time	t_{RC}	150		200		250		450		ns
Access Time	t_A		150		200		250		450	ns
Chip Enable ($\overline{CE}1$) to Output Valid	t_{CO1}		150		200		250		450	ns
Chip Enable ($\overline{CE}2$) to Output Valid	t_{CO2}		150		200		250		450	ns
Output Hold from Address Change	t_{OH}	15		15		15		15		ns
Chip Enable ($\overline{CE}1$) to Output in LZ	t_{LZ1}	5		5		5		5		ns
Chip Enable ($\overline{CE}2$) to Output in LZ	t_{LZ2}	5		5		5		5		ns
Chip Enable ($\overline{CE}1$) to Output in HZ	t_{HZ1}		50		60		80		100	ns
Chip Enable ($\overline{CE}2$) to Output in HZ	t_{HZ2}		50		60		80		100	ns

WRITE CYCLE

V_{CC} = 5.0V ± 10%, T_a = −40°C to +85°C

PARAMETER	SYMBOL	LIMITS μPD449-3 MIN	μPD449-3 MAX	μPD449-2 MIN	μPD449-2 MAX	μPD449-1 MIN	μPD449-1 MAX	μPD449 MIN	μPD449 MAX	UNIT
Write Cycle Time	t_{WC}	150		200		250		450		ns
Chip Enable ($\overline{CE}1$) to End of Write	t_{CW1}	120		150		180		210		ns
Chip Enable ($\overline{CE}2$) to End of Write	t_{CW2}	120		150		180		210		ns
Address Setup Time	t_{AW}	0		0		0		0		ns
Write Pulsewidth	t_{WP}	90		120		150		180		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write Enable to Output in HZ	t_{WZ}		50		60		80		100	ns
Output Active from End of Write	t_{OW}	10		10		10		10		ns
Data Valid to End of Write	t_{DW}	50		60		80		100		ns
Data Hold Time	t_{DH}	0		0		0		0		ns

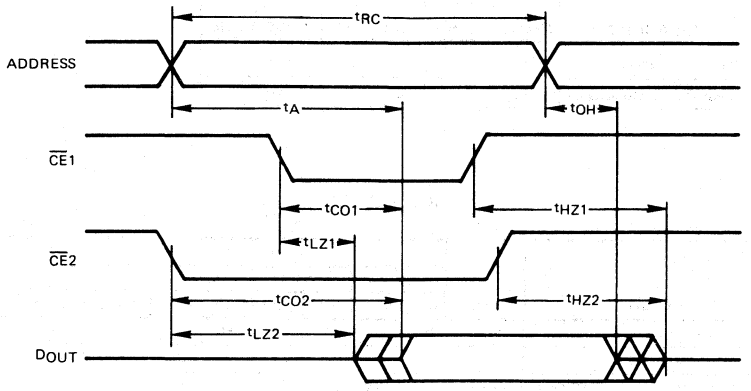
LOW V_{CC} DATA RETENTION

T_a = −40°C to +85°C

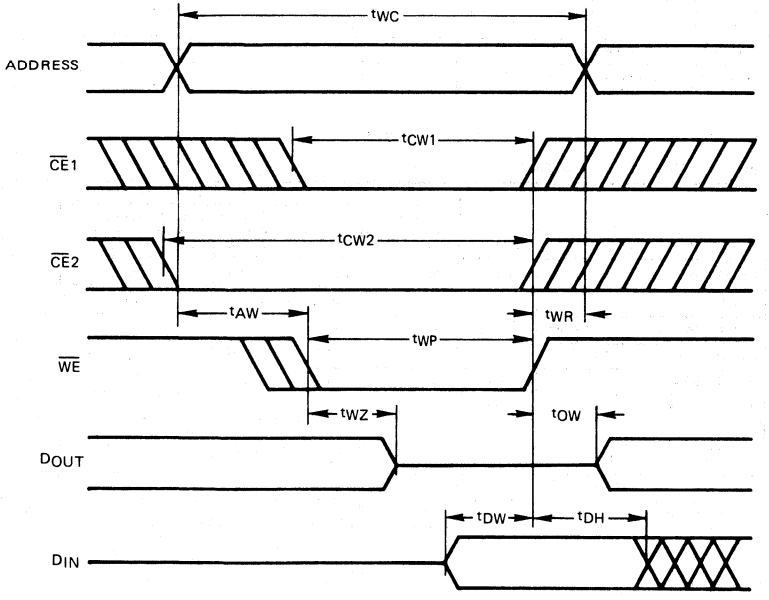
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V_{CC} for Data Retention	V_{CCDR}	V_{IN} = 0 ~ V_{CC}, $V_{\overline{CE}1}$ or $V_{\overline{CE}2}$ = V_{CC}	2.0			V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, V_{IN} = 0 ~ V_{CC} $V_{\overline{CE}1}$ or $V_{\overline{CE}2}$ = V_{CC}		0.01	10	μA
Chip Disable to Data Retention Time	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

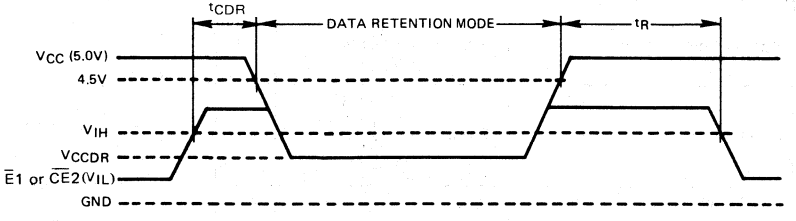
TIMING WAVEFORMS

READ CYCLE TIMING CHART



WRITE CYCLE TIMING CHART





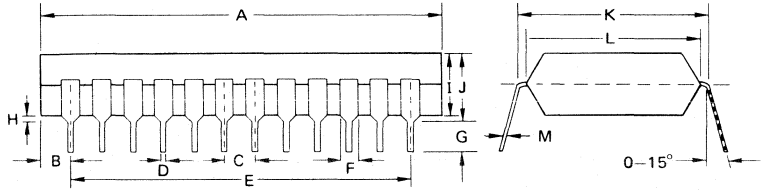
LOW VCC
DATA RETENTION
TIMING CHART

AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL + 100 pF

PACKAGE OUTLINES

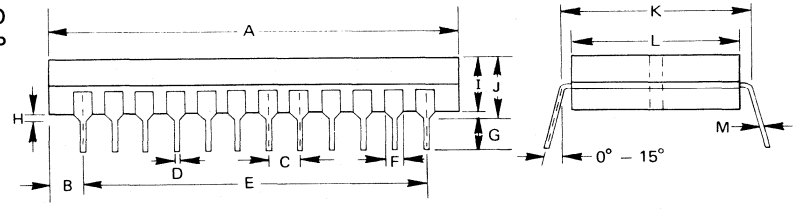
μPD449C PLASTIC



PLASTIC

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD449D CERDIP



CERDIP

ITEM	MILLIMETERS	INCHES
A	33.5 MAX	1.32 MAX
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.2 MAX
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

3

NEC

NEC Electronics U.S.A. Inc.

Microcomputer Division

MEMORIES

FIELD PROGRAMMABLE READ ONLY MEMORIES

4

NEC
NEC Electronics U.S.A. Inc.
Microcomputer Division

μPB406/406-1/406-2
μPB426/426-1/426-2
1024 WORD BY 4-BIT 4096-BIT BIPOLAR TTL PROM

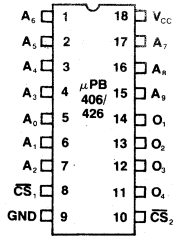
Description

The μPB406 and μPB426 are high-speed, electrically programmable, fully decoded 4096-bit TTL read-only memories. On-chip address decoding, two chip-enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB406 and μPB426 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

- ☐ 1024 word x 4 bit organization (fully decoded)
- ☐ TTL interface
- ☐ Fast Read Access Time: 50 ns max. (μPB406-2, μPB426-2)
- ☐ Power consumption: 500 mW typ.
- ☐ Two Chip Select inputs for memory expansion
- ☐ Open-collector output (μPB406)
  Three-state outputs (μPB426)
- ☐ Ceramic and plastic 18-lead dual in-line packages
- ☐ Fast programming time: 200 μs/bit typ.
- ☐ Compatible with: 7642/7643, 6352/6353 types and equivalent devices (as a ROM)
- ☐ A.I.M. (Avalanche Induced Migration), Shorted-junction technology

Pin Configuration



Pin Names

A_0-A_9	Address Inputs
O_1-O_4	Data Outputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Selects
V_{CC}	Power (+5V)
GND	Ground

Operation

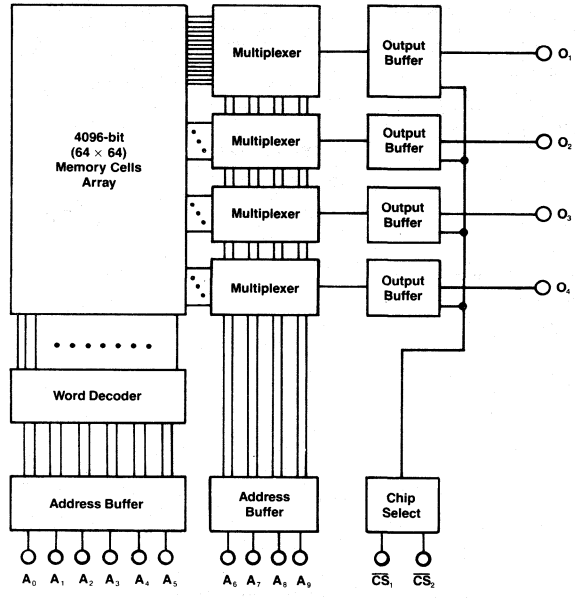
Programming

A logic one can be permanently programmed into a selected bit location by using a programmer. First, the desired word is selected by the ten address inputs in TTL levels. Either or both of the two chip select inputs must be at a logic one (high). Secondly, a train of high-current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then stopped.

Reading

To read the memory, both of the two chip select inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip select inputs are at logic one (high), all the outputs will be high (floating).

Block Diagram



Absolute Maximum Ratings*

T_a = 25° C	
Operating Temperature	−25°C to +75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

μPB406/426

DC Characteristics

T_a = 0°C to +75°C, V_{CC} = 4.50V to 5.50V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IL}			40	μA	V_I = 5.5V, V_{CC} = 5.5 V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V, V_{CC} = 5.5V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA, V_{CC} = 4.5V
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.5V, V_{CC} = 5.5V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O = 0.4V, V_{CC} = 5.5V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −18 mA, V_{CC} = 4.5V
Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = −2.4 mA
Output Short Circuit Current①	$-I_{SC}$	15		60	mA	V_O = 0V

NOTE:
① Applicable to μPB426 only.

Capacitance

T_a = 25°C, f = 1 MHz, V_{CC} = 5.0V, V_{IN} = 2.5V

Characteristics	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}		8	pF
Output Capacitance	C_{OUT}		10	pF

AC Characteristics

T_a = 0°C to +75°C, V_{CC} = 4.50V to 5.50V

Parameter	Symbol	μPB406 μPB426 Min.	Max.	μPB406-1 μPB426-1 Min.	Max.	μPB406-2 μPB426-2 Min.	Max.	Unit	Test Conditions
Address Access Time	t_{AA}		70		60		50	ns	
Chip Select Access Time	t_{ACS}		45		40		30	ns	① ② ③ ④
Chip Select Disable Time	t_{DCS}		45		40		30	ns	

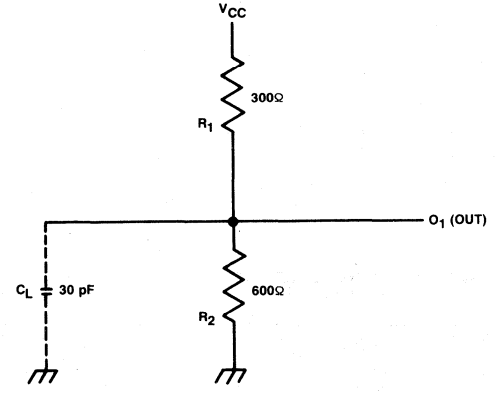


Figure 1

Notes:
① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

Programming Specification

You must rigorously observe this specification in order to program the μPB406 and μPB426 correctly. NEC will not accept responsibility for any device found to be defective if it was not programmed according to this specification.

A typical programming operation is performed by sensing, programming, and sensing again to find out if the word to be programmed has reached the desired state. Either or both of the two chip enable inputs must be at a logic one (high).

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement ensures that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic one (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. The current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process continues until the selected bit is altered to the one state. You can tell that a bit is programmed when two successive sense readings, 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied, and the sense current is terminated.

Characteristic	Limit	Unit	Notes
Ambient Temperature	25 ± 5	°C	
Programming pulse			
Amplitude	200 ± 5%	mA	
Clamp voltage	28 + 0% − 2%	V	
Ramp rate (both in rise and in fall)	70 max.	V/μs	
Pulse width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty cycle	70% min.		
Sense current			
Amplitude	20 ± 0.5	mA	
Clamp voltage	28 + 0% − 2%	V	
Ramp rate	70 max.	V/μs	15V point/ 150Ω load.
Sense current interruption before and after address change	10 min.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum sensed voltage for programmed one	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 min.	μs	

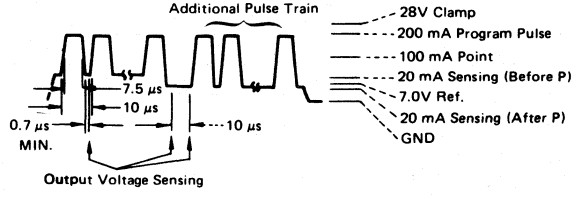
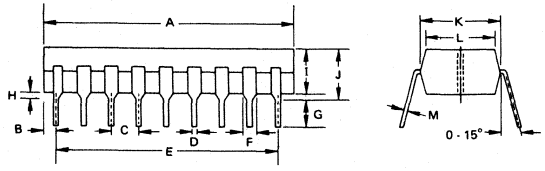


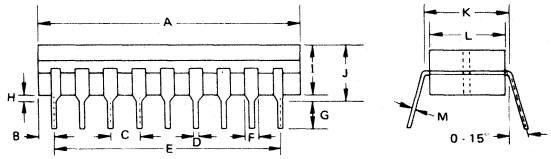
Figure 2 – Typical Output Voltage Waveform

Package Outlines

μPB406/426C PLASTIC



μPB406/426D CERDIP



Plastic

Item	Millimeters	Inches
A	23.2 Max.	0.91 Max.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 Min.	0.1 Min.
H	0.5 Min.	0.02 Min.
I	4.6 Max.	0.18 Max.
J	5.1 Max.	0.2 Max.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

Cerdip

Item	Millimeters	Inches
A	23.2 Max.	0.91 Max.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 Min.	0.1 Min.
H	0.5 Min.	0.02 Min.
I	4.6 Max.	0.18 Max.
J	5.1 Max.	0.2 Max.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

4

Qualified Programming Equipment

Approved Manufacturer	Model No.	Personality Module	Socket Adaptors
Data I/O Issaquah, WA	5, 7, 9, 17, 19	919-1555	715-1305-5
Minato Electronics Tokyo, Japan	1802	μPB4XX	SA-18/B426
Takeda Riken Tokyo, Japan	TR-429 B	PZ 3834	WZ3256-78
Tokyo Data Tokyo, Japan	PECKER-O	UN-711F	AD-7115

2048 WORD BY 8 BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

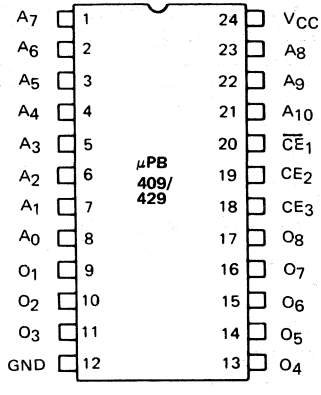
DESCRIPTION

The μPB409 and μPB429 are high-speed, electrically programmable, fully-decoded 16384 bit TTL read only memories. On-chip address decoding, three chip enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB409 and μPB429 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 2048 WORDS x 8 BITS Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time :50 ns MAX
- Medium Power Consumption :500 mW TYP
- Three Chip Enable Inputs for Memory Expansion
- Open-Collector Outputs (μPB409)
- Three-State Outputs (μPB429)
- Ceramic 24-Lead Dual In-Line Package (μPB409D, μPB429D)
- Plastic 24-Lead Dual In-Line Package (μPB409C, μPB429C)
- Fast Programming Time :200 μs/bit TYP
- Replaceable with :82S190/191
  HM76160/76161, 3636
  and Equivalent Type Devices

PIN CONFIGURATION



PIN NAMES

A_0-A_{10}	Address Inputs
CE_1-CE_3	Chip Enable Inputs
O_1-O_8	Data Outputs

μPB409/429

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . -0.5 to +7.0V
Input Voltage . . . . . -0.5 to +5.5V
Output Voltage . . . . . -0.5 to +5.5V
Output Current . . . . . 50 mA
Operating Temperature . . . . . -25°C to +75°C
Storage Temperature
Ceramic Package . . . . . -65°C to +150°C
Plastic Package . . . . . -55°C to +125°C

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 75°C, V_{CC} = 4.5 to 5.5V

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.85	V	
Input High Current	I_{IH}			40	μA	V_I=5.5V, V_{CC}=5.5V
Input Low Current	$-I_{IL}$			0.25	mA	V_I=0.4V, V_{CC}=5.5V
Output Low Voltage	V_{OL}			0.45	V	I_O=16 mA, V_{CC}=4.5V
Output Leakage Current	I_{OFF1}			40	μA	V_O=5.5V, V_{CC}=5.5V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O=0.4V, V_{CC}=5.5V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I=-18 mA, V_{CC}=4.5V
Power Supply Current	I_{CC}		100	160	mA	All inputs Grounded, V_{CC}=5.5V
Output High Voltage*	V_{OH}	2.4			V	I_O=-2.4 mA, V_{CC}=4.5V
Output Short Circuit Current*	$-I_{SC}$	20		70	mA	V_O=0V

*Note: Applicable to μPB429

CAPACITANCE

T_a = 25°C, f = 1 MHz, V_{CC} = 5V, V_{IN} = 2.5V

CHARACTERISTICS	SYMBOL	MIN	MAX	UNIT
Input Capacitance	C_{IN}		8	pF
Output Capacitance	C_{OUT}		10	pF

AC CHARACTERISTICS

T_a = 0°C to 75°C, V_{CC} = 4:5 to 5.5V ①②③④

CHARACTERISTIC	SYMBOL	μPB409-2, μPB429-2		μPB409-1, μPB429-1		μPB409, μPB429		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Access Time	t_{AA}		50		60		70	ns
Chip Enable Access Time	t_{ACE}		30		40		50	ns
Chip Enable Disable Time	t_{DCE}		30		40		50	ns

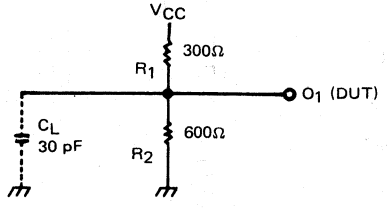


FIGURE 1

NOTES: ① Output Load: See Fig. 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Fig. 1 includes jig and probe stray capacitances.

OPERATION

You can program only when the outputs are disabled by any one of the chip enable inputs. This insures that the output will not be damaged when you apply programming voltages.

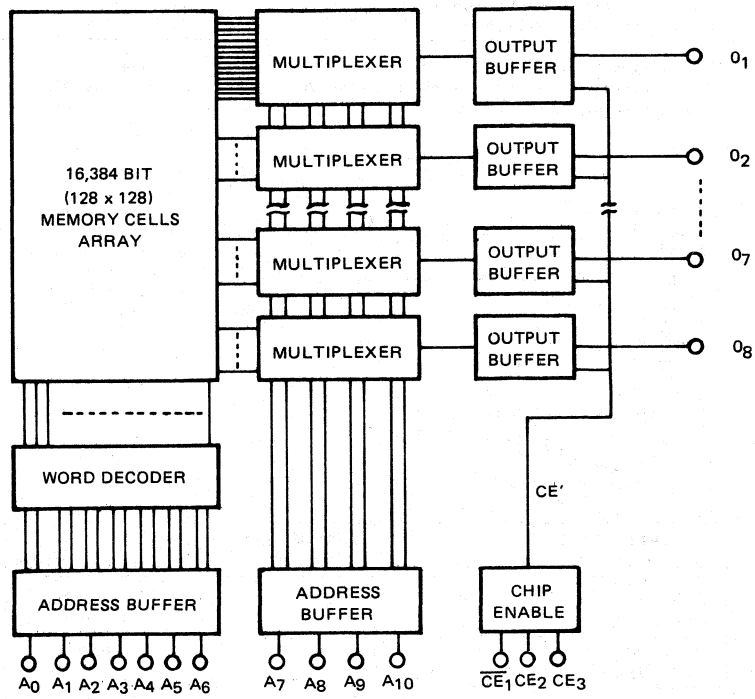
Programming

You can permanently program a logic one into a selected bit location by using special equipment (programmer). First, disable the chip as described above. Second, apply a train of high-current programming pulses to the desired output. Apply an additional pulse train after the sensed voltage indicates that the selected bit is in the logic one state. Then, stop the pulse train.

Reading

To read the memory, enable the chip (i.e., $CE_1 = 0, CE_2 = CE_3 = 1$). The outputs then correspond to the data programmed into the selected words. When the chip is disabled, all the outputs will be in a high impedance (floating) state.

LOGIC DIAGRAM



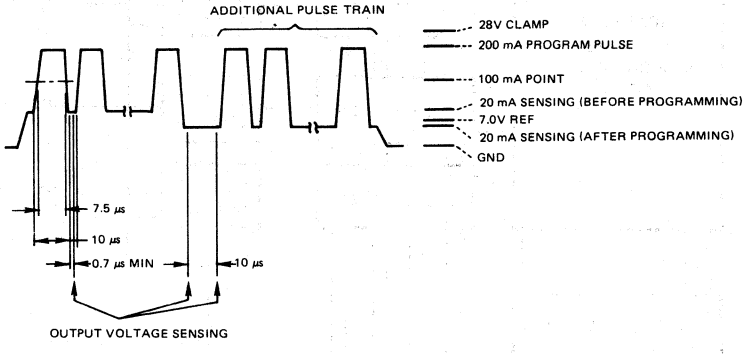
PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB409 and μPB429. NEC will not accept responsibility for any device found to be defective if it was not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% – 2%	V	
Ramp Rate (Both in Rise and in Fall)	70 MAX	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/150Ω load
Duty Cycle	70% MIN		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% – 2%	V	
Ramp Rate	70 MAX	V/μs	15V point/150Ω load
Sense Current Interruption before and after address change	10 MIN	μs	
Programming V_{CC}	5.0 + 5% – 0%	V	
Maximum Sensed Voltage* for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN	μs	

*A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse pass the limit. When this condition has been met, four additional pulses are applied, then the sense current is terminated.

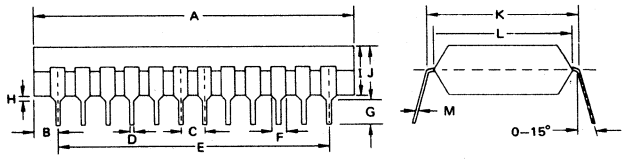
TYPICAL OUTPUT VOLTAGE WAVEFORM



PROGRAMMING EQUIPMENT

APPROVED MANUFACTURER	MODEL NO.	PERSONALITY MODULE	SOCKET ADAPTORS
Data I/O Issaquah, WA	5, 7, 9, 17, 19	919-1555	715-1628-2
Minato Electronics Tokyo, Japan	1802	μPB4XX	SA-24-/B429
Takeda Riken Tokyo, Japan	TR-429 B	PZ 3834	WZ3256-123
Toyo Data Tokyo, Japan	PECKER-O	UN-711F	AD-7118

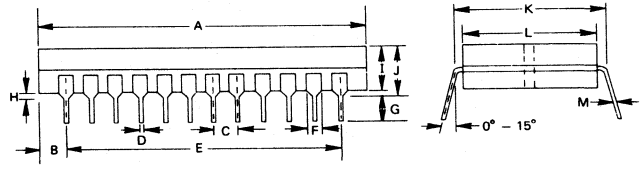
PACKAGE OUTLINE
μPB409C/429C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPB409D/429D



(Cerdip)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX	1.32 MAX
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.6	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.2 MAX
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

4

9216 BIT FIELD PROGRAMMABLE LOGIC ARRAY

DESCRIPTION

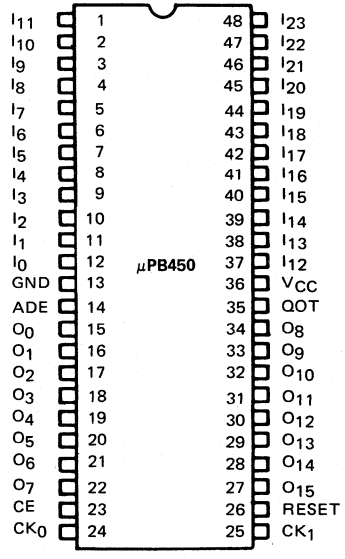
The μPB450 is a bipolar, 9, 216-bit field programmable logic array. It includes 24 input and 16 output lines, 72 product terms, input 2-bit decoders, and 16-bit feedback registers. This provides an extremely versatile organization. Interconnection of internal AND-OR arrays is performed electrically by the proven, avalanche induced migration method which is widely used in NEC Bipolar PROM technology.

FEATURES

- 24 Input Terminals
- 16 Output Terminals with Latches
- 72 Product Terms
- 16 Feedback Loops with J-K Flip Flops
- 20 2704 Input Decoders
- 80 x 72 AND-Array Elements
- 72 x 48 OR-Array Elements
- Scan Path (Shift Register Mode) Capability of J-K Flip Flops
- TTL Compatible
- Single +5V Supply
- 48 Pin Ceramic Dual-In-Line Package

4

PIN CONFIGURATION



PIN NAMES

$I_0 \sim I_{23}$	Input
$O_0 \sim O_{15}$	Outputs
ADE	Mode Control
QOT	Shift Register Output (Mode 2)
CE	Output and Mode Control
CK0	Output Latch Control
CK1	Feed Back Register Clock
RESET	Feed Back Register Reset
V_{CC}	Power Supply (+5V)
GND	Ground

16,384 (2K X 8) BIT UV ERASABLE PROM

DESCRIPTION

The μPD2716 is a 16,384 bit (2048 x 8 bit) Ultraviolet Erasable and Electrically Programmable Read-Only Memory (EPROM). It operates from a single +5 volt supply, making it ideal for microprocessor applications. It offers a standby mode with an attendant 75% savings in power consumption, and is compatible with the μPD2316E as a ROM. This allows for economical change-over to a masked ROM for production quantities, where desired.

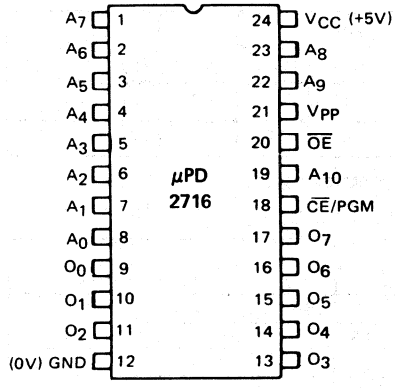
The μPD2716 features fast, simple one pulse programming controlled by TTL level signals. Total programming time for all 16,384 bits is only 100 seconds.

FEATURES

- Ultraviolet Erasable and Electrically Programmable
- Access Time — 390 ns Max
- Single Location Programming
- Programmable with Single Pulse
- Low Power Dissipation Standby Mode
- Input/Output TTL Compatible for Reading and Programming
- Pin Compatible to μPD2316E, μPD446 and μPD4016.
- Single +5V Power Supply
- 24 Pin Ceramic DIP
- Three-State Outputs

4

PIN CONFIGURATION



PIN NAMES

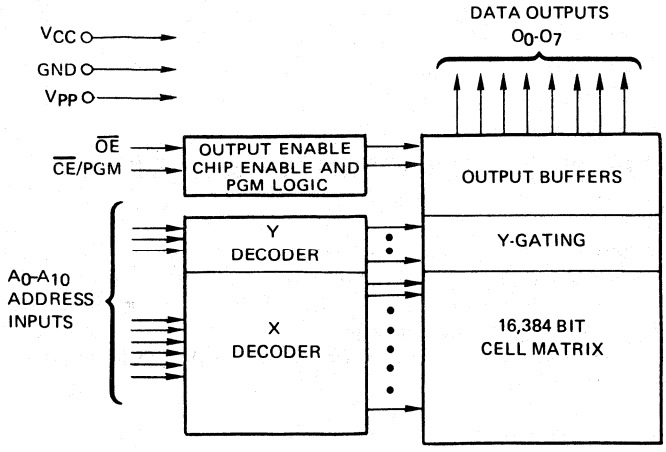
A_0-A_{10}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$/PGM	Chip Enable/Program

TABLE 1. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

V_{IH} and V_{IL} are TTL high level ("1") and TTL low level ("0") respectively.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
Output Voltage . . . . . -0.3 to +6 Volts
Input Voltage . . . . . -0.3 to +6 Volts
Supply Voltage V_{CC} . . . . . -0.3 to +6 Volts
Supply Voltage V_{PP} . . . . . -0.3 to +26.5 Volts

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0V

DC CHARACTERISTICS

READ MODE AND STANDBY MODE

T_a = 0°C ~ 70°C; V_{CC} ① = +5V ± 5%; V_{PP} ①② = V_{CC} ± 0.6V ③

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage	V_{IH}	2.0		V_{cc} +1	V	
Input Low Voltage	V_{IL}	-0.1		0.8	V	
Output Leakage Current	I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current	I_{IL}			10	μA	V_{IN} = 5.25V
V_{PP} Current	I_{PP1}			5	mA	V_{PP} = 5.85V
V_{CC} Current ②	I_{CC1}		10	25	mA	$\overline{CE}$/PGM = V_{IH} $\overline{OE}$ = V_{IL} Standby Mode
	I_{CC2}		57	100	mA	$\overline{CE}$/PGM = V_{IL} $\overline{OE}$ = V_{IL} Read Mode

Notes: ① V_{CC} must be applied simultaneously or before V_{PP} and removed after V_{PP}.

② V_{PP} may be connected directly to V_{CC} (+5V) at read mode and standby mode. The supply current would then be the sum of I_{PP1} and I_{CC} (I_{CC1} or I_{CC2}).

③ The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from +25V to +5V.

DC CHARACTERISTICS (CONT.)

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} ① = +5V ± 5%; V_{PP} ①④ = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0		V_{cc} +1	V	
Input Low Voltage	V_{IL}	-0.1		0,8	V	
Input Leakage Current	I_{IL}			10	μA	V_{IN} = 5.25V/0.45V
V_{PP} Current	I_{PP1}			5	mA	$\overline{CE}/PGM = V_{IL}$ Program Verify / Program Inhibit
	I_{PP2}			30	mA	$\overline{CE}/PGM = V_{IH}$ Program Mode
V_{CC} Current	I_{CC}			100	mA	

AC CHARACTERISTICS

READ MODE AND STANDBY MODE

T_a = 0°C to +70°C; V_{CC} ① = +5V ± 5%; V_{PP} ①② = V_{CC} ± 0.6V ③

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay	t_{ACC}			⑤	ns	$\overline{CE}/PGM = \overline{OE} = V_{IL}$
$\overline{CE}/PGM$ to Output Delay	t_{CE}			⑤	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}/PGM = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		100	ns	$\overline{CE}/PGM = V_{IL}$
Address to Output Hold	t_{OH}	0			ns	$\overline{CE}/PGM = \overline{OE} = V_{IL}$

Test Conditions
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.8 to 2.2V
Timing Measurement Reference Level:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} ① = +5V ± 5%; V_{PP} ①④ = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		120	ns	$\overline{CE}/PGM = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}/PGM = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	5			ns	
Program Pulse Fall Time	t_{PFT}	5			ns	

Test Conditions:
Input Pulse Levels . . . . . 0.8V to 2.2V
Input Timing Reference Level. . . . . 1V and 2V
Output Timing Reference Level . . .0.8V and 2V

Notes: ① V_{CC} must be applied simultaneously or before V_{PP} and removed after V_{PP}.

② V_{PP} may be connected directly to V_{CC} (+5V) at read mode and standby mode. The supply current would then be the sum of I_{PP1} and I_{CC} (I_{CC1} or I_{CC2}).

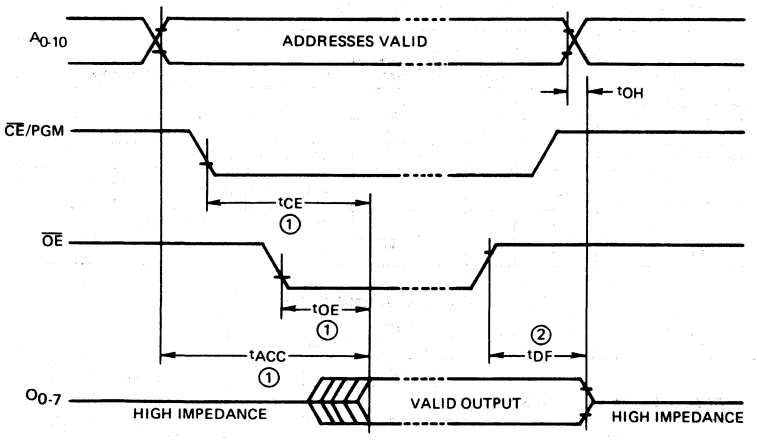
③ The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from +25V to +5V.

④ During programming, program inhibit, and program verify, a maximum of +26V should be applied to the V_{PP} pin. Overshoot voltages to be generated by the V_{PP} power supply should be limited to less than +26V.

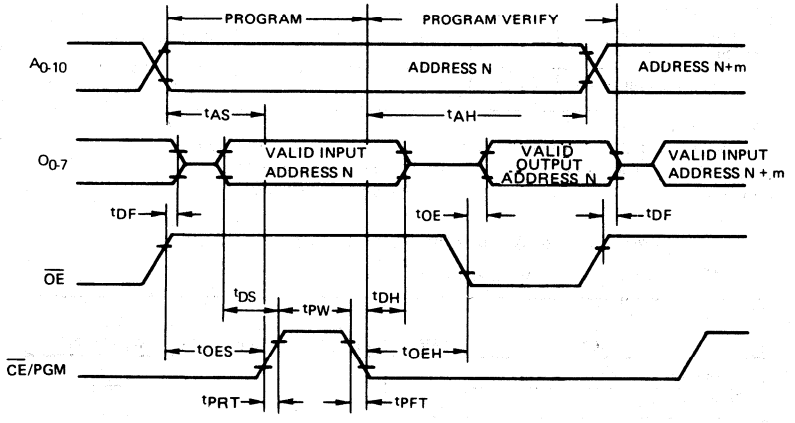
⑤ μPD2716 450 ns
μPD2716-2 390 ns

TIMING WAVEFORMS

READ MODE



PROGRAM MODE



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$/PGM for read mode without impact on t_{ACC}

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$/PGM, whichever occurs first.

FUNCTIONAL DESCRIPTION

The μPD2716 operates from a single +5V power supply and, accordingly, is ideal for use with +5V microprocessors such as μPD8085 and μPD8048/8748.

Programming of the μPD2716 is achieved with a single 50 ms TTL pulse. Total programming time for all 16,384 bits is only 100 sec. Due to the simplicity of the programming requirements, devices on boards and in systems may be programmed easily and without any special programmer.

The μPD2716 features a standby mode which reduces the power dissipation from a maximum active power dissipation of 525 mW to a maximum standby power dissipation of 132 mW. This results in a 75% savings with no increase in access time.

Erasure of the μPD2716 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2716. Consequently, if the μPD2716 is to be exposed to these types of lighting conditions for long periods of time, the μPD2716 window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the μPD2716 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15 W-sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000 μW/cm^2 power rating.

During erasure, the μPD2716 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

OPERATION

The five operation modes of the μPD2716 are listed in Table 1. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply should be at +25V during programming, program verification and program inhibit, and it should be at +5V during read and standby. $\overline{CE}$/PGM, $\overline{OE}$ and V_{PP} select the operation mode as shown in Table 1.

READ MODE

When $\overline{CE}$/PGM and $\overline{OE}$ are at low (0) level with V_{PP} at +5V, the READ MODE is set and the data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

STANDBY MODE

The μPD2716 is placed in the standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$/PGM and a V_{PP} of +5V. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced by 75% from 525 mW to 132 mW.

PROGRAMMING MODE

Programming of the μPD2716 is commenced by erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2716 is placed in the programming mode by applying a high (1) level TTL signal to the $\overline{OE}$ with V_{PP} at +25V. The data to be programmed is applied to the output pins 8 bits in parallel at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

When multiple μPD2716s are connected in parallel, except for $\overline{CE}$/PGM, individual μPD2716s can be programmed by applying a high (1) level TTL pulse to the $\overline{CE}$/PGM input of the desired μPD2716 to be programmed.

Programming of multiple μPD2716s in parallel with the same data is easily accomplished. All the alike inputs are tied together and are programmed by applying a high (1) level TTL pulse to the $\overline{CE}$/PGM inputs.

PROGRAMMING INHIBIT MODE

Programming of multiple μPD2716s in parallel with different data is rendered more easily by the program inhibit mode. Except for $\overline{CE}$/PGM, all alike inputs (including $\overline{OE}$) of the parallel μPD2716s may be common. Programming is accomplished by applying a TTL level program pulse to the μPD2716 $\overline{CE}$/PGM input with V_{PP} at +25V. A low level applied to the $\overline{CE}$/PGM of the other μPD2716 will inhibit it from being programmed.

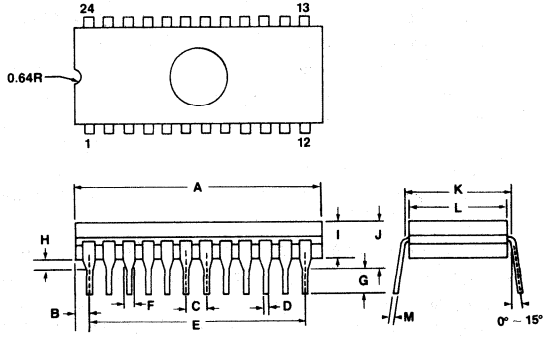
PROGRAM VERIFY MODE

A verify should be performed on the programmed bits to determine that the data was correctly programmed on all bits of the μPD2716. The program verify can be performed with V_{PP} at +25V and $\overline{CE}$/PGM and $\overline{OE}$ at low (0) levels.

OUTPUT DESELECTION

The data outputs of two or more μPD2716s may be wire-ored together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2716s should be deselected by raising the $\overline{OE}$ input to a TTL high.

PACKAGE OUTLINE μPD2716D (CERDIP)



Item	Millimeters	Inches
A	33.5 MAX.	1.32 MAX.
B	2.78	1.1
C	2.54	0.1
D	0.46 · 0.10	0.018 · 0.004
E	27.94	1.10
F	1.3	0.05
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.020
I	5.0 MAX.	0.20
J	5.5 MAX.	0.216
K	15.24	0.60
L	14.66	0.58
M	0.25 · 0.05	0.010 · 0.002

Window Label

An amber-colored window label is provided unattached for the convenience of the user. The window label filters ultra-violet light frequencies, thus preventing accidental erasure or long-term degradation caused by ambient light or sunlight.

μPD2732
μPD2732-4
32,768 (4K × 8) BIT UV ERASABLE PROM

Description

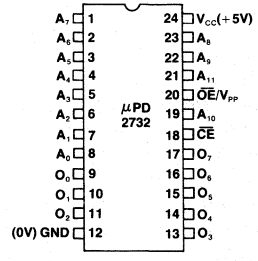
The μPD2732 is a 32,768-bit (4096 x 8 bit) Ultraviolet Erasable and Electrically Programmable Read-Only Memory (EPROM). It operates from a single +5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with an attendant 80% savings in power consumption.

A distinctive feature of the μPD2732 is a separate output control, output enable ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD2732 features fast, simple one-pulse programming controlled by TTL-level signals. Total programming time for all 32,768 bits is only 210 seconds.

Features

- ☐ Ultraviolet erasable and electrically programmable
- ☐ Access time—390 ns max
- ☐ Single location programming
- ☐ Programmable with single pulse
- ☐ Low power dissipation: 150 mA max active current, 30 mA max standby current
- ☐ Input/Output TTL-compatible for reading and programming
- ☐ Single +5V power supply
- ☐ 24-pin ceramic DIP
- ☐ Three-state outputs

Pin Configuration



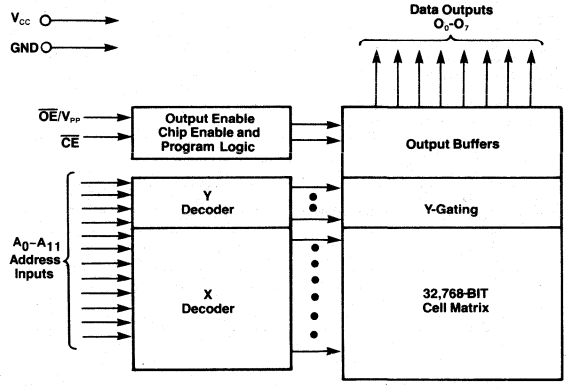
Pin Names

A_0-A_{11}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable

PINS	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	OUTPUTS
MODE				
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Table 1 – Mode Selection

Block Diagram



Absolute Maximum Ratings* (T_a = 25°C)

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.3 to +6 Volts
Input Voltage	−0.3 to +6 Volts
Supply Voltage V_{CC}	−0.3 to +6 Volts
Supply Voltage V_{PP}	−0.3 to +26.5 Volts

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance Except $\overline{OE}/V_{PP}$	C_{IN1}			6	pF	V_{IN} = 0V
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}			30	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			12	pF	V_{OUT} = 0V

DC Characteristics

Read Mode and Standby Mode

T_a = 0°C ~ 70°C; V_{CC} = +5V ± 5%

Parameter		Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage		V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Output Leakage Current		I_{LO}			10	μA	V_{OUT} = 5.25 V
Input Leakage Current	except $\overline{OE}/V_{PP}$	I_{LI1}			10	μA	V_{IN} = 5.25 V
	$\overline{OE}/V_{PP}$	I_{LI2}			10	μA	V_{IN} = 5.25 V
V_{CC} Current	Standby	I_{CC1}		15	30	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}/V_{PP}$ = V_{IL}
	Active	I_{CC2}		85	150	mA	$\overline{OE}/V_{PP}$ = $\overline{CE}$ = V_{IL}

DC Characteristics (Cont.)

Program, Program Verify and Program Inhibit Mode

T_a = 25 ± 5°C, V_{CC} = +5 V ± 5%, V_{PP} = +25 V ± 1 V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC} +1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}		85	150	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE}$ V_{PP}

AC Characteristics

Read Mode and Standby Mode

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address to Output Delay	t_{ACC}			①	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}			①	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		100	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: ① μPD2732 (450 ns max)
μPD2732-4 (390 ns max)

Test Conditions —
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.8 to 2.2V
Timing Measurement Reference Level:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

Program, Program Verify and Program Inhibit Mode

T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{PP} = +25V ± 1V

Parameter	Symbol	Limits Min	Typ	Max	Units	Test Conditions
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		120	ns	
Data Valid from $\overline{CE}$	t_{DV}			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	50			ns	
V_{PP} Recovery Time	t_{VR}	2			μs	

Test Conditions —
Input Pulse Levels = 0.8V to 2.2V
Input Timing Reference Level = 1.0V and 2.0V
Output Timing Reference Level = 0.8V and 2V

Function

The μPD2732 operates from a single +5V power supply, making it ideal for microprocessor applications.

Programming of the μPD2732 is achieved with a single 50 ms TTL pulse. Total programming time for all 32,768 bits is only 210 sec. Due to the simplicity of the programming requirements, devices on boards and in systems may be easily programmed without any special programmer.

The μPD2732 features a standby mode which reduces the power dissipation from a maximum active power dissipation of 788 mW to a maximum standby power dissipation of 158 mW. This results in an 80% savings with no increase in access time.

Erasure of the μPD2732 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2732. Consequently, if the μPD2732 is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the μPD2732 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15 W-sec/cm². The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000 μW/cm² power rating.

During erasure, the μPD2732 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Operation

The five operation modes of the μPD2732 are listed in Table 1. In READ mode, the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for $\overline{OE}/V_{PP}$ which is pulsed from TTL level to 25V.

Read Mode

When $\overline{CE}$ and $\overline{OE}/V_{PP}$ are at low (0) level, READ is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD2732 is placed in standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input. The active power dissipation is reduced by 80% from 788 mW to 158 mW.

Programming

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2732 is placed in programming mode by applying a high (1) level TTL signal to the $\overline{CE}$ and with $\overline{OE}/V_{PP}$ at +25V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

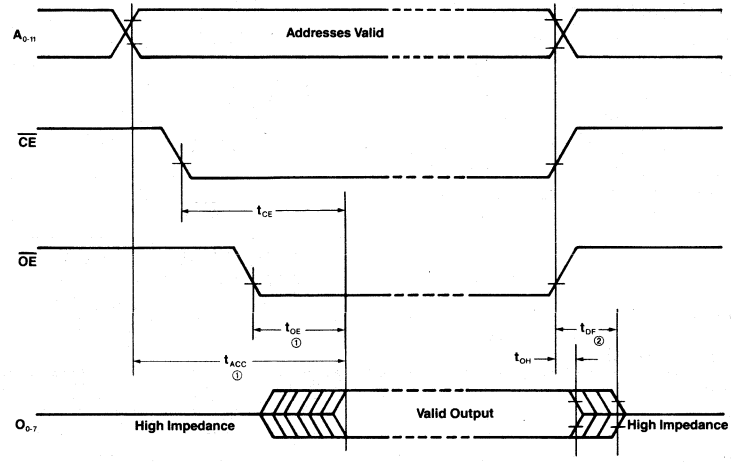
When multiple μPD2732s are connected in parallel, except for $\overline{CE}$, individual μPD2732s can be programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ input of the desired μPD2732 to be programmed.

Programming of multiple μPD2732s in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ inputs.

Programming Inhibit Mode

Programming multiple μPD2732s in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel μPD2732s may be common. Programming is accomplished by applying the TTL-level program pulse to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at +25V. A high (1) level applied to the $\overline{CE}$ of the other μPD2732 will inhibit it from being programmed.

Read Mode



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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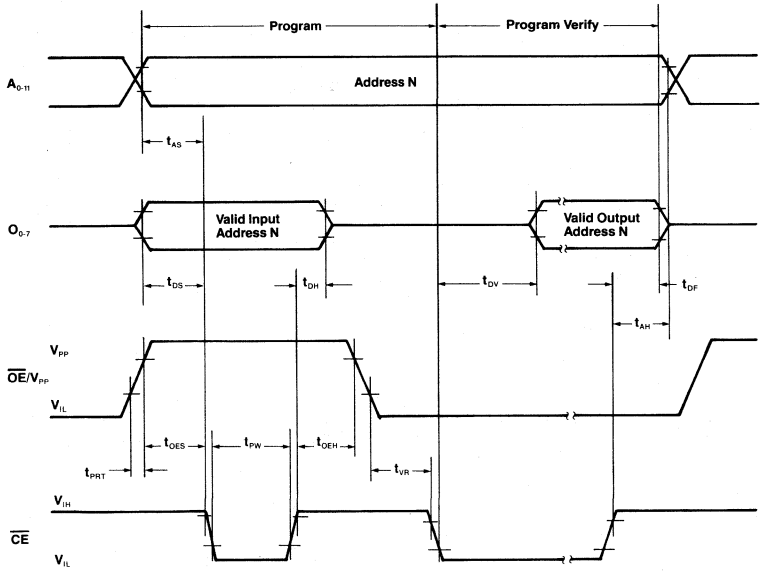
Program Mode ①



Note: ① 0.1μF capacitor must be connected between $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}/V_{PP}$ at low (0) levels.

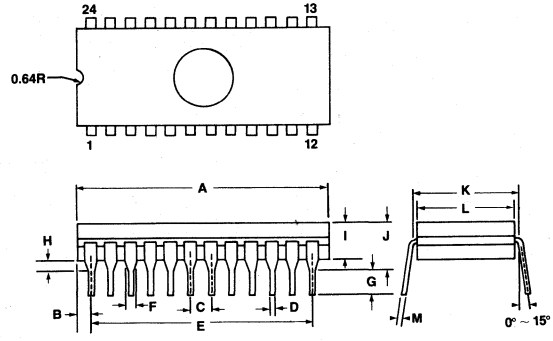
Output Deselect

The data outputs of two or more μPD2732s may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2732s should be deselected by raising the $\overline{OE}/V_{PP}$ input to a TTL high.

Window Label

An amber-colored window label is provided unattached for the convenience of the user. The window label filters ultra-violet light frequencies, thus preventing accidental erasure or long-term degradation caused by ambient light or sunlight.

Package Outline
μPD2732 D (Cerdip)



Item	Millimeters	Inches
A	33.5 MAX.	1.32 MAX.
B	2.78	1.1
C	2.54	0.1
D	0.46 ± 0.10	0.018 ± 0.004
E	27.94	1.10
F	1.3	0.05
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.020
I	5.0 MAX.	0.20
J	5.5 MAX.	0.216
K	15.24	0.60
L	14.66	0.58
M	0.25 ± 0.05	0.010 ± 0.002

PRELIMINARY

μPD2732A
32,768 (4K x 8) BIT UV ERASABLE PROM

Description

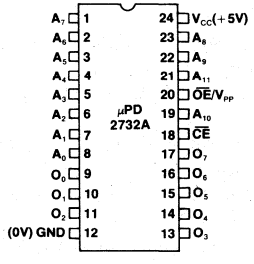
The μPD2732A is a 32,768-bit (4096 x 8 bit) Ultraviolet Erasable and Electrically Programmable Read-Only Memory (EPROM). It operates from a single +5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with an attendant 75% savings in power consumption.

A distinctive feature of the μPD2732A is a separate output control, output enable ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD2732A features fast, simple one-pulse programming controlled by TTL-level signals. Total programming time for all 32,768 bits is only 210 seconds.

Features

- Ultraviolet erasable and electrically programmable
- Access time — 250 ns max
- Single location programming
- Programmable with single pulse
- Low power dissipation: 150 mA max active current, 35 mA max standby current
- Input/Output TTL-compatible for reading and programming
- Single +5V power supply
- 24-pin ceramic DIP
- Three-state outputs

Pin Configuration



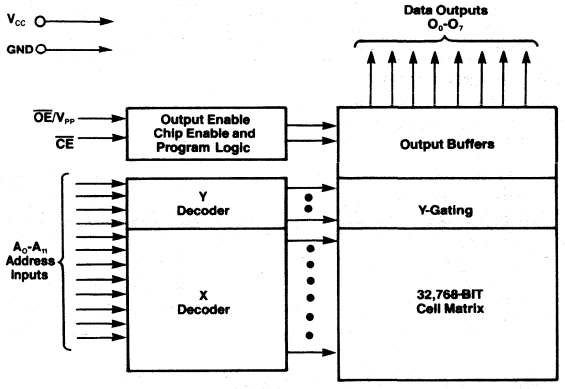
Pin Names

A_0-A_{11}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable

PINS	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	OUTPUTS
MODE				
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Table 1 – Mode Selection

Block Diagram



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Absolute Maximum Ratings* (T_a = 25°C)

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.3 to +6V
Input Voltage	−0.3 to +6V
Supply Voltage V_{CC}	−0.3 to +6V
Supply Voltage V_{PP}	−0.3 to +22V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance Except $\overline{OE}/V_{PP}$	C_{IN1}			6	pF	V_{IN} = 0V
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}			20	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			12	pF	V_{OUT} = 0V

DC Characteristics

Read Mode and Standby Mode

T_a = 0°C ~ 70°C; V_{CC} = +5V ± 5%

Parameter		Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage		V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Output Leakage Current		I_{LO}			10	μA	V_{OUT} = 5.25 V
Input Leakage Current	except $\overline{OE}/V_{PP}$	I_{LI1}			10	μA	V_{IN} = 5.25 V
	$\overline{OE}/V_{PP}$	I_{LI2}			10	μA	V_{IN} = 5.25 V
V_{CC} Current	Standby	I_{CC1}			35	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}/V_{PP}$ = V_{IL}
	Active	I_{CC2}			150	mA	$\overline{OE}/V_{PP}$ = $\overline{CE}$ = V_{IL}

DC Characteristics (Cont.)

Program, Program Verify and Program Inhibit Mode
T_a = 25 ± 5°C, V_{CC} = +5V ± 5%, V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC} +1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -400\,\mu A$
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}		85	150	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$

AC Characteristics

Read Mode and Standby Mode
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address to Output Delay	t_{ACC}			250	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}			250	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}	10		100	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		90	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Test Conditions —
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.8 to 2.2V
Timing Measurement Reference Level:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

Program, Program Verify and Program Inhibit Mode
T_a = 25°C ± 5°C, V_{CC} = +5V ± 5%; V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from $\overline{CE}$	t_{DV}			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	50			ns	
V_{PP} Recovery Time	t_{VR}	2			μs	

Test Conditions —
Input Pulse Levels = 0.8V to 2.2V
Input Timing Reference Level = 1.0V and 2.0V
Output Timing Reference Level = 0.8V and 2V
Input Rise and Fall Times: 20 ns

Function

The μPD2732A operates from a single +5V power supply, making it ideal for microprocessor applications.

Programming of the μPD2732A is achieved with a single 50 ms TTL pulse. Total programming time for all 32,768 bits is only 210 sec. Due to the simplicity of the programming requirements, devices on boards and in systems may be easily programmed without any special programmer.

The μPD2732A features a standby mode which reduces the power dissipation from a maximum active power dissipation of 788 mW to a maximum standby power dissipation of 184 mW. This results in a 75% savings with no increase in access time.

Erasure of the μPD2732A programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2732A. Consequently, if the μPD2732A is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the μPD2732A is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15 W-sec/cm². The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000 μW/cm² power rating.

During erasure, the μPD2732A should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Operation

The five operation modes of the μPD2732A are listed in Table 1. In READ mode, the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for $\overline{OE}/V_{PP}$ which is pulsed from TTL level to 21V.

Read Mode

When $\overline{CE}$ and $\overline{OE}/V_{PP}$ are at low (0) level, READ is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD2732A is placed in standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input. The active power dissipation is reduced by 75% from 788 mW to 184 mW.

Programming

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2732A is placed in programming mode by applying a high (1) level TTL signal to the $\overline{CE}$ and with $\overline{OE}/V_{PP}$ at +21V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

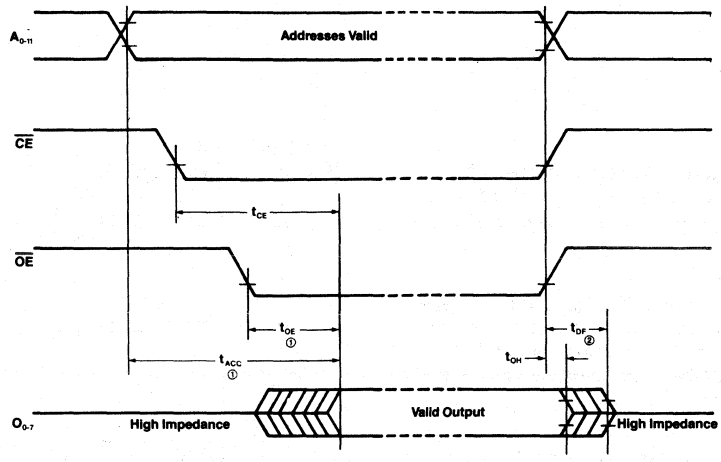
When multiple μPD2732As are connected in parallel, except for $\overline{CE}$, individual μPD2732As can be programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ input of the desired μPD2732A to be programmed.

Programming of multiple μPD2732As in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ inputs.

Programming Inhibit Mode

Programming multiple μPD2732As in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel μPD2732As may be common. Programming is accomplished by applying the TTL-level program pulse to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at +21V. A high (1) level applied to the $\overline{CE}$ of the other μPD2732A will inhibit it from being programmed.

id Mode



otes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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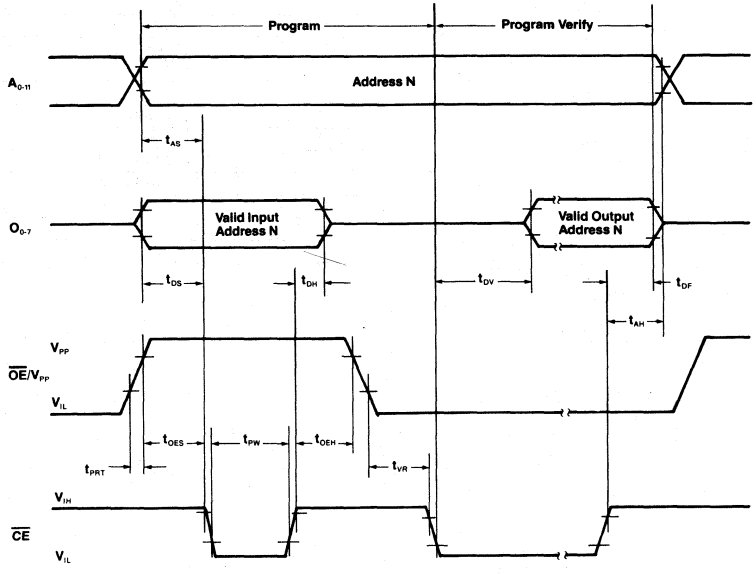
ogram Mode ①



Note: ① 0.1μF capacitor must be connected between $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}/V_{PP}$ at low (0) levels.

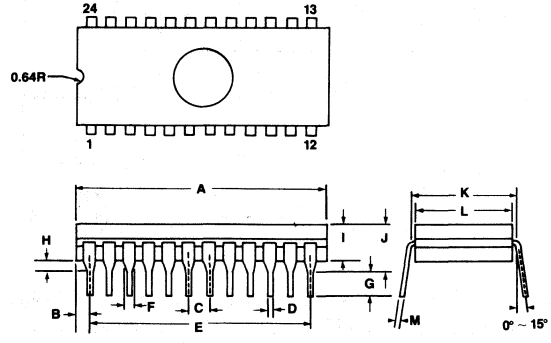
Output Deselect

The data outputs of two or more μPD2732As may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2732As should be deselected by raising the $\overline{OE}/V_{PP}$ input to a TTL high.

Window Label

An amber-colored window label is provided unattached for the convenience of the user. The window label filters ultra-violet light frequencies, thus preventing accidental erasure or long-term degradation caused by ambient light or sunlight.

Package Outline
μPD2732AD (Cerdip)



Item	Millimeters	Inches
A	33.5 MAX	1.32 MAX
B	2.78	1.1
C	2.54	0.1
D	0.46 ± 0.10	0.018 ± 0.004
E	27.94	1.10
F	1.3	0.05
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.020
I	5.0 MAX	0.20
J	5.5 MAX	0.216
K	15.24	0.60
L	14.66	0.58
M	0.25 ± 0.05	0.010 ± 0.002

μPD2764
65,536 (8K × 8) BIT UV ERASABLE PROM

Description

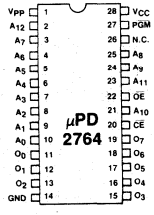
The μPD2764 is a 65,536-bit (8192 x 8 bit) Ultraviolet Erasable and Electrically Programmable Read-Only Memory (EPROM). It operates from a single +5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with an attendant 67% savings in power consumption.

A distinctive feature of the μPD2764 is a separate output control, output enable ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD2764 features fast, simple one-pulse programming controlled by TTL-level signals. Total programming time for all 65,536 bits is 420 seconds.

Features

- ☐ Ultraviolet erasable and electrically programmable
- ☐ Access time—250 ns max
- ☐ Single location programming
- ☐ Programmable with single pulse
- ☐ Low power dissipation: 150 mA max active current, 50 mA max standby current
- ☐ Input/Output TTL-compatible for reading and programming
- ☐ Single +5V power supply
- ☐ 28-pin ceramic DIP
- ☐ Three-state outputs

Pin Configuration



Pin Names

A_0-A_{12}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program
N.C.	No Connect

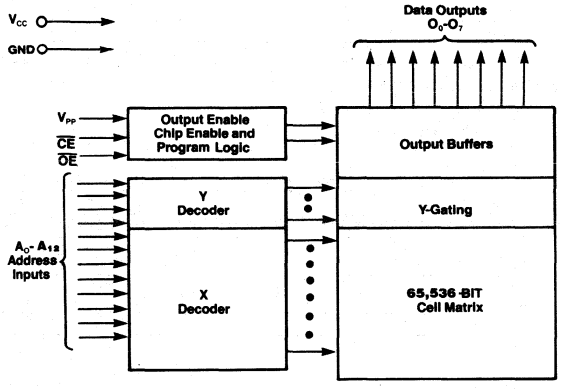
MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}

Table 1 – Mode Selection

Block Diagram



Absolute Maximum Ratings* (T_a = 25°C)

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.6 to +6V
Input Voltage	−0.6 to +6V
Supply Voltage V_{CC}	−0.6 to +6V
Supply Voltage V_{PP}	−0.6 to +22V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			12	pF	V_{OUT} = 0V

DC Characteristics

Read Mode and Standby Mode
T_a = 0°C to 70°C; V_{CC} = +5V ±5%

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Output Leakage Current	I_{LO}			10	μA	V_{OUT} = 5.25 V
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 5.25 V
V_{CC} Current Standby	I_{CC1}			50	mA	$\overline{CE}$ = V_{IH}
V_{CC} Current Active	I_{CC2}			150	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}

DC Characteristics (Cont.)

Program, Program Verify and Program Inhibit Mode
T_a = 25°C ± 5°C, V_{CC} = +5V ± 5%, V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		$V_{CC}+1$	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -400\,\mu A$
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}			150	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IL}$

AC Characteristics

Read Mode and Standby Mode
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address to Output Delay	t_{ACC}			250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}			250	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}	10		100	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		90	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Test Conditions —
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.8 to 2.2V
Timing Measurement Reference Level:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

Program, Program Verify and Program Inhibit Mode
T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Chip Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from $\overline{OE}$	t_{OE}			150	ns	
Program Pulse Width	t_{PW}	45	50	55	ms	
V_{PP} Setup Time	t_{VS}	2			μs	

Test Conditions —
Input Pulse Levels = 0.8V to 2.2V
Input Timing Reference Level = 1.0V and 2.0V
Output Timing Reference Level = 0.8V and 2V
Input Rise and Fall Times: 20 ns

Function

The μPD2764 operates from a single +5V power supply, making it ideal for microprocessor applications.

Programming of the μPD2764 is achieved with a single 50 ms TTL pulse. Total programming time for all 65,536 bits is 420 sec. Due to the simplicity of the programming requirements, devices on boards and in systems may be easily programmed without any special programmer.

The μPD2764 features a standby mode which reduces the power dissipation from a maximum active power dissipation of 788 mW to a maximum standby power dissipation of 262 mW. This results in a 67% savings with no increase in access time.

Erasure of the μPD2764 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2764. Consequently, if the μPD2764 is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the μPD2764 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15 W-sec/cm². The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000 μW/cm² power rating.

During erasure, the μPD2764 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Operation

The five operation modes of the μPD2764 are listed in Table 1. In READ mode, the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for V_{PP} which is pulsed from TTL level to 21V.

Read Mode

When $\overline{CE}$ and $\overline{OE}$ are at low (0) level, READ is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD2764 is placed in standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced by 67% from 788 mW to 262 mW.

Programming

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2764 is placed in programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ and $\overline{PGM}$ with V_{PP} at +21V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

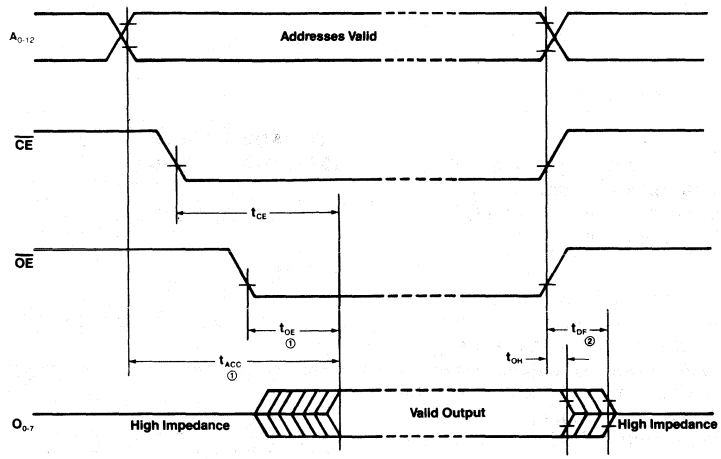
When multiple μPD2764s are connected in parallel except for $\overline{CE}$, individual μPD2764s can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD2764 to be programmed.

Programming of multiple μPD2764s in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

Programming Inhibit Mode

Programming multiple μPD2764s in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD2764s may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with V_{PP} at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD2764 will inhibit it from being programmed.

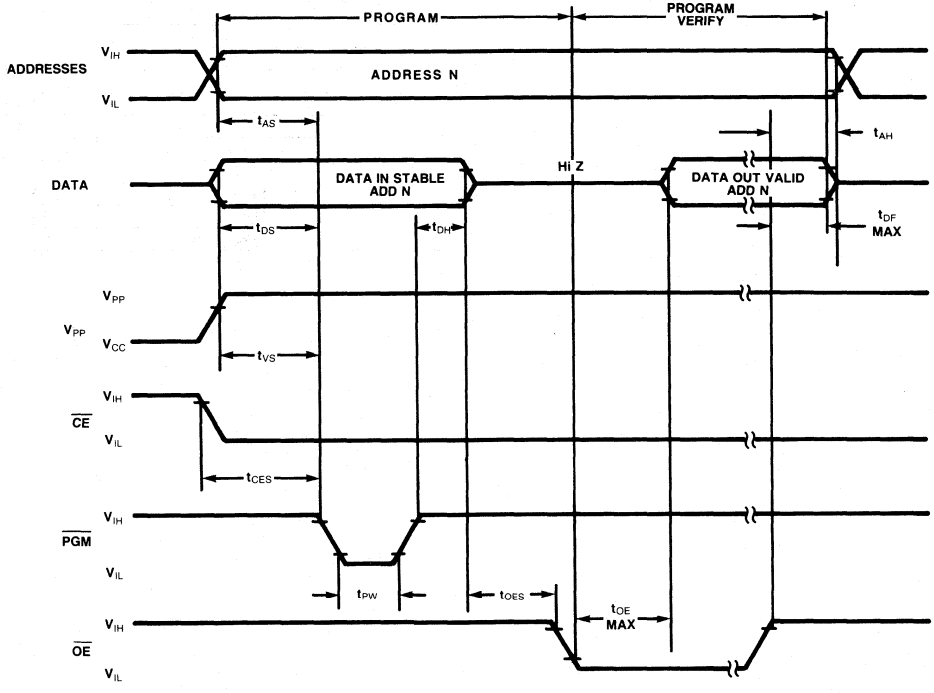
Read Mode



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

4

Program Mode



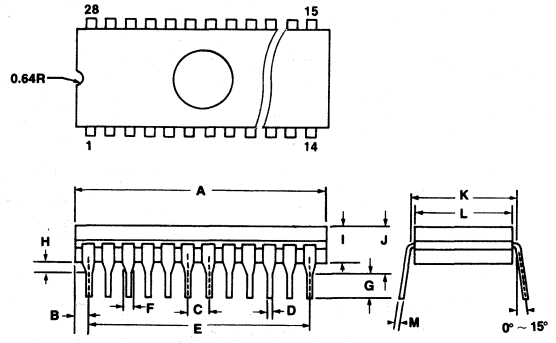
Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at high (1) level.

Output Deselect

The data outputs of two or more μPD2764s may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2764s should be deselected by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the READ line from the system control BUS. These connections offer the lowest average power consumption.

Package Outline
μPD2764 D (Cerdip)



Item	Millimeters	Inches
A	37.7 MAX.	1.48 MAX.
B	2.78	1.1
C	2.54	0.1
D	0.46 ± 0.10	0.018 ± 0.004
E	27.94	1.10
F	1.3	0.05
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.020
I	5.0 MAX.	0.20
J	5.5 MAX.	0.216
K	15.24	0.60
L	14.66	0.58
M	0.25 ± 0.05	0.010 ± 0.002

NEC

NEC Electronics U.S.A. Inc.

Microcomputer Division

MEMORIES

ELECTRONIC ARRAYS MASK PROGRAMMED READ ONLY MEMORIES

5

Custom ROM Verification Code Procedure

ROMs the Right Way

You will select well if you choose Electronic Arrays as your supplier of mask programmed ROMs.

Every ROM is like a custom LSI circuit. It's designed to store a bit pattern unique to your requirements. No one else can use your ROM. And you depend upon your ROM supplier to meet his commitments regarding delivery and quality. A ROM manufacturer must therefore be particularly cognizant of the custom nature of the business if he is to be effective in meeting customer needs.

At EA, we have the "ROM PERSPECTIVE", developed over a ten-year period of supplying custom ROMs. By utilizing our Mother Lot contact mask programming technique, and local domestic assembly, EA ships quality ROMs with fast, reliable delivery.

We also apply our knowledge to make verifying your custom ROM patterns a snap. With your complete input, as described within, we'll read out, duplicate, and send a verification package on its way back to you in 24 hours—every time.

NEC Electronics U.S.A. Inc.
Electronic Arrays Division

NEC

A. VERIFICATION SEQUENCE SUMMARY

The diagram on page 3 details the procedure used by EA to verify your bit patterns. At your end, the sequence is simple. EA does all the hard stuff.

1. You ship to EA UV EPROMs or ROMs containing your custom bit patterns.
2. Upon receipt, EA reads out your patterns onto our PDP-11/70 computer file.
3. EA programs UV EPROMs the same or electrically similar to those you submitted, using the stored program data base from our computer.
4. A complete octal printout of your code is generated, including designation of chip selects and any custom marking required.
5. The EA-programmed UV EPROMs and printout are shipped to you for verification and approval.
6. Upon your receipt and verification testing, you notify us by phone, TWX, or mail of your approval. This starts the clock as regards delivery of first samples and all subsequent deliveries.
7. You sign and return to EA the cover sheets attached to each ROM code printout in the space indicated. Please don't forget this last important detail.

B. SENDING COMPLETE DATA

Complete information is necessary from you to avoid unnecessary verification delays. The following checklist should be reviewed for all custom patterns sent to EA:

☐ 1. Have you included the desired chip select logic levels for each ROM? This information cannot be included in the UV EPROM, and must be furnished separately. We cannot proceed without it—it is an integral part of the ROM pattern data we require (see C below for details).

☐ 2. If your are sending multiple UV EPROMs for a single ROM (e.g., two 16K UV EPROMs for one 32K ROM), be sure each part is clearly marked with the starting address for that section of the ROM. It is best to include this address marking on the UV EPROM package itself via a sticker.

☐ 3. Are the UV EPROMs themselves electrically sound? Double check them to ensure they program and read out properly with the right levels.

☐ 4. Do you require your own marking on the package? We'll be happy to custom-mark your ROMs for you if you will supply us with your desired marking. We've up to 20 digits available on one line for your marking preference.

☐ 5. Are the devices properly packaged for shipment to EA? To avoid accidental UV erasure, be sure the quartz window is covered. A small, gummed label is good protection. And we receive many UV EPROMs in a "CRUSHED" condition—often irreparable. Do not ship in an envelope. Ensure the UV EPROMs are packed in a rigid container to physically protect the leads, and with conductive foam to protect them from static charge. Then ship in a jiffy bag, or better yet, a small box with protective packing.

☐ 6. Can you include duplicate master UV EPROMs (or ROMs)? This allows EA to use a checksum to attest to readout integrity and reduces the potential error rate. If you can't send duplicate masters, please include a checksum for each individual UV EPROM (or ROM). The more redundancy we receive, the more rigorous EA can be in each verification step.

☐ 7. If you wish to receive your masters back with their original program, please include blank UV EPROMs for EA to program for verification. This will facilitate our turn time, and allow us to return your masters with the verification EPROMs.

☐ 8. If you are ordering the EA8332 32K ROM, have you indicated whether you want the A or B pinout version? The pinout is irreversibly fixed simultaneous with the bit pattern during contact mask, and must be specified by you. Reference the front of the EA8332A/B data sheet for pinout option details.

C. CHIP SELECT PROGRAMMING

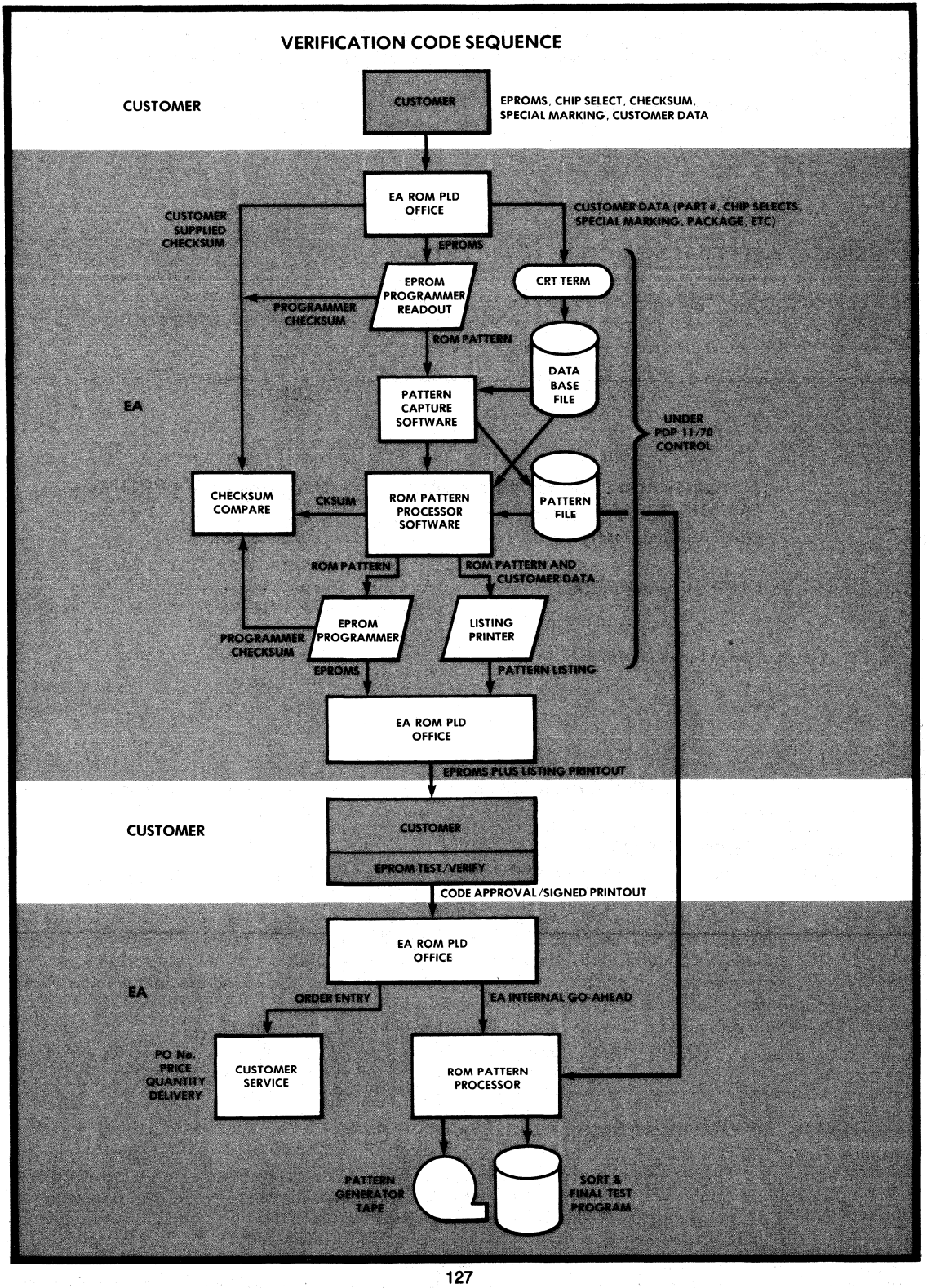
Every EA ROM has programmable chip selects which are permanently programmed into the ROM along with the bit pattern during wafer fabrication.

These chip selects are available for your convenience since they allow multiple ROMs to be utilized in parallel without external ROM select logic. **You must furnish EA with the desired chip selection logic level for each CS pin on your ROM concurrent with the submission of the bit pattern.**

See diagram on page 3. Note that the customer role is kept to a minimum in the overall verification effort. You need only:

1. Supply the EPROMs, CHIP SELECT, SPECIAL MARKING, CHECKSUM.
2. Test the product returned to you for verification.
3. Sign and return the approval sheet attached to each printout.

Prior to order entry into customer service, we of course also require your P.O. number, prices, quantity, and requested delivery schedule. All delivery commitments are based upon EA receipt of code verification and complete order entry data.


VERIFICATION CODE SEQUENCE
CUSTOMER
CUSTOMER
EPROMS, CHIP SELECT, CHECKSUM, SPECIAL MARKING, CUSTOMER DATA
EA ROM PLD OFFICE
CUSTOMER SUPPLIED CHECKSUM
CUSTOMER DATA (PART #, CHIP SELECTS, SPECIAL MARKING, PACKAGE, ETC)
EPROMS
EPROM PROGRAMMER READOUT
CRT TERM
PROGRAMMER CHECKSUM
ROM PATTERN
DATA BASE FILE
EA
PATTERN CAPTURE SOFTWARE
UNDER PDP 11/70 CONTROL
CHECKSUM COMPARE
CKSUM
ROM PATTERN PROCESSOR SOFTWARE
PATTERN FILE
ROM PATTERN
ROM PATTERN AND CUSTOMER DATA
PROGRAMMER CHECKSUM
EPROM PROGRAMMER
LISTING PRINTER
EPROMS
PATTERN LISTING
EA ROM PLD OFFICE
EPROMS PLUS LISTING PRINTOUT
CUSTOMER
CUSTOMER
EPROM TEST/VERIFY
CODE APPROVAL/SIGNED PRINTOUT
EA ROM PLD OFFICE
EA
ORDER ENTRY
EA INTERNAL GO-AHEAD
PO No. PRICE QUANTITY DELIVERY
CUSTOMER SERVICE
ROM PATTERN PROCESSOR
PATTERN GENERATOR TAPE
SORT & FINAL TEST PROGRAM

5

Each chip select (CS) must be programmed to be selected by either a logic 1 or logic 0. Reference the ROM data sheet "DC Operating Characteristics" to correctly interpret the logic 1 (high) and logic 0 (low) voltage conditions when determining your chip select options.

Chip selects must be specified for the following pins on EA ROMs:

ROM TYPE	SIZE	CHIP SELECT PINS	TOTAL
EA8308A	8K	18, 20	2
EA8316E	16K	18, 20, 21	3
EA8332A	32K	20, 21	2
EA8332B	32K	18, 20	2
EA8364	64K	20	1

D. USING UV EPROMS FOR CODE TRANSMITTAL

EA receives the vast majority of its customer codes by way of customer-programmed UV EPROMs. You may utilize any of the following UV EPROMs to transmit codes to EA:

UV EPROM	SIZE
2708	8K
2716/2516	16K
2732/2532	32K
2764/2564	64K

To transmit a code for this ROM:	Use these UV EPROMs:
EA8308A (8K ROM)	**One 2708**
EA8316E (16K ROM)	**Two 2708's or One 2716**
EA8332A/B (32K ROM)	**Four 2708's or Two 2716's or One 2732**
EA8364 (64K ROM)	**Eight 2708's or Four 2716's or Two 2732's or One 2764**

When submitting multiple UV EPROMs for one ROM code, **remember to mark the starting address on each EPROM (B-2. above).**

E. EXPEDITED VERIFICATION

If distances are great and/or time is of the absolute essence, EA has an alternate verification procedure you may use:

UV EPROMs- Send EA 3 identically programmed UV EPROMs or sets of UV EPROMs. EA will read out all 3 and test for a match. If a match is obtained, EA will proceed with masking to produce ROMs identical to the 3 received. A printout will be furnished, but for information purposes only, not approval. The customer is responsible for the integrity of the patterns as submitted.

MASKED ROMs- Send 2 masked ROMs or sets of ROMs. EA will test for a match. If a match is obtained, EA will proceed with masking to produce ROMs identical to those received. A printout will be furnished, but for information purposes only, not approval. EA guarantees their ROMs to contain the identical pattern as the ROMs EA received.

F. ALTERNATE CODE TRANSMITTAL METHODS

There are acceptable alternatives to transmitting custom ROM codes to EA other than via UV EPROMs or ROMs. Codes may be transmitted via paper tape, punched cards, or other acceptable mediums. Standard octal and hexadecimal formats are currently available for use with punched computer cards or paper tape. Other non-standard formats may be acceptable provided adequate descriptions and compatible equipment are available. Contact EA sales personnel for further details and factory response.

μPD2316E/EA8316E
READ ONLY MEMORY
2048 WORDS, 8 BITS/WORD

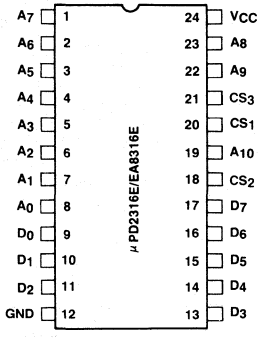
Description

The μPD2316E/EA8316E is a 16,384-bit Read Only Memory utilizing MOS N-channel silicon gate technology. The device is completely static in operation, organized as 2,048 words by 8 bits, and operates from a single +5 volt power supply. All inputs and outputs are fully TTL compatible. It has three programmable chip select inputs and three-state outputs that allow memory expansion to 16,384 words by 8 bits without the use of any external logic. Programming of the device is accomplished by a custom mask during fabrication. The EA8316E pin-out is compatible with 2708 and 2716 EPROMs and can replace two 2708s or one 2716 for production. The EA8316E is available to two access time specifications, the standard 450 ns or the faster 350 ns version.

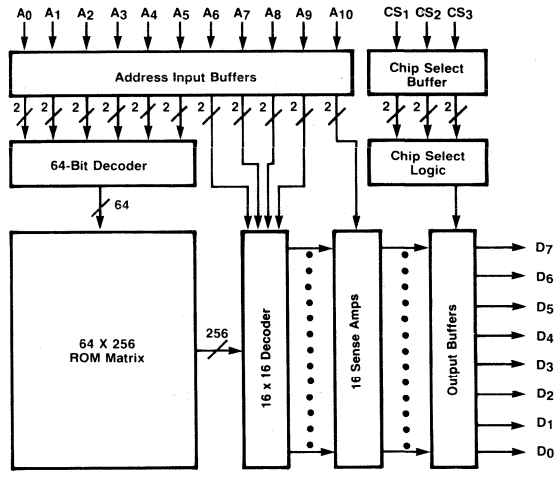
Features

- ☐ Two Fast Access Time Options
  - — 450 ns Maximum, EA8316E
  - — 350 ns Maximum, EA8316E-5
- ☐ All Outputs Drive 2 TTL Loads Directly
- ☐ All Inputs TTL Compatible
- ☐ Single +5 Volt Supply with ±5% Tolerance
- ☐ Three-State Outputs for Direct Bus Compatibility
- ☐ Three Programmable Chip Select Inputs
- ☐ Pin-Compatible to 2708 and 2716 EPROMs
- ☐ Fully Static Operation
- ☐ All Inputs Protected Against Static Charge

Pin Configuration



Block Diagram



5

Absolute Maximum Ratings*

T_a = 25°C, f = 1 MHz

Voltage on All Inputs, Outputs, and Supply Pins	−0.5 to 7.0V
Maximum Junction Temperature	+150°C
θ_{JC} (Hermetic DIP)	+65°C/W
Storage Temperature	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C, f = 1MHz. All pins at 0 volts.

Parameter	Symbol	Limits Min	Typ	Max	Test Conditions
Input Capacitance	C_{IN}		5pF	7pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		7pF	10pF	V_{OUT} = 0V

DC Characteristics

T_a = −10°C to +70°C and V_{CC} = 5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Load Current	I_{IL}			10	μA	V_{IN} = 0 to + 5.25V
Output "Low" Voltage	V_{OL}			0.40	V	I_{OL} = +3.2 mA
Output "High" Voltage	V_{OH}	2.4			V	I_{OH} = −200 μA
Output Leakage Current	I_{LO}			10	μA	Chip disabled, V_{OUT} = +0.4V to V_{CC}
Power Supply Current	I_{CC}		60	90	mA	All inputs +5.25V, Outputs unloaded

μPD2316E/EA8316E

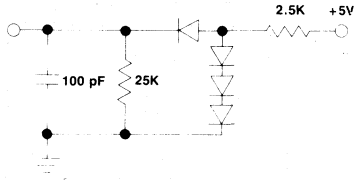
AC Characteristics

T_a = −10°C to +70°C

Parameter	Symbol	EA8316E-5 Min	EA8316E-5 Max	EA8316-E Min	EA8316-E Max	Unit
Address to Output Delay Time	t_{ACC}		350		450	ns
Chip Select to Output Delay Time	t_{CO}		150		150	ns
Chip Deselect to Output Data Float Time	t_{DF}		100		100	ns
Previous Data Valid After Address Change	t_{OH}	20		20		ns

AC Test Conditions

Input Pulse Rise and Fall Times . . . . . 20 ns
Timing Measurement Reference
Levels: . . . . . V_{IH}, V_{OH} = 2.0V; V_{OL}, V_{IL} = 0.8V.



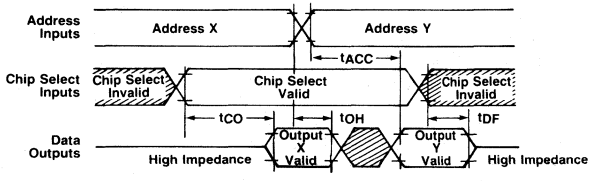
Output Load (AC): 1 TTL Load + 100 pF.

Standard Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground. Positive current flows into the referenced pin.

Output Load (AC): 2 Series 74 TTL, C_L = 100 pF
$0°C \leq t_A \leq +70°C$
$+4.75V \leq V_{CC} \leq +5.25V$

Timing Waveform



Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid Address and the corresponding valid Data Out.

Output Hold Delay, t_{OH}

Output hold delay is the minimum time after an Address change that the previous data remains valid.

Output Enable Time, t_{CO}

Output enable time is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

Output Disable Time, t_{DF}

Output disable time is the delay between Chip Selects becoming false and output stages going to the high impedance state.

Custom Programming Instructions

Bit Pattern Submittal Options

The customer's unique bit pattern can be submitted to Electronic Arrays via several convenient methods such that it is easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to EA contained within:

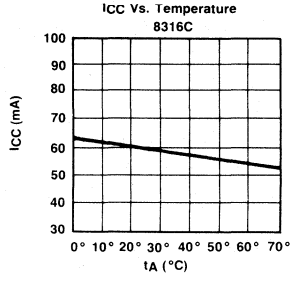
1. One programmed 2716 EPROM
2. Two programmed 2708 EPROMs
3. One customer-programmed 8316E ROM
4. Punched computer cards per the detail format shown below.

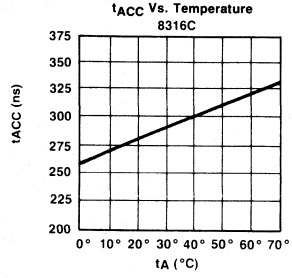
Bit Pattern Verification

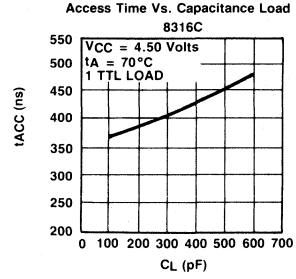
For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found by experience to be most expeditious.

Customer Pattern Submitted Via:	Verification Routine
1. One programmed 2716	Customer sends EA one additional erased 2716. EA programs the spare 2716 with the pattern data base extracted from the programmed 2716, and returns to customer for pattern verification.
2. Two programmed 2708s	Customer sends EA two additional erased 2708s. EA programs the spare 2708s with the pattern data base extracted from the programmed 2708s and returns to customer for pattern verification.

Typical Characteristics







Customer Pattern Submitted Via:	Verification Routine
3. One mask-programmed 8316E (or one 16K ROM)	Customer sends EA one erased 2716 or two erased 2708s. EA programs these EPROMs with the pattern data base extracted from the 8316 and returns to the customer for pattern verification.
4. Punched computer cards	After extracting the bit pattern from the card deck, EA's data base is used to punch a new deck. This deck, plus a complete printout, is returned to customer for pattern verification.

In all cases a computer printout of the complete bit pattern is also available upon customer request. The original 2716s, 2708s, or 8316s are retained by EA as the original bit pattern source data, at least until the first sample EA8316Es are tested and customer-approved.

The data base tape derived from the above source devices or card deck is utilized in turn to produce a pattern generator tape and ROM test pattern. The pattern generator tape drives EA's automatic pattern generation mask equipment, resulting in mask tooling that contains the customer's unique one/zero pattern. The ROM test pattern is used at production sort and final test to test each device 100% to the complete custom bit pattern.

Chip Select Level Programming

CS_1, CS_2, and CS_3 must be programmed by the customer to be selected by either a logic 1 or a logic 0 level. Accordingly, the customer must furnish EA with the desired chip selection level (1 or 0 only) for CS_1, CS_2, and CS_3, concurrent with submission of the bit pattern. The CS input logic levels are permanently established within each ROM in the same manner as the bit pattern.

Punched Computer Card Instructions

This technique requires that the customer supply EA with a deck of standard 80-column computer cards describing the data to be stored in the ROM array.

Title Card

All customer ROM "Data Cards" must be preceded by a "Title Card" which contains all unique information pertaining to that ROM other than the ROM data content. The required punching format is as follows:

Card Column No.	Card Contents
1	*(Asterisk)
2-19	Customer Name
20-21	Blank (no punch)
22-23	Month; e.g., 05 for May
24	/(slash)
25-26	Day of the month; e.g., 04 for the 4th day
27	/(slash)
28-29	The last two digits of the year
30-31	Blank
32-36	ROM Type (i.e., 8316E)
37	Blank
38-41	CS_1 =
42	CS_1 level desired for chip selection (1 or 0 only)
43	Blank
44-47	CS_2 =
48	CS_2 level desired for chip selection (1 or 0 only)
49-54	Blank
55-80	Customer part number

Alternative Data File Formats

In addition to the standard EA octal format, it is possible to furnish data to EA in other formats if prearranged with the factory. A standard hexadecimal format is currently available. Other nonstandard formats may be acceptable. Contact EA sales personnel.

Data Cards

The required punching format is described below. All addresses must be included with their outputs defined. That is, no assumptions are made regarding the bit configuration of undefined outputs. Therefore, the customer must submit cards defining the entire ROM contents, when portions of the ROM may be unused (zero).

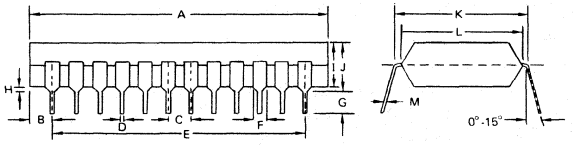
Card Column No.	Octal Pattern Format Card Contents
1-4	Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card (this is the initial address).
5-7	Punch a 3-digit octal number representing the outputs for the input address specified in column 1-4.
8-10	Punch a 3-digit octal number representing the outputs for the initial input address + 1.
11-13	Punch a 3-digit octal number representing the outputs for the initial input address + 2.
—	—
—	—
—	—
50-52	Punch a 3-digit octal number representing the outputs for the initial input address + 15.
53-59	Blank
60-80	Not used by EA. May contain customer identification.

Each card, therefore, carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the unique ROM number. The cards must be provided for all possible sequential address locations (in blocks of 16). A 2,048-word ROM therefore, requires 128 cards, with all 16 output words defined on each card.

5

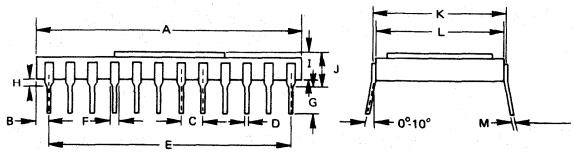
μPD2316E/EA8316E

Package Outlines
μPD2316EC
EA8316EC
Plastic



Item	Millimeters	Inches
A	33 Max	1.3 Max
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 Min	0.1 Min
H	0.5 Min	0.02 Min
I	5.22 Max	0.205 Max
J	5.72 Max	0.225 Max
K	15.24	0.6
L	13.2	0.55 Max
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD2316ED
EA8316ED
Ceramic



Item	Millimeters	Inches
A	30.78 Max	1.23 Max
B	1.53 Max	0.07 Max
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 Min	0.04 Min
G	3.2 Min	0.125 Min
H	1.02 Min	0.04 Min
I	3.23 Max	0.13 Max
J	4.25 Max	0.17 Max
K	15.24 Typ	0.60 Typ
L	14.93 Typ	0.59 Typ
M	0.25 ± 0.05	0.010 ± 0.002

μPD2332A/B/EA8332A/B
READ ONLY MEMORY
4096 WORDS, 8 BITS/WORD

Description

The μPD2332A/B/EA8332A/B is a 32,768-bit fully static Read Only Memory utilizing MOS N-channel silicon-gate ion-implanted technology. It is organized 4096 words by 8 bits and operates from a single +5 volt power supply with a ±10% supply tolerance. All inputs are TTL compatible, and the three-state outputs can drive 2 standard TTL loads each. It is unique in that both proposed JEDEC standard pin configurations are available. The 8332A incorporates CS_2 and A_{11} on pins 21 and 18 respectively. The EA8332B incorporates CS_2 and A_{11} on pins 18 and 21 respectively. Hence pin compatibility with other available 32K ROMs is at user option. Both pinout versions are available to two access time specifications, the standard 450 ns or the faster 350 ns version.

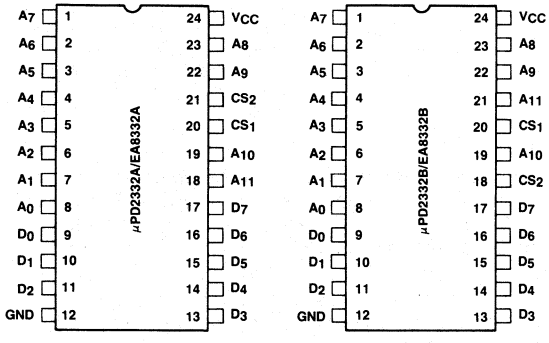
Features

- ☐ Two Fast Access Time Options
  - — 450 ns Max, EA8332
  - — 350 ns Max, EA8332-1
- ☐ All Outputs Drive 2 TTL Loads Directly
- ☐ All Inputs TTL Compatible
- ☐ Single +5 Volt Supply with ±10% Tolerance
- ☐ Three-State Outputs for Direct Bus Compatibility
- ☐ Both Proposed JEDEC Pinouts Available

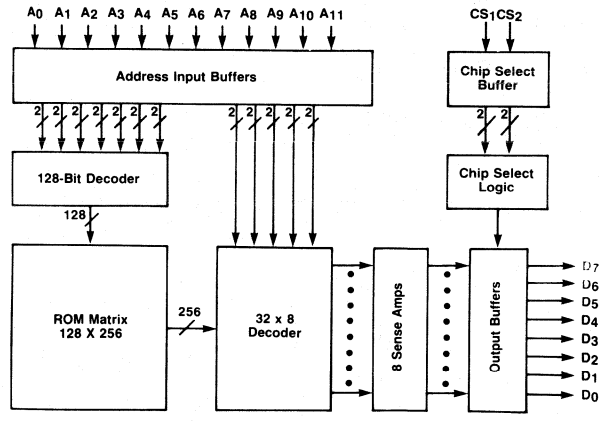
	Pin 18	Pin 21
EA8332A	A_{11}	CS_2
EA8332B	CS_2	A_{11}

- ☐ Two Programmable Chip Select Inputs
- ☐ Pin Compatible to EA2716 and 2732 EPROMs
- ☐ Fully Static Operation
- ☐ All Inputs Protected Against Static Charge

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

T_a = 25°C, f = 1 MHz	
Voltage on All Inputs, Outputs, and Supply Pins	−0.5 to 7.0V
Maximum Junction Temperature	+150°C
θ_{JC} (Hermetic DIP)	−65°C/W
Storage Temperature	−65°C to +150°C

*COMMENT: Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground. Positive current flows into the referenced pin.

Output Load (AC): 2 Series 74 TTL, C_L = 100 pF
$0°C \leq t_A \leq +70°C$
$+4.50V \leq V_{CC} \leq +5.50V$

DC Characteristics

T_a = −10°C to +70°C and V_{CC} = 5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		$V_{CC}+1$	V	
Input Load Current	I_{IL}			10	μA	V_{IN} = 0 to 5.5V
Output "Low" Voltage	V_{OL}			0.40	V	I_{OL} = +3.2 mA
Output "High" Voltage	V_{OH}	2.4			V	I_{OH} = −200 μA
Output Leakage Current	I_{LO}			10	μA	Chip Disabled V_{OUT} = +0.4V to V_{CC}
Power Supply Current	I_{CC}		60	90	mA	All inputs +5.5V Output Unloaded

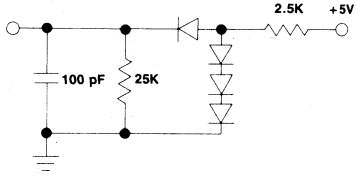
AC Characteristics

T_a = −10°C to +70°C

Parameter	Symbol	EA8332A/B-1 Min	EA8332A/B-1 Max	EA8332A/B Min	EA8332A/B Max	Unit
Address to Output Delay Time	t_{ACC}		350		450	ns
Chip Select to Output Delay Time	t_{CO}		150		150	ns
Chip Deselect to Output Data Float Time	t_{DF}		100		100	ns
Previous Data Valid After Address Change	t_{OH}	20		20		ns

AC Test Conditions

Input Pulse Rise and Fall Times . . . . . 20 ns
Timing Measurement Reference Levels: . . . . . V_{IH},V_{OH} = 2.0V; V_{OL},V_{IL} = 0.8V



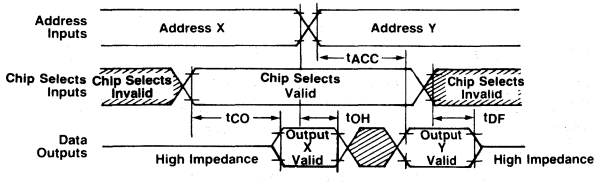
Output Load (AC): 1 TTL Load + 100 pF

Capacitance

T_a = 25°C, f = 1 MHz; all pins at 0 volts.

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Test Conditions
Input Capacitance	C_{IN}		5pF	7pF	V_{IN} = OV
Output Capacitance	C_{OUT}		7pF	10pF	V_{OUT} = OV

Timing Waveform



Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid Address and the corresponding valid Data Out.

Output Hold Delay, t_{OH}

Output hold delay is the minimum time after an Address change that the previous data remains valid.

Output Enable Time, t_{CO}

Output enable time is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

Output Disable Time, t_{DF}

Output disable time is the delay between Chip Selects becoming false and output stages going to the high impedance state.

Custom Programming Instructions

Bit Pattern Submittal Options

The customer's unique bit pattern can be submitted to Electronic Arrays via several convenient methods such that it is easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to EA contained within:

1. Two programmed 2716 EPROMs
2. Four Programmed 2708 EPROMs
3. Two customer-programmed 8316E ROMs
4. Two customer-programmed 8316A ROMs
5. Punched computer cards per the detail format shown below.

Bit Pattern Verification

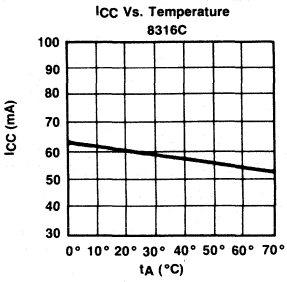
For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found by experience to be most expeditious.

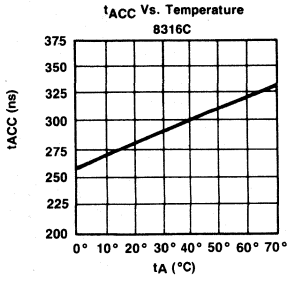
Customer Pattern Submitted Via:	Verification Routine
1. Two programmed 2716s	Customer sends EA two additional erased 2716s. EA programs the spare 2716s with the pattern data base extracted from the programmed 2716s, and returns to customer for pattern verification.
2. Four programmed 2708s	Customer sends EA four additional erased 2708s. EA programs the spare 2708s with the pattern data base extracted from the programmed 2708s and returns to customer for pattern verification.
3. Two mask-programmed 8316Es (or 8316As)	Customer sends EA two erased 2716s or four erased 2708s. EA programs these EPROMs with the pattern data base extracted from the 8316s and returns to the customer for pattern verification.
4. Punched computer cards	After extracting the bit pattern from the card deck, EA's data base is used to punch a new deck. This deck, plus a complete printout, is returned to customer for pattern verification.

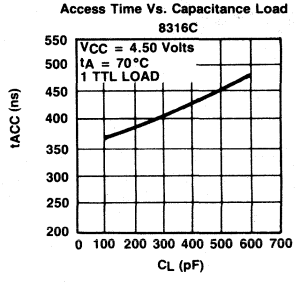
In all cases a computer printout of the complete bit pattern is also available upon customer request. The original 2716s, 2708s, or 8316s are retained by EA as the original bit pattern source data, at least until the first sample EA8332s are tested and customer approved.

The data base tape derived from the above source devices or card deck is utilized in turn to produce a pattern generator tape and ROM test pattern. The pattern generator tape drives EA's automatic pattern generation mask equipment, resulting in mask tooling that contains the customer's unique one/zero pattern. The ROM test pattern is used at production sort and final test to test each device 100% to the complete custom bit pattern.

Typical Characteristics







Customer Programming Instructions (Cont.)

Chip Select Level Programming

CS_1 and CS_2 must be programmed by the customer to be selected by either a logic 1 or a logic 0 level. Accordingly, the customer must furnish EA with the desired chip selection level (1 or 0 only) for CS_1 and CS_2, concurrent with submission of the bit pattern. The CS input logic levels are permanently established within each ROM in the same manner as the bit pattern.

Punched Computer Card Instructions

This technique requires that the customer supply EA with a deck of standard 80 column computer cards describing the data to be stored in the ROM array.

Title Card

All customer ROM "Data Cards" must be preceded by a "Title-Card" which contains all unique information pertaining to that ROM other than the ROM data content. The required punching format is as follows:

Card Column No.	Card Contents
1	*(Asterisk)
2-19	Customer Name
20-21	Blank (no punch)
22-23	Month; e.g., 0.5 for May
24	/(slash)
25-26	Day of the month; e.g., 04 for the 4th day
27	/(slash)
28-29	The last two digits of the year
30-31	Blank
32-36	ROM Type (i.e. 8332A or 8332B)
37	Blank
38-41	CS_1 =
42	CS_1 level desired for chip selection (1 or 0 only)
43	Blank
44-47	CS_2 =
48	CS_2 level desired for chip selection (1 or 0 only)
49-54	Blank
55-80	Customer part number

Alternative Data File Formats

In addition to the standard EA octal format, it is possible to furnish data to EA in other formats if prearranged with the factory. A standard hexadecimal format is currently available. Other nonstandard formats may be acceptable. Contact EA sales personnel.

Data Cards

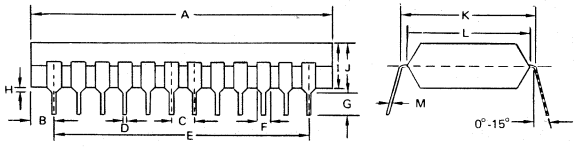
The required punching format is described below. All addresses must be included with their outputs defined. That is, no assumptions are made regarding the bit configuration of undefined outputs. Therefore, the customer must submit cards defining the entire ROM contents, when portions of the ROM may be unused (zero).

Card Column No.	Octal Pattern Format Card Contents
1-4	Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card (this is the initial address).
5-7	Punch a 3-digit octal number representing the outputs for the input address specified in column 1-4.
8-10	Punch a 3-digit octal number representing the outputs for the initial input address + 1.
11-13	Punch a 3-digit octal number representing the outputs for the initial input address + 2.
—	—
—	—
—	—
50-52	Punch a 3-digit octal number representing the outputs for the initial input address + 15.
53-59	Blank
60-80	Not used by EA. May contain customer identification.

Each card, therefore, carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the unique ROM number. The cards must be provided for all possible sequential address locations (in blocks of 16). A 4096 word ROM, therefore, requires 256 cards, with all 16 output words defined on each card.

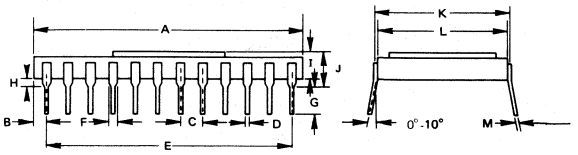
5

Package Outlines
μPD2338AC/EA8338AC
μPD2338BC/EA8338BC
Plastic



Item	Millimeters	Inches
A	33 Max	1.3 Max
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 Min	0.1 Min
H	0.5 Min	0.02 Min
I	5.22 Max	0.205 Max
J	5.72 Max	0.225 Max
K	15.24	0.6
L	13.2	0.55 Max
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD2338AD/EA8338AD
μPD2338BD/EA8338BD
Ceramic



Item	Millimeters	Inches
A	30.78 Max	1.23 Max
B	1.53 Max	0.07 Max
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 Min	0.04 Min
G	3.2 Min	0.125 Min
H	1.02 Min	0.04 Min
I	3.23 Max	0.13 Max
J	4.25 Max	0.17 Max
K	15.24 Typ	0.60 Typ
L	14.93 Typ	0.59 Typ
M	0.25 ± 0.05	0.010 ± 0.002

μPD2364/EA8364
READ ONLY MEMORY
8192 WORDS, 8 BITS/WORD

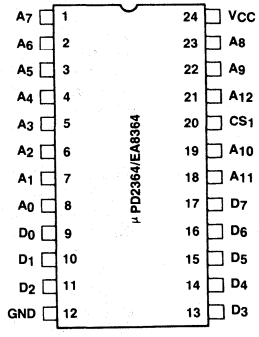
Description

The μPD2364/EA8364 is a 65,536-bit Read Only Memory utilizing MOS N-channel silicon gate technology. The device is completely static in operation, organized as 8192 words by 8 bits,and operates from a single +5 volt power supply. All inputs and outputs are fully TTL compatible. It has one programmable chip select input and three-state outputs that allow memory expansion to 16,384 words by 8 bits without the use of any external logic. Programming of the device is accomplished by a custom mask during fabrication. The EA8364 pin-out is compatible with 2716 and 2732 EPROMs and can replace two 2732s or one 2564 for production.

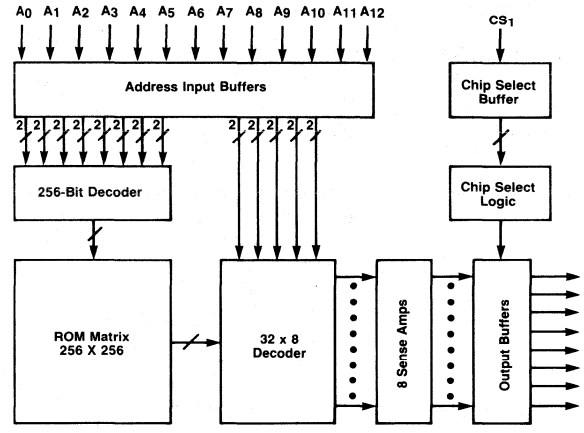
Features

- ☐ Two Fast Access Time Options
  - — 450 ns Maximum — EA8364
  - — 350 ns Maximum — EA8364-1
- ☐ All Inputs and Outputs TTL Compatible
- ☐ Single +5 Volt Supply with ±10% Tolerance
- ☐ Three-State Outputs for Direct Bus Compatibility
- ☐ One Programmable Chip Select Input
- ☐ Pin-Compatible to 2716, 2732, and 2564 EPROMs
- ☐ Fully Static Operation
- ☐ All Inputs Protected Against Static Charge

Pin Configuration



Block Diagram



5

Absolute Maximum Ratings*

T_a = 25°C, f = 1 MHz	
Voltage on All Inputs, Outputs, and Supply Pins	−0.5 to 7.0V
Maximum Junction Temperature	+150°C
θ_{JC} (Hermetic DIP)	−65°C/W
Storage Temperature	−65°C to +125°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Test Conditions
Input Capacitance	C_{IN}			10 pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			15 pF	V_{OUT} = 0V

DC Characteristics

T_a = −10°C to +70°C and V_{CC} = 5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Load Current	I_{IL}			10	μA	V_{IN} = 0 to 5.5V
Output "Low" Voltage	V_{OL}			0.4	V	I_{OL} = +3.2 mA
Output "High" Voltage	V_{OH}	2.4			V	I_{OH} = −200 μA
Output Leakage Current	I_{LO}			10	μA	Chip Disabled V_{OUT} = +0.4V to V_{CC}
Power Supply Current	I_{CC}		80	140	mA	All inputs +5.5V Output Disabled
Power Supply Current	I_{CC}		100	160	mA	All inputs +5.5V Output Disabled 8364-1

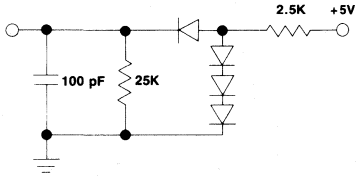
AC Characteristics

T_a = −10°C to +70°C

Parameter	Symbol	EA8364-1 Min	EA8364-1 Max	EA8364 Min	EA8364 Max	Unit
Address to Output Delay Time	t_{ACC}		350		450	ns
Chip Select to Output Delay Time	t_{CO}		150		150	ns
Chip Deselect to Output Data Float Time	t_{DF}		150		150	ns
Previous Data Valid After Address Change	t_{OH}	20		20		ns

AC Test Conditions

Input Pulse Rise and Fall Times . . . . . 20 ns
Timing Measurement Reference
Levels . . . . . V_{IH}, V_{OH} = 2.0V; V_{OL}, V_{IL} = 0.8V



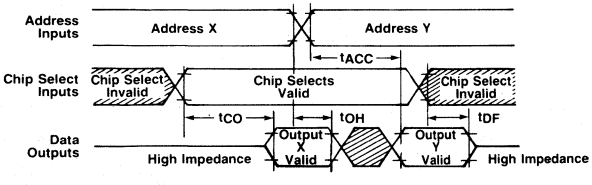
Output Load (AC): 1 TTL Load + 100 pF

Standard Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground. Positive current flows into the referenced pin.

Output Load (AC): 1 Series 74 TTL, C_L = 100 pF
$0°C \leq t_A \leq +70°C$
$+4.50V \leq V_{CC} \leq +5.50V$

Timing Waveform



Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid Address and the corresponding valid Data Out.

Output Hold Delay, t_{OH}

Output hold delay is the minimum time after an Address change that the previous data remains valid.

Output Enable Time, t_{CO}

Output enable time is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

Output Disable Time, t_{DF}

Output disable time is the delay between Chip Selects becoming false and output stages going to the high impedance state.

Custom Programming Instructions

Bit Pattern Submittal Options

The customer's unique bit pattern can be submitted to Electronic Arrays via several convenient methods such that it is easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to EA contained within:

1. One programmed 2564/2764 EPROM
2. Two programmed 2532/2732 EPROMs
3. Four programmed 2516/2716 EPROMs
4. One customer-programmed 8364 ROM
5. Two customer-programmed 8332 ROMs

Bit Pattern Verification Sequence

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found by experience to be most expeditious.

Customer Pattern Submitted Via:	Verification Routine
1. One programmed 2564/2764	Customer sends EA one additional erased 2564/2764. EA programs the spare 2564/2764 with the pattern data base extracted from the programmed 2564/2764, and returns to customer for pattern verification.
2. Two programmed 2532/2732s	Customer sends EA two additional erased 2532/2732s. EA programs the spare 2532/2732s with the pattern data base extracted from the programmed 2532/2732s and returns to customer for pattern verification.
3. Four programmed 2516/2716s	Customer sends EA four additional erased 2516/2716s. EA programs the spare 2516/2716s with the pattern data base extracted from the programmed 2516/2716s and returns to customer for pattern verification.
4. One mask programmed 64K ROM (or 2 32K masked ROMs)	Customer sends EA one additional erased 2564/2764 or two additional erased 2532/2732s. EA programs these EPROMs with the pattern data base extracted from the 64K ROM (or 32K ROMs) and returns to customer for pattern verification. An alternative to the above is to provide EA with 2 identical ROMs. Each will capture the patterns from both, compare them, and if they match, the code is presumed correct. In this case, only a printout is returned to customer for verification. Whenever ROMs are used to submit bit patterns, include the ROM chip select logic levels for each.

In all cases where multiple EPROMs or ROMs are submitted for one 64K ROM (i.e., 2 32Ks or 4 16Ks) the applicable address locations of each device within the 64K memory map must be clearly indicated for each package—preferably on the device package itself.

Bit Pattern Verification Sequence

An additional verification alternative, when distances are great and/or time is of the essence, is to submit three identically programmed EPROMs (or sets of EPROMs, if not 2564/2764s). EA will compare all three programs, and if we get a match, proceed with tooling. A printout is returned to the customer but no verification EPROMs are necessary under these conditions.

EA is also equipped to accept bit patterns transmitted over the phone lines. If this method is desired by the customer, contact Electronic Arrays for format information and direct transmission procedures.

In all cases, a computer printout of the complete bit pattern is also furnished to all customers. Attached to each printout is a cover sheet containing data relevant to the ROM. Following careful review of the data and the bit pattern, the customer indicates verification and approval by signing the cover sheet and returning it to EA.

The data base tape derived from above source devices is utilized in turn to produce a pattern generator tape and a ROM test pattern. The pattern generator tape drives EA's automatic pattern generation mask equipment, resulting in mask tooling that contains the customer's unique one/zero pattern. The ROM test pattern is used at production wafer sort and final test to test each device 100% to the complete custom bit pattern.

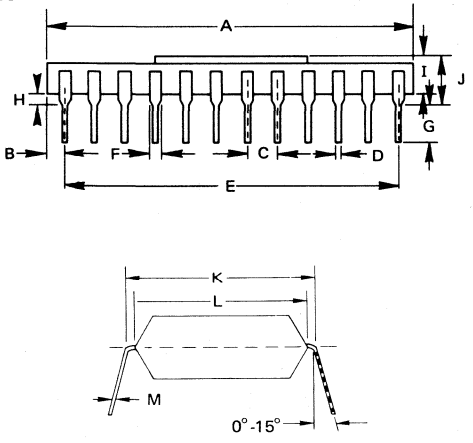
Chip Select Level Programming

CS_1 must be programmed by the customer to be selected by either a logic 1 or a logic 0 level. Accordingly, the customer must furnish EA with the desired chip selection level (1 or 0 only) for CS_1 concurrent with submission of the bit pattern. The CS input logic levels are permanently established within each ROM in the same manner as the bit pattern.

Alternative Data File Formats

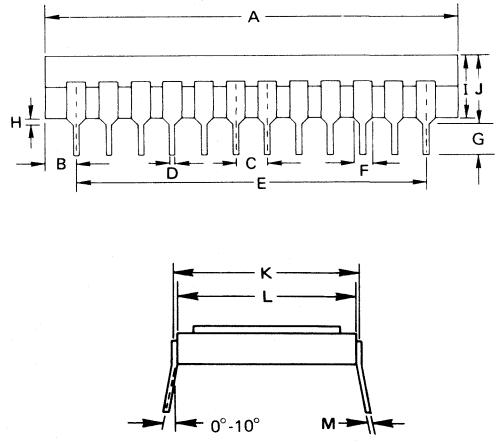
In addition to the EPROM technique, it is possible to furnish ROM data to EA in other media if prearranged with the factory. Standard octal and hexadecimal formats are currently available. Other nonstandard formats may be acceptable. Contact EA sales personnel.

Package Outlines
μPD2364C
EA8364C
Plastic



Item	Millimeters	Inches
A	33 Max	1.3 Max
B	2.53 Max	0.1 Max
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94 ± 0.1	1.1 ± 0.004
F	1.5 Min	0.059 Min
G	2.54 Min	0.1 Min
H	0.5 Min	0.02 Min
I	5.22 Max	0.205 Max
J	5.72 Max	0.225 Max
K	15.24 Typ	0.6 Typ
L	13.2 Typ	0.52 Typ
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD2364D
EA8364D
Ceramic



Item	Millimeters	Inches
A	30.78 Max	1.21 Max
B	1.53 Max	0.06 Max
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 Min	0.04 Min
G	3.2 Min	0.13 Min
H	1.02 Min	0.04 Min
I	3.23 Max	0.13 Max
J	4.25 Max	0.17 Max
K	15.24 Typ	0.60 Typ
L	14.93 Typ	0.59 Typ
M	0.25 ± 0.05	0.010 ± 0.002

NEC

NEC Electronics U.S.A. Inc.

Microcomputer Division

MICROCOMPUTERS

SINGLE CHIP 4-BIT MICROCOMPUTERS

6

4-BIT SINGLE CHIP MICROCOMPUTER FAMILY

DESCRIPTION

The μCOM-4 4-bit Microcomputer Family is a broad product line of 14 individual devices designed to fulfill a wide variety of design criteria. The product line shares a compatible architecture and instruction set. The architecture includes all functional blocks necessary for a single chip controller, including an ALU, Accumulator, Byte-wide ROM, RAM, and Stack. The instruction set maximizes the efficient utilization of the fixed ROM space, and includes a variety of Single Bit Manipulation, Table Look-Up, BCD arithemetic, and Skip instructions.

The μCOM-4 Microcomputer Family includes seven different products capable of directly driving 35V Vacuum Fluorescent Displays. Four products are manufactured with a CMOS process technology. μCOM-4 Microcomputers are ideal for low-cost general purpose controller applications such as industrial controls, instruments, appliance controls, intelligent VF display drivers, and games.

FEATURES

- Choice of ROM size: 2000 x 8, 1000 x 8, or 640 x 8
- Choice of RAM size: 96 x 4, 64 x 4, or 32 x 4
  - Six 4-Bit Working Registers Available
  - One 4-Bit Flag Register Available
- Powerful Instruction Set
  - Choice of 80 or 58 Instructions
  - Table Look-Up Capability with CZP and JPA Instructions
  - Single Bit Manipulation of RAM or I/O Ports
  - BCD Arithmetic Capability
- Choice of 3-Level, 2-Level, or 1-Level Subroutine Stack
- Extensive I/O Capability
  - Choice of 35 or 21 I/O Lines

	42/52-Pin Packages	28-Pin Package
– 4-Bit Input Ports	2	1
– 4-Bit I/O Ports	2	2
– 4-Bit Output Ports	4	2
– 3-Bit Output Ports	1	–
– 1-Bit Output Port	–	1

- Programmable 6-Bit Timer Available
- Choice of Hardware or Testable Interrupt
- Built-In Clock Signal Generation Circuitry
- Built-In Reset Circuitry
- Single Power Supply
- Low Power Consumption
- PMOS or CMOS Technologies
- Choice of 42-pin DIP, 28-pin DIP, or 52-pin Flat Plastic Package

Internal Registers

The ALU, the Accumulator, and the Carry Flag together comprise the central portion of the μCOM-4 Microcomputer Family architecture. The ALU performs the arithmetic and logical operations and checks for various results. The Accumulator stores the results generated by the ALU and acts as the major interface point between the RAM, the I/O ports, and the Data Pointer registers. The Carry F/F can be addressed directly, and can also be set during an addition. The μPD546, μPD553, μPD557L, and μPD650 also have a Carry Save F/F for storage the value of the Carry F/F.

Data Pointer Registers

The DP_H register and 4-bit DP_L register reside outside the RAM. They function as the Data Pointer, addressing the rows and columns of the RAM, respectively. They are individually accessible and the L register can be automatically incremented or decremented.

RAM

All μCOM-4 microcomputers have a static RAM organized into a multiple-row by 16-column configuration, as follows:

MICROCOMPUTER	RAM	ORGANIZATION	DP_H	DP_L
μPD546, μPD553, μPD557L, and μPD650	96 x 4	6 rows x 16 columns	3	4
μPD547, μPD547L μPD552, and μPD651	64 x 4	4 rows x 16 columns	2	4
μPD550, μPD550L, μPD554, μPD554L, and μPD652	32 x 4	2 rows x 16 columns	1	4

The μPD546, μPD553, μPD557L, and μPD650 also have a 4-bit Flag register and six 4-bit working registers resident in the last row of the RAM. Their extended instruction set provides 10 additional instructions with which you can access or manipulate these seven registers.

ROM

The ROM is the mask-programmable portion of the μCOM-4 Microcomputer which stores the application program. It is organized as follows:

MICROCOMPUTER	ROM	ORGANIZATION	
		FIELDS	PAGES
μPD546, μPD553, μPD557L, and μPD650	2000 x 8	8	16
μPD547, μPD547L, μPD552, μPD651	1000 x 8	8	8
μPD554, μPD554L, and μPD652	1000 x 8	8	8
μPD550 and μPD550L	640 x 8	8	8

FUNCTIONAL DESCRIPTION (CONT.)

Program Counter and Stack Register

The Program Counter contains the address of a particular instruction being executed. It is incremented during normal operation, but can be modified by various JUMP and CALL instructions. The Stack Register is a LIFO push-down stack register used to save the value of the Program Counter when a subroutine is called. It is organized as follows:

MICROCOMPUTER	STACK ORGANIZATION	ALLOWABLE SUBROUTINE CALLS
μPD546, μPD553, μPD557L, and μPD650	3 words x 11 bits	3 Levels
μPD651	2 words x 10 bits	2 Levels
μPD547, μPD547L, and μPD552	1 word x 10 bits	1 Level
μPD550, μPD550L, μPD554, μPD554L, and μPD652	1 word x 10 bits	1 Level

Interrupts

All μCOM-4 microcomputers are equipped with a software-testable interrupt which skips an instruction if the Interrupt F/F has been set. The TIT instruction resets the Interrupt F/F.

In addition, the μPD546, μPD553, μPD557L, and μPD650 have a level-triggered hardware interrupt, which causes an automatic stack level shift and interrupt service routine call when an interrupt occurs.

Interval Timer

The μPD546, μPD553, μPD557L, and μPD650 are equipped with a programmable 6-bit interval timer which consists of a 6-bit polynomial counter and a 6-bit binary down counter. The STM instruction sets the initial value of the binary down counter and starts the timing. The polynomial counter decrements the binary down counter when 63 instruction cycles have been completed. When the binary down counter reaches zero, the timer F/F is set. The TTM instruction tests the timer F/F, and skips the next instruction if it is set.

Clock and Reset Circuitry

The Clock Circuitry for any μCOM-4 microcomputer can be implemented by connecting either an Intermediate Frequency Transformer (IFT) and a capacitor, or a Ceramic Resonator and two capacitors, to the CL_0 and CL_1 Inputs. The Power-On-Reset Circuitry for any μCOM-4 microcomputer can be implemented by connecting a Resistor, a Capacitor, and a Diode to the RESET input.

FUNCTIONAL DESCRIPTION (CONT.)

I/O Capability

The μCOM-4 microcomputer family devices have either 35 or 21 I/O lines, depending upon the individual device, for communication with and control of external circuitry. They are organized as follows:

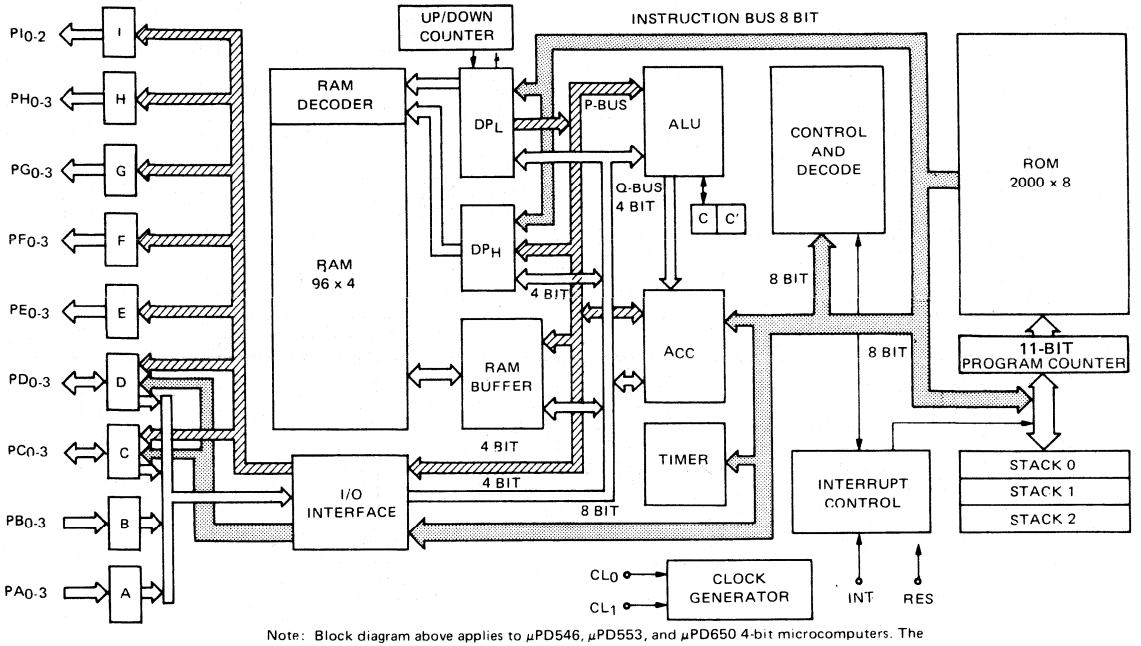
PORT	SYMBOL	FUNCTION	μPD546, μPD547, μPD547L, μPD552, μPD553, μPD650, and μPD651	μPD550, μPD550L, μPD554, μPD554L, μPD557L, and μPD652
Port A	PA_{0-3}	4-Bit Input	•	•
Port B	PB_{0-3}	4-Bit Input	•	
Port C	PC_{0-3}	4-Bit Input/Output (VF Drive Possible)	•	•
Port D	PD_{0-3}	4-Bit Input/Output (VF Drive Possible)	•	•
Port E	PE_{0-3}	4-Bit Output (VF Drive Possible)	•	•
Port F	PF_{0-3}	4-Bit Output (VF Drive Possible)	•	•
Port G	PG_{0-3}	4- Bit Output (VF Drive Possible)	•	
	PG_{0-1}	1-Bit Output (VF Drive Possible)		•
Port H	PH_{0-3}	4-Bit Output (VF Drive Possible)	•	
Port I	PI_{0-2}	3-Bit Output (VF Drive Possible)	•	

Development Tools

The NEC Development System (NDS) is available for developing software service code, editing, and assembling source code into object code. In addition, the ASM-43 Cross Assembler is available for systems which support either the Intel ISIS-II Operating System or the CP/M (® Digital Research Corp.) Operating System.

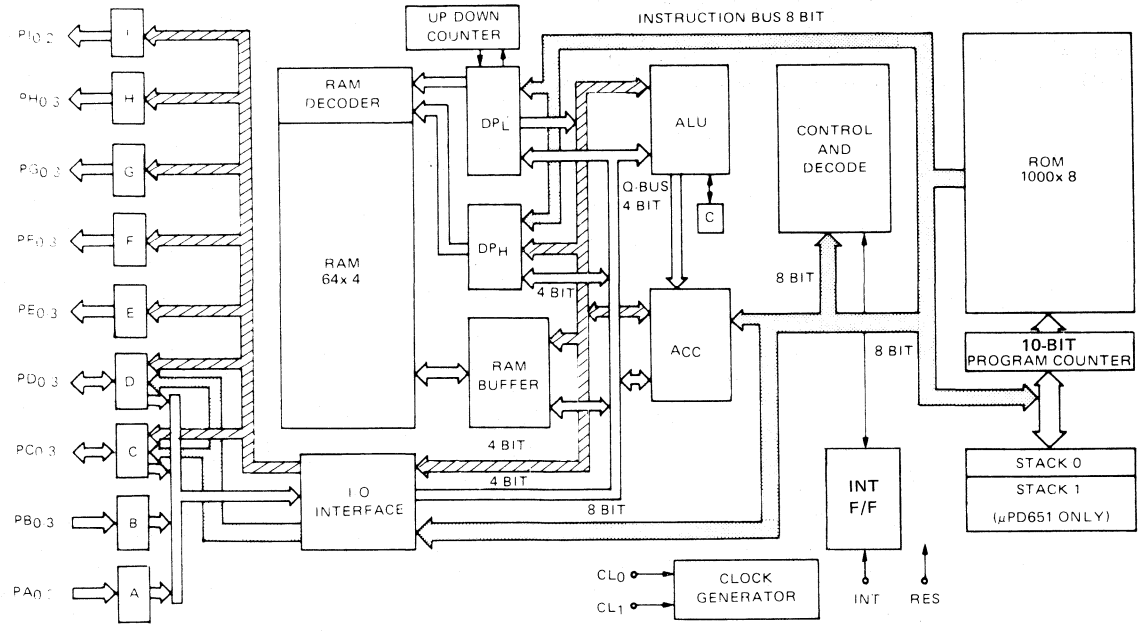
The EVAKIT-43P Evaluation Board is available for production device emulation and prototype system debugging. The SE-43P Emulation Board is available for demonstrating the final system design. The μPD556B ROM-less Evaluation Chip is available for small pilot production.

μPD546, μPD553, μPD557L, μPD650 BLOCK DIAGRAM

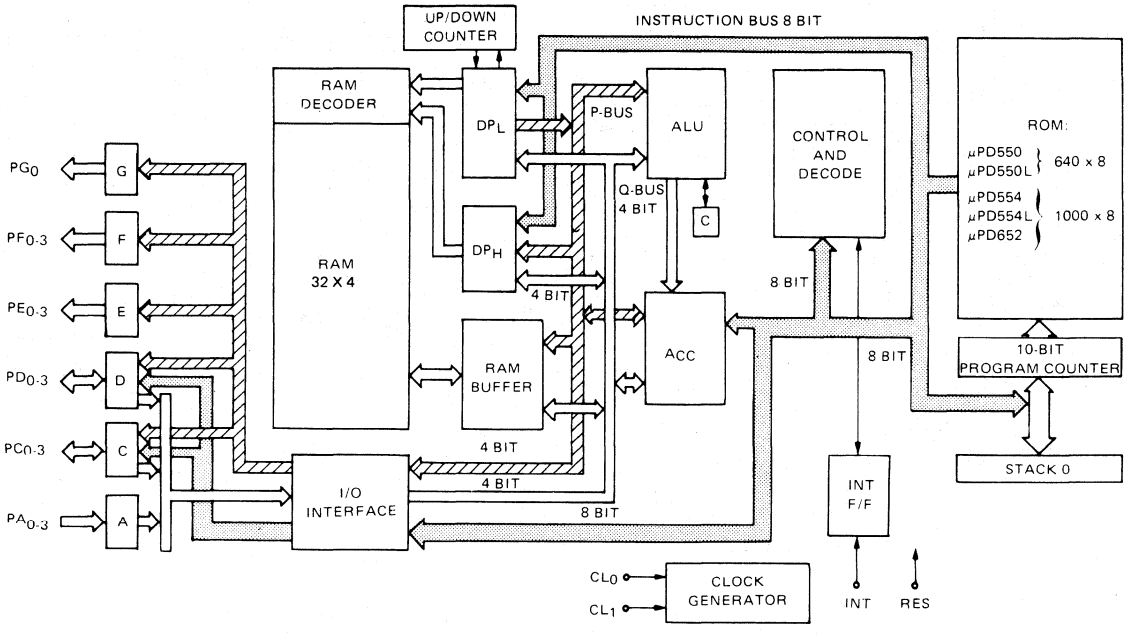


Note: Block diagram above applies to μPD546, μPD553, and μPD650 4-bit microcomputers. The μPD557L block diagram is similar to the above, except that PB_{0-3}, PG_{1-3}, PH_{0-3}, and PI_{0-2} have been eliminated to accommodate the μPD557L's 28-pin package.

μPD547, μPD547L, μPD552, μPD651 BLOCK DIAGRAM



BLOCK DIAGRAM



INSTRUCTION SET

The μPD546, μPD553, μPD557L, and μPD650 execute all 80 instructions of the extended μCOM-4 instruction set. The 22 additional instructions are indicated by shading.

The μPD547, μPD547L, μPD550, μPD550L, μPD552, μPD554, μPD554L, μPD651, and μPD652 execute a 58 instruction subset of the μCOM-4 instruction set.

INSTRUCTION SET SYMBOL DEFINITIONS

The following abbreviations are used in the description of the μCOM-4 instruction set:

SYMBOL	EXPLANATION AND USE
ACC	Accumulator
ACC_n	Bit "n" of Accumulator
address	Immediate address
C	Carry F/F
C′	Carry Save F/F
data	Immediate data
D_n	Bit "n" of immediate data or immediate address
DP	Data Pointer
DP_H	Upper Bits of Data Pointer
DP_L	Lower 4 Bits of Data Pointer
FLAG	FLAG Register
INTE F/F	Interrupt Enable F/F
INT F/F	Interrupt F/F
P( )	Parallel Input/Output Port addressed by the value within the brackets
P_n	Bit "n" of Program Counter
PA	Input Port A
PC	Input/Output Port C
PD	Input/Output Port D
PE	Output Port E
R	R Register
S	S Register
SKIP	Number of Bytes in next instruction when skip condition occurs
STACK	Stack Register
TC	6-Bit Binary Down Timer Counter
TIMER F/F	Timer F/F
W	W Register
X	X Register
Y	Y Register
Z	Z Register
( )	The contents of RAM addressed by the value within the brackets
[ ]	The contents of ROM addressed by the value within the brackets
←	Load, Store, or Transfer
↔	Exchange
−	Complement
∀	LOGICAL EXCLUSIVE OR
	Applies to μPD546, μPD553, μPD556B, μPD557L, and μPD650 only

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
			LOAD										
LI data	$A_{CC} \leftarrow D_{3\text{-}0}$	Load A_{CC} with 4 bits of immediate data; execute succeeding LI instructions as NOP instructions	1	0	0	1	D_3	D_2	D_1	D_0	1	1	String
L	$A_{CC} \leftarrow (DP)$	Load A_{CC} with the RAM contents addressed by DP	0	0	1	1	1	0	0	0	1	1	
LM data	$A_{CC} \leftarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1\text{-}0}$	Load A_{CC} with the RAM contents addressed by DP; Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of Immediate Data; Store the result in DP_H	0	0	1	1	1	0	D_1	D_0	1	1	
LDI data	$DP \leftarrow D_{6\text{-}0}$	Load DP with 7 bits of immediate data	0 0	0 D_6	0 D_5	1 D_4	0 D_3	1 D_2	0 D_1	1 D_0	2	2	
LDZ data	$DP_H \leftarrow 0$ $DP_L \leftarrow D_{3\text{-}0}$	Load DP_H with 0; Load DP_L with 4 bits of immediate data	1	0	0	0	D_3	D_2	D_1	D_0	1	1	
			STORE										
S	$(DP) \leftarrow A_{CC}$	Store A_{CC} into the RAM location addressed by DP	0	0	0	0	0	1	0	0	1	1	
			TRANSFER										
TAL	$DP_L \leftarrow A_{CC}$	Transfer A_{CC} to DP_L	0	0	0	0	0	1	1	1	1	1	
TLA	$A_{CC} \leftarrow DP_L$	Transfer DP_L to A_{CC}	0	0	0	1	0	0	1	0	1	1	
TAW	$W \leftarrow A_{CC}$	Transfer A_{CC} to W	0	1	0	0	0	0	1	1	1	2	
TAZ	$Z \leftarrow A_{CC}$	Transfer A_{CC} to Z	0	1	0	0	0	0	1	0	1	2	
THX	$X \leftarrow DP_H$	Transfer DP_H to X	0	1	0	0	0	1	1	1	1	2	
TLY	$Y \leftarrow DP_L$	Transfer DP_L to Y	0	1	0	0	0	1	1	0	1	2	
			EXCHANGE										
X	$A_{CC} \leftrightarrow (DP)$	Exchange A with the RAM contents addressed by DP	0	0	1	0	1	0	0	0	1	1	
XI	$A_{CC} \leftrightarrow (DP)$ $DP_L \leftarrow DP_L + 1$ Skip if $DP_L = 0H$	Exchange A_{CC} with RAM contents addressed by DP; increment DP_L; Skip if $DP_L = 0H$	0	0	1	1	1	1	0	0	1	1 + S	$DP_L = 0H$
XD	$A_{CC} \leftrightarrow (DP)$ $DP_L \leftarrow DP_L - 1$ Skip if $DP_L = FH$	Exchange A_{CC} with the RAM contents addressed by DP; decrement DP_L; Skip if $DP_L = FH$	0	0	1	0	1	1	0	0	1	1 + S	$DP_L = FH$
XM data	$A_{CC} \leftrightarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1\text{-}0}$	Exchange A_{CC} with the RAM contents addressed by DP; Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of immediate data; store the results in DP_H	0	0	1	0	1	0	D_1	D_0	1	1	
XMI data	$A_{CC} \leftrightarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1\text{-}0}$ $DP_L \leftarrow DP_L + 1$ Skip if $DP_L = 0H$	Exchange A_{CC} with the RAM contents addressed by DP; Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of immediate data; store the results in DP_H increment DP_L; Skip if $DP_L = 0H$	0	0	1	1	1	1	D_1	D_0	1	1 + S	$DP_L = 0H$
XMD data	$A_{CC} \leftrightarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1\text{-}0}$ $DP_L \leftarrow DP_L - 1$ Skip if $DP_L = FH$	Exchange A_{CC} with the RAM contents addressed by DP; Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of immediate data; store the results in DP_H decrement DP_L; Skip if $DP_L = FH$	0	0	1	0	1	1	D_1	D_0	1	1 + S	$DP_L = FH$
XAW	$A_{CC} \leftrightarrow W$	Exchange A_{CC} with W	0	1	0	0	1	0	1	1	1	2	
XAZ	$A_{CC} \leftrightarrow Z$	Exchange A_{CC} with Z	0	1	0	0	1	0	1	0	1	2	
XHR	$DP_H \leftrightarrow R$	Exchange DP_H with R	0	1	0	0	1	1	0	1	1	2	
XHX	$DP_H \leftrightarrow X$	Exchange DP_H with X	0	1	0	0	1	1	1	1	1	2	
XLS	$DP_L \leftrightarrow$ S Register	Exchange DP_L with S Register	0	1	0	0	1	1	0	0	1	2	
XLY	$DP_L \leftrightarrow Y$	Exchange DP_L with Y	0	1	0	0	1	1	1	0	1	2	
XC	$C \leftrightarrow C'$	Exchange Carry F/F with Carry Save F/F	0	0	0	1	1	0	1	0	1	1	

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								BYTES	CYCLES	SKIP CONDITION
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
ARITHMETIC													
AD	$A_{CC} \leftarrow A_{CC} + (DP)$ Skip if overflow	Add the RAM contents addressed by DP to A_{CC}; skip if overflow is generated	0	0	0	0	1	0	0	0	1	1 + S	Overflow
ADC	$A_{CC} \leftarrow A_{CC} + (DP) + C$ if overflow occurs, $C \leftarrow 1$	Add the RAM contents addressed by DP, and the Carry F/F to A_{CC}; if overflow occurs, set carry F/F	0	0	0	1	1	0	0	1	1	1	
ADS	$A_{CC} \leftarrow A_{CC} + (DP) + C$ if overflow occurs, $C \leftarrow 1$ and skip	Add the RAM contents addressed by DP and the carry F/F to A_{CC}; if overflow occurs, set Carry F/F and skip	0	0	0	0	1	0	0	1	1	1 + S	Overflow
DAA	$A_{CC} \leftarrow A_{CC} + 6$	Add 6 to A_{CC} to Adjust Decimal for BCD Addition	0	0	0	0	0	1	1	0	1	1	
DAS	$A_{CC} \leftarrow A_{CC} + 10$	Add 10 to A_{CC} to Adjust Decimal for BCD Subtraction	0	0	0	0	1	0	1	0	1	1	
LOGICAL													
EXL	$A_{CC} \leftarrow A_{CC} \forall (DP)$	Perform a LOGICAL EXCLUSIVE-OR between the RAM contents addressed by DP and A_{CC}; store the result in A_{CC}	0	0	0	1	1	0	0	0	1	1	
ACCUMULATOR													
CLA	$A_{CC} \leftarrow 0$	Clear A_{CC} to zero	1	0	0	1	0	0	0	0	1	1	String
CMA	$A_{CC} \leftarrow \overline{A_{CC}}$	Complement A_{CC}	0	0	0	1	0	0	0	0	1	1	
CIA	$A_{CC} \leftarrow \overline{A_{CC}} + 1$	Complement A; Increment A	0	0	0	1	0	0	0	1	1	1	
RAR	$A_{CC_{n-1}} \leftarrow A_{CC_n}$ $C \leftarrow A_{CC_0}$ $(n = 1 \rightarrow 3)$ $A_{CC_3} \leftarrow C$	Rotate A_{CC} right through Carry F/F	0	0	1	1	0	0	0	0	1	1	
CARRY FLAG													
CLC	$C \leftarrow 0$	Reset Carry F/F to zero	0	0	0	0	1	0	1	1	1	1	
STC	$C \leftarrow 1$	Set Carry F/F to one	0	0	0	1	1	0	1	1	1	1	
TC	Skip if C = 1	Skip if Carry F/F is true	0	0	0	0	0	1	0	0	1	1 + S	C = 1
FLAG													
SFB	$FLAG_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of FLAG Register to one	0	1	1	1	1	1	D_1	D_0	1	2	
RFB	$FLAG_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of FLAG Register to zero	0	1	1	0	1	1	D_1	D_0	1	2	
FBT	Skip if $FLAG_{bit} = 1$	Skip if a single bit (denoted by D_1D_0) of the FLAG Register is true	0	1	0	1	1	1	D_1	D_0	1	2 + S	$FLAG_{bit} = 1$
FBF	Skip if $FLAG_{bit} = 0$	Skip if a single bit (denoted by D_1D_0) of the FLAG Register is false	0	0	1	0	0	0	D_1	D_0	1	2 + S	$FLAG_{bit} = 0$
INCREMENT AND DECREMENT													
INC	$A_{CC} \leftarrow A_{CC} + 1$ Skip if overflow	Increment A; Skip if overflow is generated	0	0	0	0	1	1	0	1	1	1 + S	Overflow
DEC	$A_{CC} \leftarrow A_{CC} - 1$ Skip if underflow	Decrement A; Skip if underflow occurs	0	0	0	0	1	1	1	1	1	1 + S	Underflow
IND	$DP_L \leftarrow DP_L + 1$ Skip if $DP_L = 0H$	Increment DP_L; Skip if $DP_L = 0H$	0	0	1	1	0	0	1	1	1	1 + S	$DP_L = 0H$
DED	$DP_L \leftarrow DP_L - 1$ Skip if $DP_L = FH$	Decrement DP_L; Skip if $DP_L = FH$	0	0	0	1	0	0	1	1	1	1 + S	$DP_L = FH$
INM	$(DP) \leftarrow (DP) + 1$ Skip if $(DP) = 0H$	Increment the RAM contents addressed by DP; Skip if the contents = 0H	0	0	0	1	1	1	0	1	1	1 + S	$(DP) = 0H$
DEM	$(DP) \leftarrow (DP) - 1$ Skip if $(DP) = FH$	Decrement the RAM contents addressed by DP; skip if the contents = FH	0	0	0	1	1	1	1	1	1	1 + S	$(DP) = FH$

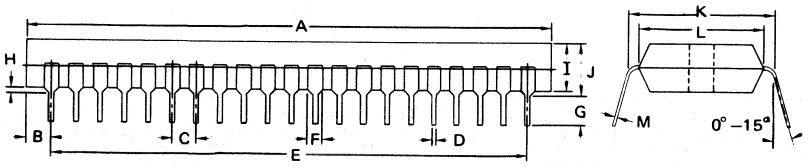
MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
BIT MANIPULATION													
RMB data	$(DP)_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1-D_0) of RAM at the location addressed by DP to zero	0	1	1	0	1	0	D_1	D_0	1	1	
SMB data	$(DP)_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of RAM at the location addressed by DP to one	0	1	1	1	1	0	D_1	D_0	1	1	
REB data	$PE_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of output Port E to zero	0	1	1	0	0	1	D_1	D_0	1	2	
SEB data	$PE_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of output Port E to one	0	1	1	1	0	1	D_1	D_0	1	2	
RPB data	$P(DP_L)_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of the output port addressed by DP_L to zero	0	1	1	0	0	0	D_1	D_0	1	1	
SPB data	$P(DP_L)_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of the output port addressed by DP_L	0	1	1	1	0	0	D_1	D_0	1	1	
JUMP, CALL AND RETURN													
JMP address	$P_{10\text{-}0} \leftarrow D_{10\text{-}0}$	Jump to the address specified by 11 bits of immediate data	1 D_7	0 D_6	1 D_5	0 D_4	0 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	2	2	
JCP address	$P_{5\text{-}0} \leftarrow D_{5\text{-}0}$	Jump to the address within the current ROM page specified by 6 bits of immediate data	1	1	D_5	D_4	D_3	D_2	D_1	D_0	1	1	
JPA	$P_{5\text{-}2} \leftarrow A_{CC}$ $P_{1\text{-}0} \leftarrow 00$	Jump to the address within the current ROM page modified by A_{CC}	0	1	0	0	0	0	0	1	1	2	
CAL address	Stack $\leftarrow$ P + 2 $P_{10\text{-}0} \leftarrow D_{10\text{-}0}$	Store a return address (P + 2) in the stack; call the subroutine program at the location specified by 11 bits of immediate data	1 D_7	0 D_6	1 D_5	0 D_4	1 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	2	2	
CZP address	Stack $\leftarrow$ P + 1 $P_{10\text{-}6} \leftarrow 00000$ $P_{5\text{-}2} \leftarrow D_{3\text{-}0}$ $P_{1\text{-}0} \leftarrow 00$	Store a return address (P + 1) in the stack; call the subroutine program at one of sixteen locations in Page 0 of Field 0, specified by 4 bits of immediate data	1	0	1	1	D_3	D_2	D_1	D_0	1	1	
RT	P $\leftarrow$ Stack	Return from Subroutine	0	1	0	0	1	0	0	0	1	2	
RTS	P $\leftarrow$ Stack Skip unconditionally	Return from Subroutine; skip unconditionally	0	1	0	0	1	0	0	1	1	2 + S	Unconditional
SKIP													
CI data	Skip if $A_{CC} = D_{3\text{-}0}$	Skip if A_{CC} equals 4 bits of immediate data	0 1	0 1	0 0	1 0	0 D_3	1 D_2	1 D_1	1 D_0	2	2 + S	$A_{CC} = D_{3\text{-}0}$
CM	Skip if $A_{CC} = (DP)$	Skip if A_{CC} equals the RAM contents addressed by DP	0	0	0	0	1	1	0	0	1	1 + S	$A_{CC} = (DP)$
CMB data	Skip if $A_{CC_{bit}} = (DP)_{bit}$	Skip if the single bit (denoted by D_1D_0) of A_{CC}, is equal to the single bit (also denoted by D_1D_0) of RAM addressed by DP	0	0	1	1	0	1	D_1	D_0	1	1 + S	$A_{CC_{bit}} = (DP)_{bit}$
TAB data	Skip if $A_{CC_{bit}} = 1$	Skip if the single bit (denoted by D_1D_0) of A_{CC} is true	0	0	1	0	0	1	D_1	D_0	1	1 + S	$A_{CC_{bit}} = 1$
CLI data	Skip if $DP_L = D_{3\text{-}0}$	Skip if DP_L equals 4 bits of immediate data	0 1	0 1	0 1	1 0	0 D_3	1 D_2	1 D_1	0 D_0	2	2 + S	$DP_L = D_{3\text{-}0}$
TMB data	Skip if $(DP)_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by DP is true	0	1	0	1	1	0	D_1	D_0	1	1 + S	$(DP)_{bit} = 1$
TPA data	Skip if $PA_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of Port A is true	0	1	0	1	0	1	D_1	D_0	1	2 + S	$PA_{bit} = 1$
TPB data	Skip if $P(DP_L)_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of the input Port addressed by DP_L is true	0	1	0	1	0	0	D_1	D_0	1	1 + S	$P(DP_L)_{bit} = 1$
STM	TIMER F/F $\leftarrow$ 0 TC $\leftarrow D_{5\text{-}0}$	Reset Timer F/F to zero; Load Timer Counter with 6 bits of immediate data; Start timer	0 1	0 0	0 D_5	1 D_4	0 D_3	1 D_2	0 D_1	0 D_0	2	2	
TTM	Skip if TIMER F/F = 1	Skip if Timer F/F is true	0	0	0	0	0	1	0	1	1	1 + S	TIMER F/F = 1

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
INTERRUPT													
TIT	Skip if INT F/F = 1	Skip if Interrupt F/F is true; Reset Interrupt F/F	0	0	0	0	0	0	1	1	1	1 + S	INT F/F = 1
EI	INTE F/F ← 1	Set Interrupt Enable F/F to one; Enable Interrupt	0	0	1	1	0	0	0	1	1	1	
DI	INTE F/F ← 0	Reset Interrupt Enable F/F to zero; Disable Interrupt	0	0	0	0	0	0	0	1	1	1	
PARALLEL I/O													
IA	$A_{CC} \leftarrow PA$	Input Port A to A_{CC}	0	1	0	0	0	0	0	0	1	2	
IP	$A_{CC} \leftarrow P(DP_L)$	Input the Port addressed by DP_L to A_{CC}	0	0	1	1	0	0	1	0	1	1	
OE	$PE \leftarrow A_{CC}$	Output A_{CC} to Port E	0	1	0	0	0	1	0	0	1	2	
OP	$P(DP_L) \leftarrow A_{CC}$	Output A_{CC} to the port addressed by DP_L	0	0	0	0	1	1	1	0	1	1	
OCD	$PD_{3-0} \leftarrow D_{7-4}$ $PC_{3-0} \leftarrow D_{3-0}$	Output 8 bits of immediate data to Ports C and D	0 D_7	0 D_6	0 D_5	1 D_4	1 D_3	1 D_2	1 D_1	0 D_0	2	2	
CPU CONTROL													
NOP		Perform no operation; consume one machine cycle	0	0	0	0	0	0	0	0	1	1	

6

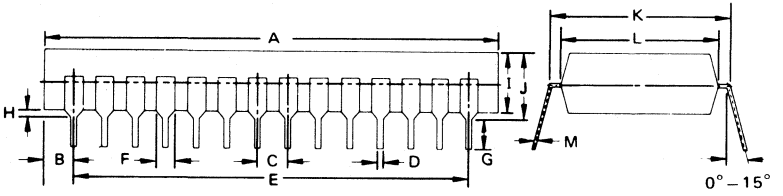
PACKAGE OUTLINES



42-PIN DIP
μPD546C
μPD547C
μPD547LC
μPD552C
μPD553C
μPD650C
μPD651C

Plastic

ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

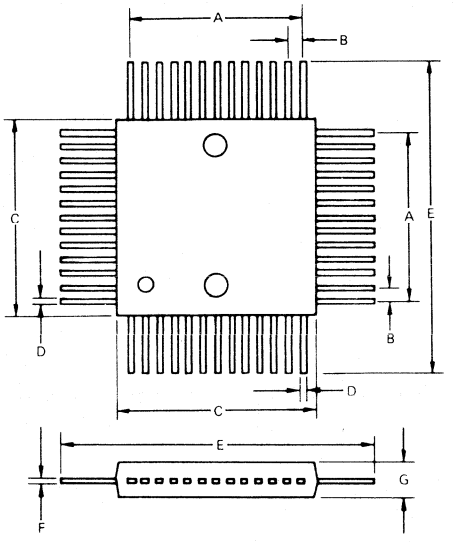


28-PIN DIP
μPD550C
μPD550LC
μPD554C
μPD554LC
μPD557LC
μPD652C

Plastic

ITEM	MILLIMETERS	INCHES
A	38.0 MAX	1.496 MAX
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

52-PIN FLAT PLASTIC
PACKAGE
μPD651G



PLASTIC

ITEM	MILLIMETERS	INCHES
A	12.0 MAX	0.47 MAX
B	1.0 ± 0.1	0.04 ± 0.004
C	14.0	0.55
D	0.4	0.016
E	21.8 ± 0.4	0.86 ± 0.016
F	0.15	0.006
G	2.6	0.1

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4-BIT SINGLE CHIP MICROCOMPUTERS

DESCRIPTION

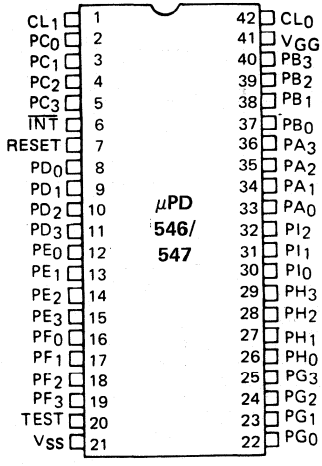
The μPD546 and the μPD547 are pin-compatible 4-bit single chip microcomputers which have similar architectures.

The μPD546 contains a 2000 x 8-bit ROM, and a 96 x 4-bit RAM which includes six working registers and the Flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit timer. The μPD546 executes all 80 instructions of the extended μCOM-4 family instruction set.

The μPD547 contains a 1000 x 8-bit ROM and a 64 x 4-bit RAM. It has a testable interrupt input $\overline{INT}$, a single-level stack, and executes all 58 instructions of the μCOM-4 family instruction set. The μPD547 is upward compatible with the μPD546.

Both the μPD546 and the μPD547 provide 35 I/O lines organized into the 4-bit input Ports A and B, the 4-bit I/O Ports C and D, the 4-bit output Ports E, F, G, and H, and the 3-bit output Port I. Both devices typically execute their instructions with a 10 μs instruction cycle time. The μPD546 and the μPD547 are manufactured with a standard PMOS process, allowing use of a single −10V power supply, and are available in a 42-pin dual-in-line plastic package.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage, V_{GG}	−15 to +0.3V
Input Voltages	−15 to +0.3V
Output Voltages	−15 to +0.3V
Output Current (Ports C through I, each bit)	−4 mA
(Total, all ports)	−25 mA

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.0	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL}	−4.3		V_{GG}	V	Ports A through D, $\overline{INT}$, RESET
Clock Voltage High	$V_{\phi H}$	0		−0.8	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -1V$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -11V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -11V$
Output Voltage High	V_{OH_1}			−1.0	V	Ports C through I, $I_{OH} = -1.0$ mA
	V_{OH_2}			−2.3	V	Ports C through I, $I_{OH} = -3.3$ mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C through I, $V_O = -11V$
Supply Current	I_{GG}		−30	−50	mA	

CAPACITANCE

$T_a = 25°C$

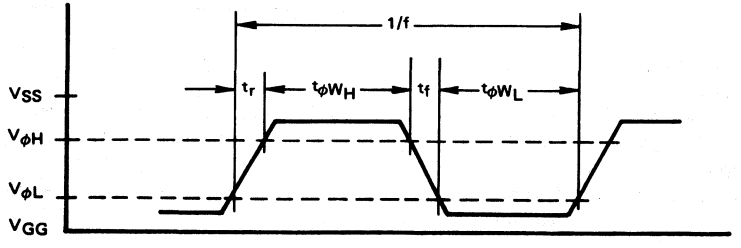
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM



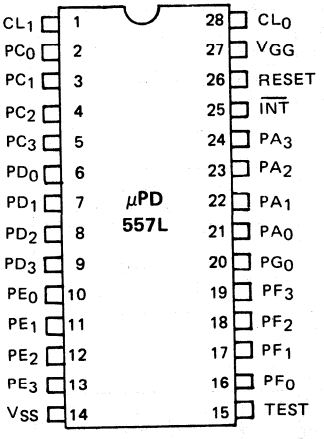
4-BIT SINGLE CHIP MICROCOMPUTER WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

DESCRIPTION

The μPD557L is a 4-bit single chip microcomputer which has the same architecture as the μPD553, but is pin-compatible with the μPD550L and the μPD554L. The μPD557L contains a 2000 x 8-bit ROM and a 96 x 4-bit RAM, which includes six working registers and the FLAG register. It has a lever-triggered hardware interrupt input $\overline{INT}$, a three-level stack and a 6-bit programmable timer. The μPD557L provides 21 I/O lines, organized into the 4-bit input port A, the 4-bit I/O ports C and D, and the 4-bit output ports E and F, and the 1-bit output port G. The 17 I/O ports and output ports are capable of being pulled to −35V in order to drive Vacuum Fluorescent Displays directly. The μPD557L typically executes all 80 instructions of the extended μCOM-4 family instruction set with a 25 μs instruction cycle time. It is manufactured with a modified PMOS process, allowing use of a single −8V power supply and is available in a 28-pin dual-in-line plastic package.

The μPD550L and the μPD554L are upward-compatible with the μPD557L.

PIN CONFIGURATION



PIN NAMES

PA_0–PA_3	Input Port A
PC_0–PC_3	Input/Output Port C
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
PG_0	Output Port G
$\overline{INT}$	Interrupt Input
CL_0–CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature		−10°C to +70°C
Storage Temperature		−40°C to +125°C
Supply Voltage, V_{GG}		−15 to +0.3V
Input Voltages	(Port A, $\overline{INT}$, RESET)	−15 to +0.3V
	(Ports C, D)	−40 to +0.3V
Output Voltages		−40 to +0.3V
Output Current	(Ports C, D, each bit)	−4 mA
	(Ports E, F, G, each bit)	−25 mA
	(Total, all ports)	−100 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -8.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.5	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−6.5		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−6.5		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -9V$
	I_{LIL_2}			−30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -9V$
Output Voltage High	V_{OH_1}			−1.0	V	Ports C through G, $I_{OH} = -2$ mA
	V_{OH_2}			−4.0	V	Ports E, F, G, $I_{OH} = -20$ mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, $V_O = -9V$
	I_{LOL_2}			−30	μA	Ports C through G, $V_O = -35V$
Supply Current	I_{GG}		−20	−36	mA	

CAPACITANCE

$T_a = 25°C$

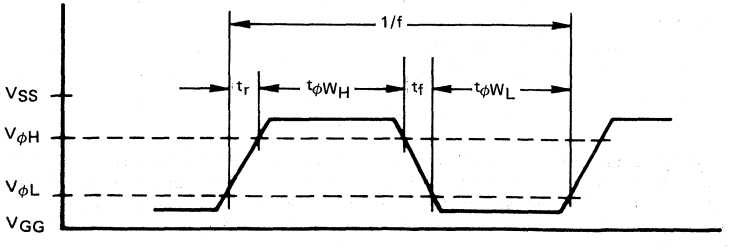
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -8.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	100		180	kHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	2.0		8.0	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	2.0		8.0	μs	

CLOCK WAVEFORM



CMOS 4-BIT SINGLE CHIP MICROCOMPUTERS

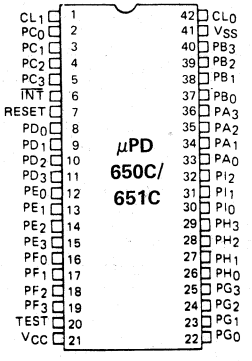
DESCRIPTION

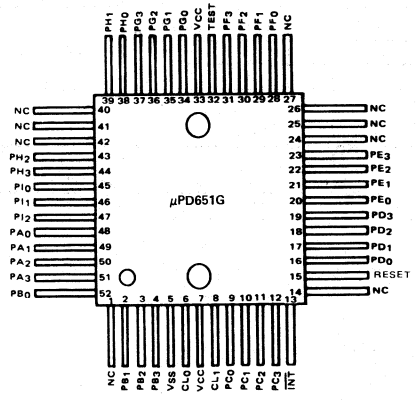
The μPD650 and the μPD651 are pin-compatible CMOS 4-bit single chip microcomputers which have similar architectures.

The μPD650 contains a 2000 x 8-bit ROM, and a 96 x 4-bit RAM which includes six working registers and the Flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit Timer. The μPD650 executes all 80 instructions of the extended μCOM-4 family instruction set. The μPD651 contains a 1000 x 8-bit ROM and a 64 x 4-bit RAM. It has a testable interrupt input $\overline{INT}$, a two-level stack, and executes all 58 instructions of the μCOM-4 family instruction set. The μPD651 is upward-compatible with the μPD650.

Both the μPD650 and the μPD651 provide 35 I/O lines, organized into the 4-bit input ports A and B, the 4-bit I/O ports C and D, the 4-bit output ports E, F, G, and H, and the 3-bit output port I. Both devices typically execute their instructions with a 10 μs instruction cycle time. The μPD650 and the μPD651 are manufactured with a standard CMOS process, allowing use of a single +5V power supply, and are available in a 42-pin Dual-in-line plastic package. The μPD651 is also available in a space-saving 52-pin flat plastic package.

PIN CONFIGURATION





PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{CC}	Power Supply Positive
V_{SS}	Ground
TEST	Factory Test Pin (Connect to V_{CC})
NC	No Connection

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -30°C to +85°C
Storage Temperature . . . . . -55°C to +125°C
Supply Voltage, V_{CC} . . . . . -0.3 to +7.0V
Input Voltages (Ports A through D, $\overline{INT}$, RESET) . . . . . -0.3 to V_{CC} +0.3V
Output Voltages . . . . . -0.3 to V_{CC} +0.3V
Output Current (Ports C through I, each bit) . . . . . 2.5 mA
T_a = 25°C (Total, all ports) . . . . . 28 mA

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = -30°C to +85°C; V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0.7 V_{CC}		V_{CC}	V	Ports A through D, $\overline{INT}$ RESET
Input Voltage Low	V_{IL}	0		0.3 V_{CC}	V	Ports A through D, $\overline{INT}$ RESET
Clock Voltage High	$V_{\phi H}$	0.7 V_{CC}		V_{CC}	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	0		0.3 V_{CC}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$ RESET, V_I = V_{CC}
Input Leakage Current Low	I_{LIL}			-10	μA	Ports A through D, $\overline{INT}$, RESET, V_I = 0V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H}$ = V_{CC}
Clock Input Leakage Current Low	$I_{L\phi L}$			-200	μA	CL_0 Input, $V_{\phi L}$ = 0V
Output Voltage High	V_{OH_1}	V_{CC} -0.5			V	Ports C through I, I_{OH} = -1.0 mA
	V_{OH_2}	V_{CC} -2.5			V	Ports C through I, I_{OH} = -2.0 mA
Output Voltage Low	V_{OL_1}			+0.6	V	Ports E through I, I_{OL} = +2.0 mA
	V_{OL_2}			+0.4	V	Ports E through I, I_{OL} = +1.2 mA
Output Leakage Current Low	I_{LOL}			-10	μA	Ports C, D, V_O = 0V
Supply Current	I_{CC}		+0.8	+2.0	mA	

CAPACITANCE

T_a = 25°C

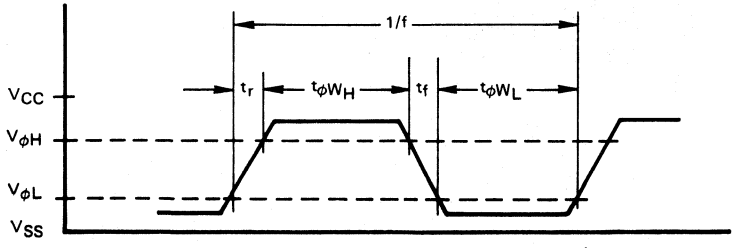
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

T_a = -30°C to +85°C; V_{CC} = +5 ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM



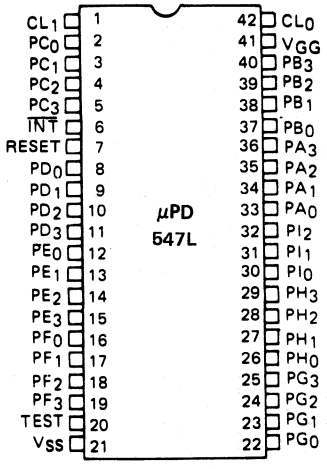
4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD547L is a 4-bit single chip microcomputer which has the same architecture as the μPD547. It contains a 1000 x 8-bit ROM, a 64 x 4-bit RAM, a testable interrupt input $\overline{INT}$ and a single-level stack.

The μPD547L provides 35 I/O lines, organized into the 4-bit input ports A and B, the 4-bit I/O ports C and D, the 4-bit output ports, E, F, G, and H, and the 3-bit output port I. The μPD547L typically executes all 58 instructions of the μCOM-4 family instruction set with a 25 μs instruction cycle time. It is manufactured with a modified PMOS process, allowing use of a single −8V power supply, and is available in a 42-pin dual-in-line plastic package.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage, V_{GG}	−15 to +0.3V
Input Voltages	−15 to +0.3V
Output Voltages	−15 to +0.3V
Output Current (Ports C through I, each bit)	−4 mA
(Total, all ports)	−25 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −8V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−1.6	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL}	−3.8		V_{GG}	V	Ports A through D, $\overline{INT}$, RESET
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, V_I = −1V
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A through D, $\overline{INT}$, RESET, V_I = −9V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H}$ = 0V
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = −9V
Output Voltage High	V_{OH_1}			−1.0	V	Ports C through I, I_{OH} = −1.0 mA
	V_{OH_2}			−2.3	V	Ports C through I, I_{OH} = −3.3 mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C through I, V_O = −9V
Supply Current	I_{GG}		−15	−25	mA	

CAPACITANCE

T_a = 25°C

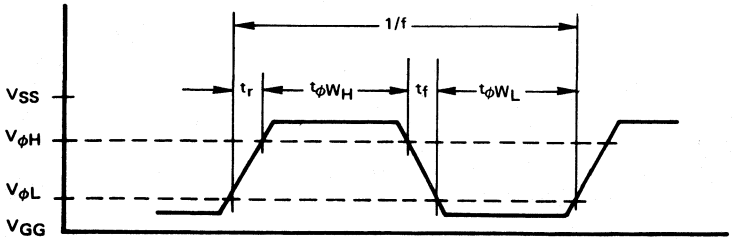
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −8V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	100		180	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	2.0		8.0	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	2.0		8.0	μs	

CLOCK WAVEFORM



547LS-REV1-1-82-CAT

4-BIT SINGLE CHIP MICROCOMPUTERS WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

DESCRIPTION

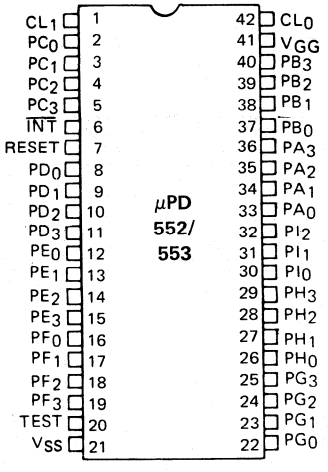
The μPD552 and the μPD553 are pin-compatible 4-bit single chip microcomputers which have similar architectures.

The μPD552 contains a 1000 x 8-bit ROM and a 64 x 4-bit RAM. It has a testable interrupt input $\overline{INT}$, a single-level stack, and executes all 58 instructions of the μCOM-4 family instruction set. The μPD552 is upward compatible with the μPD553.

The μPD553 contains a 2000 x 8-bit ROM, and a 96 x 4-bit RAM which includes six working registers and the Flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit Timer. The μPD553 executes all 80 instructions of the extended μCOM-4 family instruction set.

Both the μPD552 and the μPD553 provide 35 I/O lines organized into the 4-bit input Ports A and B, the 4-bit I/O Ports C and D, the 4-bit output Ports E, F, G, and H, and the 3-bit output Port I. The 27 I/O ports and output ports are capable of being pulled to −35V in order to drive Vacuum Fluorescent Displays directly. Both devices typically execute their instructions with a 10 μs instruction cycle time. The μPD552 and the μPD553 are manufactured with a standard PMOS process, allowing use of a single −10V power supply, and are available in a 42-pin dual-in-line plastic package.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
Supply Voltage, V_{GG} . . . . . −15 to V
Input Voltages (Port A, B, $\overline{INT}$, RESET) . . . . . −15 to +0.3V
(Ports C, D) . . . . . −40 to +0.3V
Output Voltages . . . . . −40 to +0.3V
Output Current (Ports C through I, each bit) . . . . . −12 mA
(Total, all ports) . . . . . −60 mA

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−3.5	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−7.5		V_{GG}	V	Ports A, B, $\overline{INT}$, RESET
	V_{IL_2}	−7.5		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.8	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -11V$
	I_{LIL_2}			−30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -11V$
Output Voltage High	V_{OH}			−2.0	V	Ports C through I, $I_{OH} = -8$ mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through I, $V_O = -11V$
	I_{LOL_2}			−30	μA	Ports C through I, $V_O = -35V$
Supply Current	I_{GG}		−30	−50	mA	

CAPACITANCE

$T_a = 25°C$

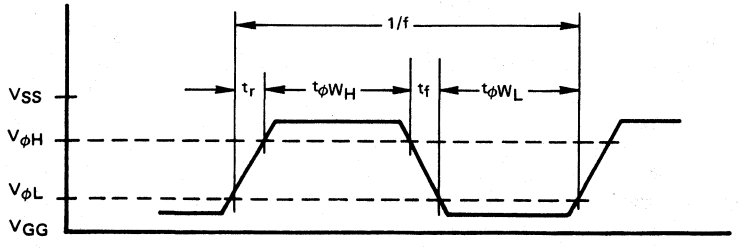
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM

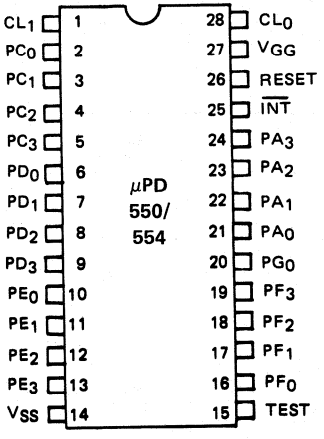


4-BIT SINGLE CHIP MICROCOMPUTERS WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

DESCRIPTION

The μPD550 and the μPD554 are pin-compatible 4-bit single chip microcomputers which have the same architecture. The only difference between them is that the μPD550 contains a 640 x 8-bit ROM, whereas the μPD554 contains a 1000 x 8-bit ROM. Both devices have a 32 x 4-bit RAM, a testable interrupt input $\overline{INT}$, and a single-level stack. The μPD550 and the μPD554 provide 21 I/O lines organized into the 4-bit input port A, the 4-bit I/O ports C and D, the 4-bit output ports E and F, and the 1-bit output port G. The 17 I/O ports and output ports are capable of being pulled to −35V in order to drive Vacuum Fluorescent Displays directly. The μPD550 and the μPD554 typically execute all 58 instructions of the μCOM-4 family instruction set with a 10 μs instruction cycle time. Both devices are manufactured with a standard PMOS process, allowing use of a single −10V power supply, and are available in a 28 pin dual-in-line plastic package.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
CL_0-CL_1	External Clock Signals
$\overline{INT}$	Interrupt Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

6

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage, V_{GG}	−15 to +0.3V
Input Voltages (Port A, $\overline{INT}$, RESET)	−15 to +0.3V
(Ports C, D)	−40 to +0.3V
Output Voltages	−40 to +0.3V
Output Current (Ports C, D, each bit)	−4 mA
(Ports E, F, G, each bit)	−15 mA
(Total, all ports)	−60 mA

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.0	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−4.3		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−4.3		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -11V$
	I_{LIL_2}			−30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -11V$
Output Voltage High	V_{OH_1}			−1.0	V	Ports C, D, $I_{OH} = -2$ mA
	V_{OH_2}			−2.5	V	Ports E, F, G, $I_{OH} = -10$ mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, $V_O = -11V$
	I_{LOL_2}			−30	μA	Ports C through G, $V_O = -35V$
Supply Current	I_{GG}		−20	−40	mA	

CAPACITANCE

$T_a = 25°C$

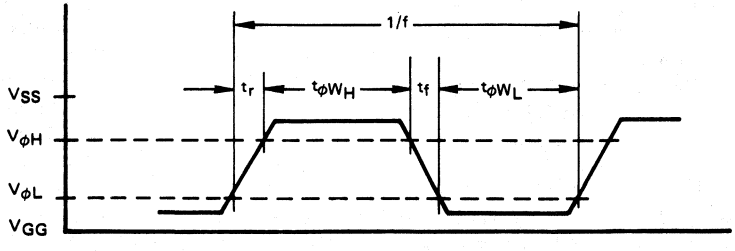
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM



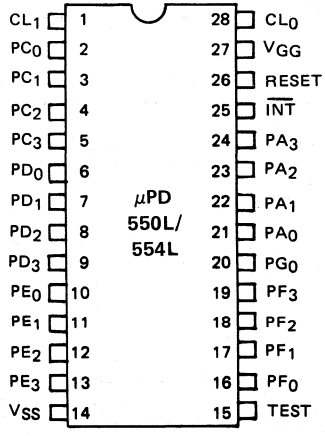
4-BIT SINGLE CHIP MICROCOMPUTERS WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

DESCRIPTION

The μPD550L and the μPD554L are pin-compatible 4-bit single chip microcomputers which have the same architecture. The only difference between them is that the μPD550L contains a 640 x 8-bit ROM, whereas the μPD554L contains a 1000 x 8-bit ROM. Both devices have a 32 x 4-bit RAM, a testable interrupt input $\overline{INT}$, and a single-level stack. The μPD550L and the μPD554L provide 21 I/O lines organized into the 4-bit input port A, the 4-bit I/O ports C and D, the 4-bit output ports E and F, and the 1-bit output port G. The 17 I/O ports and output ports are capable of being pulled to −35V in order to drive Vacuum Fluorescent Displays directly. The μPD550L and the μPD554L typically execute all 58 instructions of the μCOM-4 family instruction set with a 25 μs instruction cycle time. Both devices are manufactured with a modified PMOS process, allowing use of a single −8V power supply, and are available in a 28-pin dual-in-line plastic package.

The μPD550L and the μPD554L are upward compatible with the μPD557L.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
CL_0-CL_1	External Clock Signals
$\overline{INT}$	Interrupt Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage, V_{GG}	−15 to +0.3V
Input Voltages (Port A, $\overline{INT}$, RESET)	−15 to +0.3V
(Ports C, D)	−40 to +0.3V
Output Voltages	−40 to +0.3V
Output Current (Ports C, D, each bit)	−4 mA
(Ports E, F, G, each bit)	−15 mA
(Total, all ports)	−60 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −8.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−1.6	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−4.5		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−4.5		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −1V
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −9V
	I_{LIL_2}			−30	μA	Ports C, D, V_I = −35V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H}$ = 0V
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = −9V
Output Voltage High	V_{OH_1}			−1.0	V	Ports C, D, I_{OH} = −2 mA
	V_{OH_2}			−2.5	V	Ports E, F, G, I_{OH} = −10 mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, V_O = −9V
	I_{LOL_2}			−30	μA	Ports C through G, V_O = −35V
Supply Current	I_{GG}		−12	−24	mA	

CAPACITANCE

T_a = 25°C

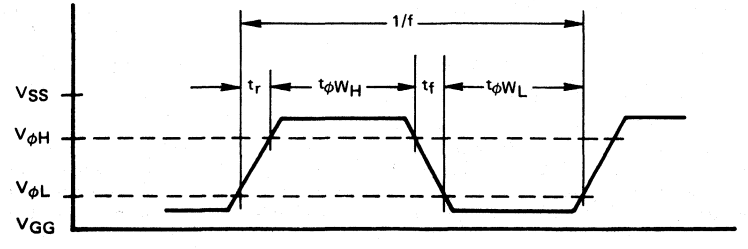
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −8.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	100		180	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	2.0		8.0	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	2.0		8.0	μs	

CLOCK WAVEFORM

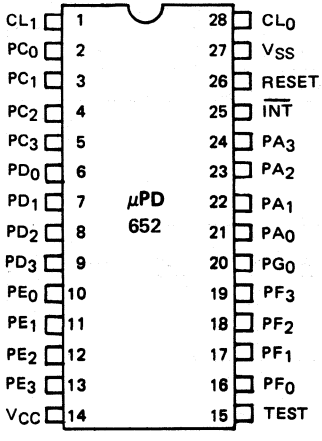


CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μPD652 is a CMOS 4-bit single chip microcomputer having the same architecture as the μPD554. It contains a 1000 x 8-bit ROM, a 32 x 4-bit RAM, a testable interrupt input $\overline{INT}$, and a single-level stack. The μPD652 provides 21 I/O lines, organized into the 4-bit input port A, the 4-bit I/O ports C and D, the 4-bit output ports E and F, and the 1-bit output port G. The μPD652 typically executes all 58 instructions of the μCOM-4 family instruction set with a 10 μs instruction cycle time. It is manufactured with a standard CMOS process, allowing use of a single +5V power supply, and is available in a 28-pin Dual-in-line plastic package.

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{CC}	Power Supply Positive
V_{SS}	Power Supply Negative
TEST	Factory Test Pin (Connect to V_{CC})

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−30°C to +85°C
Storage Temperature	−55°C to +125°C
Supply Voltage, V_{CC}	−0.3 to 7.0V
Input Voltages (Ports A, C, D, $\overline{INT}$, RESET)	−0.3 to V_{CC} +0.3V
Output Voltages	−0.3 to V_{CC} +0.3V
Output Current (Ports C through G, each bit)	−2.5 mA
(Total, all ports)	−28.0 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −30°C to +85°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0.7 V_{CC}		V_{CC}	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL}	0		0.3 V_{CC}	V	Ports A, C, D, $\overline{INT}$, RESET
Clock Voltage High	$V_{\phi H}$	0.7 V_{CC}		V_{CC}	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	0		0.3 V_{CC}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET, $V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET, V_I = 0V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = V_{CC}$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = 0V
Output Voltage High	V_{OH_1}	V_{CC}−0.5			V	Ports C through G, I_{OH} = −1.0 mA
	V_{OH_2}	V_{CC}−2.5			V	Ports C through G, I_{OH} = −2.0 mA
Output Voltage Low	V_{OL_1}			+0.6	V	Ports E, F, G, I_{OL} = +2.0 mA
	V_{OL_2}			+0.4	V	Ports E, F, G, I_{OL} = +1.2 mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C, D, V_O = 0V
Supply Current	I_{CC}		+0.8	+2.0	mA	

CAPACITANCE

T_a = 25°C

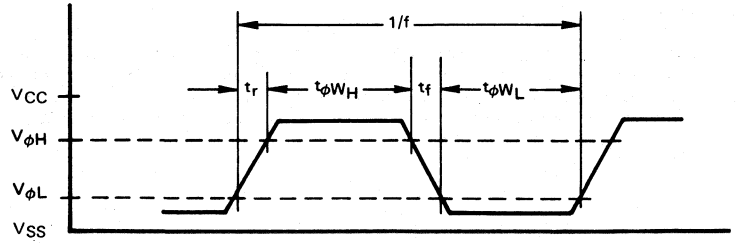
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

T_a = −30°C to +85°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	kHz	External Clock
Rise and Fall Times	t_r, t_f	0		0.3	μs	
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM



μCOM-4 4-BIT SINGLE CHIP ROM-LESS EVALUATION CHIP

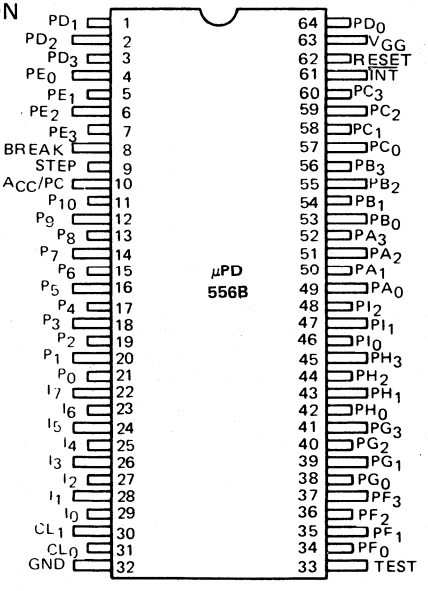
DESCRIPTION

The μPD556B is the ROM-less evaluation chip for the μCOM-4 4-bit single chip microcomputer family. The μPD556B is used in conjunction with an external 2048 x 8-bit program memory, such as the μPD2716 UV EPROM, to emulate each of the 14 different μCOM-4 single chip microcomputers.

The μPD556B contains a 96 x 4-bit RAM, which includes six working registers and the Flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit timer. The μPD556B executes all 80 instructions of the extended μCOM-4 family instruction set.

The μPD556B provides 35 I/O lines organized into the 4-bit input Ports A and B, the 4-bit I/O Ports C and D, the 4-bit output Ports E, F, G, and H, and the 3-bit output Port I. It typically executes its instructions with a 10μs instruction cycle time. The μPD556B is manufactured with a standard PMOS process, allowing use of a single −10V power supply, and is available in a 64-pin quad-in-line ceramic package.

PIN CONFIGURATION

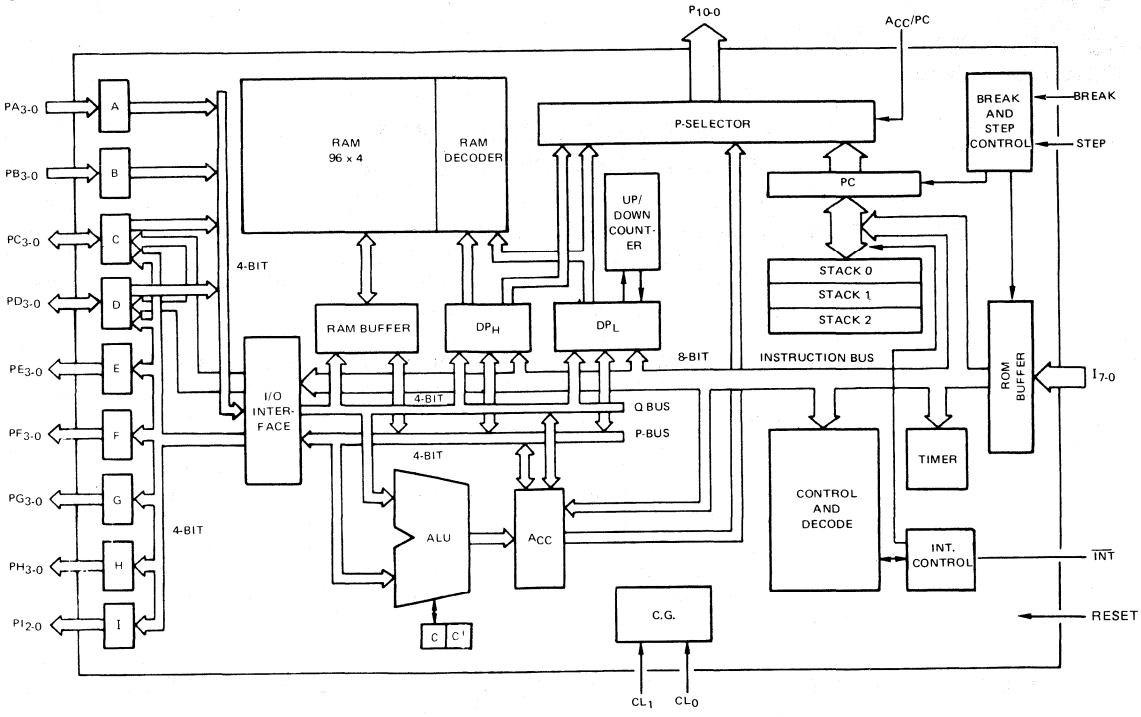


PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
I_{0-7}	Instruction Input
PC_{0-10}	Program Counter Output
A_{CC}/PC	Accumulator/Program Counter Select
BREAK	Break Input
STEP	Single Step Input
CL_0-CL_1	External Clock Source
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

6

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage, V_{GG}	−15V to +0.3V
All Input Voltages	−15V to +0.3V
All Output Voltages	−15V to +0.3V
Output Current (total, all ports)	−4 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		−2.0	V	Ports A to D, I_{7-0} BREAK, STEP, $\overline{INT}$, RESET, and A_{CC}/PC
Input Low Voltage	V_{IL}	−4.3		V_{GG}	V	Ports A to D, I_{7-0} BREAK, STEP, $\overline{INT}$, RESET, and A_{CC}/PC
Clock High Voltage	$V_{\phi H}$	0		−0.8	V	CL_0 Input, External Clock
Clock Low Voltage	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A and B, I_{7-0} $\overline{INT}$, RESET, BREAK, STEP, A_{CC}/PC, V_I = −1V
				+10	μA	Ports C and D, V_I = −1V
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A and B, I_{7-0} $\overline{INT}$, RESET, BREAK, STEP, A_{CC}/PC, V_I = −11V
				−10	μA	Ports C and D, V_I = −11V
Clock Input Leakage High	$I_{L\phi H}$			+200	μA	CL_0 Input, External Clock, $V_{\phi H}$ = 0V
Clock Input Leakage Low	$I_{L\phi L}$			−200	μA	CL_0 Input, External Clock, $V_{\phi L}$ = −11V
Output High Voltage	V_{OH1}			−1.0	V	Ports C to I, P_{10-0} I_{OH} = −1.0 mA
	V_{OH2}			−2.3	V	Ports C to I, P_{10-0} I_{OH} = −3.3 mA
Output Leakage Current Low	I_{LOL}			−30	μA	Ports C to I, P_{10-0} V_O = −11V
Supply Current	I_{GG}		−30	−50	mA	

AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −10V ± 10%

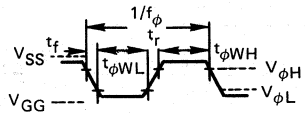
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Frequency	f_ϕ	150		440	KHz	
Clock Rise and Fall Times	t_r, t_f	0		0.3	μs	
Clock Pulse Width High	$t_{\phi WH}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi WL}$	0.5		5.6	μs	
Input Setup Time	t_{IS}			5	μs	
Input Hold Time	t_{IH}	0			μs	
BREAK to STEP Interval	t_{BS}	200			μs	f = 400 KHz, "1" Written
STEP to RUN Interval	t_{SB}	200			μs	f = 400 KHz, "1" Written
STEP Pulse Width	t_{WS}	30			μs	f = 400 KHz, "1" Written
BREAK to A_{CC} Interval	t_{BA}	200			μs	f = 400 KHz, "1" Written
A_{CC}/PC Pulse Width	t_{WA}	30			μs	f = 400 KHz, "1" Written
STEP to A_{CC} Interval	t_{SA1}	200			μs	f = 400 KHz, "1" Written
PC to STEP Overlap	t_{SA2}			5	μs	f = 400 KHz, "1" Written
PC to RUN Interval	t_{AB}	0			μs	f = 400 KHz, "1" Written
A_{CC}/PC → P_{10-0} Delay	t_{DAP1}			15	μs	f = 400 KHz, "1" Written
	t_{DAP2}			15	μs	f = 400 KHz, "1" Written

CAPACITANCE

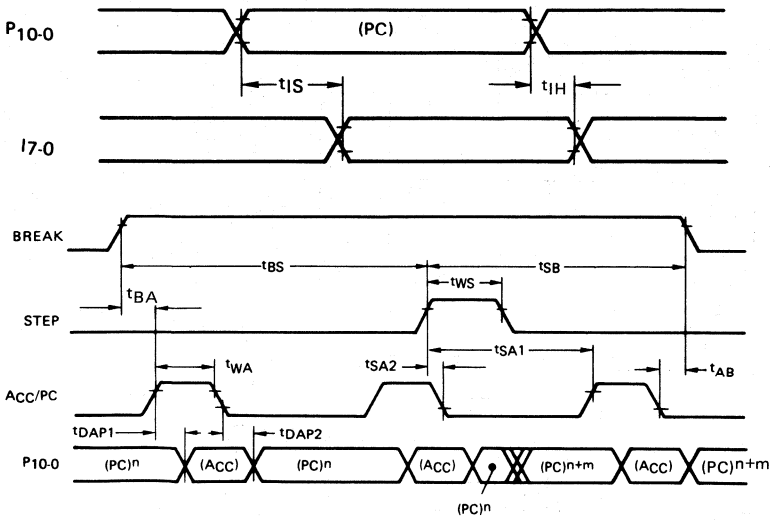
T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

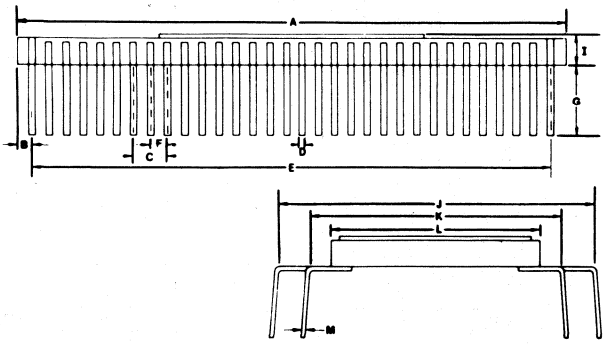
CLOCK WAVEFORM



TIMING WAVEFORMS



PACKAGE OUTLINE μPD556B



CERAMIC

ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002

μPD7500 SERIES CMOS 4-BIT SINGLE CHIP MICROCOMPUTER FAMILY

Description

The μPD7500 Series CMOS 4-Bit Single Chip Microcomputer Family is a broad product line of 10 individual devices designed to fulfill a wide variety of applications. The advanced 4th generation architecture includes all of the functional blocks necessary for a single chip controller, including an ALU, Accumulator, Program Memory (ROM), Data Memory (RAM), four General Purpose Registers, Stack Pointer, Program Status Word (PSW), 8-Bit Timer/Event Counter, Interrupt Controller, Display Controller/Driver, and 8-Bit Serial Interface. The instruction set maximizes the efficient utilization of fixed Program Memory space, and includes a variety of addressing, Table-Look-up, Logical, Single Bit Manipulation, vectored jump, and Condition Skip Instructions.

The μPD7500 Series includes three different devices, the μPD7501, μPD7502, and μPD7503, capable of directly driving Liquid Crystal Displays with up to 12 7-segment digits. The μPD7508A can directly drive up to 35V Vacuum Fluorescent Displays with up to 8 7-segment digits, and the μPD7519 can directly drive up to 35V Vacuum Fluorescent Displays with up to 16 7-segment digits.

All 10 devices are manufactured with a Silicon gate CMOS process, consuming only 900μA max at 5V, and only 400μA max at 3V. The HALT and STOP power-down instructions can significantly reduce power consumption even further.

The flexibility and the wide variety of μPD7500 Series devices available make the μPD7500 series ideally suited for a wide range of battery-powered, solar-powered, and portable products, such as telecommunication devices, hand-held instruments and meters, automotive products, industrial controls, energy management systems, medical instruments, portable terminals, portable measuring devices, appliances, and consumer products.

Features

- ☐ Advanced 4th Generation Architecture
- ☐ Choice of 8-Bit Program Memory (ROM) size:
  - 1K, 2K, 4K internal, or 8K external bytes
- ☐ Choice of 4-Bit Data Memory (RAM) size:
  - 64, 96, 128, 208, 224, or 256 internal nibbles
- ☐ RAM Stack
- ☐ Four General Purpose Registers: D, E, H, and L
  - Can address Data Memory and I/O ports
  - Can be stored to or retrieved from Stack
- ☐ Powerful Instruction Set
  - From 58 to 110 instructions, including:
    - Direct/indirect addressing
    - Table Look-up
    - RAM Stack Push/Pop
    - Single byte subroutine calls
    - RAM and I/O port single bit manipulation
    - Accumulator and I/O port Logical operations
    - 10 μs Instruction Cycle Time, typically
- ☐ Extensive General Purpose I/O Capability
  - One 4-Bit Input Port
  - Two 4-Bit latched tri-state Output Ports
  - Five 4-Bit input/latched tri-state Output Ports
  - Easily expandable with μPD82C43 CMOS I/O Expander
  - 8-Bit Parallel I/O capability
- ☐ Hardware Logic Blocks — Reduce Software Requirements
  - Operation completely transparent to instruction execution
  - 8-Bit Timer/Event Counter
    - Binary-up counter generates INT_T at coincidence
    - Accurate Crystal Clock or External Event operation possible
  - Vectored, Prioritized Interrupt Controller
    - Three external interrupts (INT_0, INT_1, INT_2)
    - Two internal interrupts (INT_T, INT_S)
  - Display Controller/Driver
    - Complete Direct Drive and Control of Multiplexed LCD or Vacuum Fluorescent Display
    - Display Data automatically multiplexed from RAM to dedicated segment/backplane/digit driver lines
  - 8-Bit Serial Interface
    - 3-line I/O configuration generates INT_S upon transmission of eighth bit
    - Ideal for distributed intelligence systems or communication with peripheral devices
  - Complete operation possible in HALT and STOP power-down modes
- ☐ Built-in System Clock Generator
- ☐ Built-in Schmidt-Trigger RESET Circuitry
- ☐ Single Power Supply, Variable from 2.7V to 5.5V
- ☐ Low Power Consumption Silicon Gate CMOS Technology
  - 900 μA max at 5V, 400 μA max at 3V
  - HALT, STOP Power-down instructions reduce power consumption to 20 μA max at 5V, 10μA at 3V (Stop mode)
- ☐ Extended −40°C to +85°C Temperature Range Available
- ☐ Choice of 28-pin or 40-pin dual-in-line packages, or 52-pin or 64-pin flat plastic packages

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Features	7500	7501	7502	7503	7506	7507	7507S	7508	7508A	7519
Internal ROM (8-bit words)		1K	2K	4K	1K	2K	2K	4K	4K	4K
Expandable to	8K									
RAM	256 x 4	96 x 4	128 x 4	224 x 4	64 x 4	128 x 4	128 x 4	224 x 4	208 x 4	256 x 4
I/O Lines	32	24	23	23	22	32	20	32	32	28
8-Bit Timer/Event Counter	•	•	•	•	•	•	•	•	•	•
8-Bit Serial Interface	•	•	•	•		•	•	•	•	•
Registers Outside RAM	4 x 4	2 x 4	4 x 4	4 x 4	2 x 4	4 x 4	4 x 4	4 x 4	4 x 4	4 x 4
Instructions	110	63	92	92	58	92	91	92	92	92
Min Cycle Time (μs)	6.67	6.67	6.67	6.67	6.67	6.67	6.67	6.67	6.67	6.67
Interrupts	5	4	4	4	2	4	4	4	4	4
Stack Levels	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM
Display Controller/ Driver		LCD	LCD	LCD					VFD drive only	VFD
Analog I/O										14-bit D/A
Current Consumption (max)										
Normal Operation	← 900 A at 5V ± 10%; 400μA at 3V ± 10% →									
Stop Mode	← 20 A at 5V ± 10%; 10μA at 3V ± 10% →									
Operating Temperature Range	−10°C to +70°C ←					−40°C to +85°C →				
Packages										
28-pin DIP					•			•		
40-pin DIP						•		•	•	
52-pin Flat					•	•		•		
64-pin Flat		•	•	•						
64-pin QUIL	•									•

Instruction Set

The μPD7500 Series Instruction Set consists of 110 powerful instructions designed to take full advantage of the advanced μPD7500 architecture in your application. It is divided into two subsets, according to the complexity of the device.

Instruction Set "A" is available for the higher-performance μPD7500 Series devices having either a 2K × 8-bit or a 4K × 8-bit Program Memory. It can be used with the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, and μPD7519 products.

Instruction Set "B" is available for the lower-cost μPD7500 Series devices having a 1K × 8-bit Program Memory. Its instructions are a compatible subset of Instruction Set "A," and can be used with the μPD7500, μPD7501, and μPD7506 products.

Instruction Set Symbol Definitions

The following abbreviations are used in the description of the μPD7500 Series Instruction sets:

Symbol	Explanation and Use
A	Accumulator
A_n	Bit "n" of Accumulator
addr	Address
bit	Operand specifying one bit of a nibble
B_n	Bit "n" of two-bit operand B_1 B_0 Bit Specified 0 0 Bit 0 (LSB) 0 1 Bit 1 1 0 Bit 2 1 1 Bit 3 (MSB)
Bank	Bank Flag of PSW (PD7500 only)
borrow	Resulting value is less than 0H
C	Carry Flag
data	Immediate data operand
D	D Register
D_n	Bit "n" of immediate data operand
DE	DE Register Pair
DL	DL Register Pair
E	E Register
H	H Register
HL	HL Register Pair
IER	Interrupt Enable Register IER bit: 0 1 2 3 Interrupt: INT_T $INT_{0/S}$ INT_1 INT_2
IME	Interrupt Master Enable F/F
INT_n	Interrupt "n"
IRF_n	Interrupt Request Flag "n"
L	L Register
overflow	Resulting value is greater than FH
P( )	Parallel Input/Output Port addressed by the value within the parentheses
PC	Program Counter
PC_n	Bit "n" of Program Counter
PSW	Program Status Word PSW bit: 0 1 2 3 Flag: Carry Bank SK_0 SK_1
rp	Register Pair, specified by the 3-bit immediate data operand D_{2-0}, as follows: D_2 D_1 D_0 rp Additional Action 0 0 0 DL none (instruction set "A" only) 0 0 1 DE none (instruction set "A" only) 1 0 0 HL– decrement L; skip if L = FH 1 0 1 HL+ increment L; skip if L = OH 1 1 0 HL none
S	Skip Cycles: 0 when skip condition does not occur 1 when skip condition does occur
SIO	Serial I/O Shift Register
SIOCR	Serial I/O Count Register
SP	Stack Pointer
String	String Effect; in a string of similar instructions, only the first encountered is executed; the remainder of the instructions in the string are executed as NOP instructions
taddr	Operand specifying ROM Table Data
T_n	Bit "n" of ROM Table Data
TCR	Timer Counter Register
TMR	Timer Modulo Register
( )	The contents of the RAM location addressed by the value within the parentheses
[ ]	The contents of the ROM location addressed by the value within the brackets
←	Load, Store, or Transfer right operand into left operand
←→	Exchange the left and right operands
NOT	Logical NOT (One's complement)
AND	LOGICAL AND
OR	LOGICAL OR
XOR	LOGICAL Exclusive OR
▨	Instruction pertains to μPD7500 only

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Instruction Set "A"

For the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, and μPD7519 devices only

Mnemonic	Function	Description	Instruction Code									Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
			Load											
LADR addr	A←(D_{7-0})	Load Accumulator from directly addressed RAM	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	0 D_0	38 00-FF	2	2	
LAI data	A←D_{3-0}	Load Accumulator with immediate data	0	0	0	1	D_3	D_2	D_1	D_0	10-1F	1	1	String
LAM rp	A←(rp) rp = DL, DE, HL−, HL+, HL if rp = HL−, skip if borrow if rp = HL+, skip if overflow	Load Accumulator from Memory, possible skip	0	1	0	D_2	0	0	D_1	D_0	40, 41 50-52	1	1+S	See explanation of "rp" in symbol definitions
LAMT (μPD7500, μPD7502 only)	ROM addr = PC_{10-6}, 0, C, A_{3-0} A←[ROM addr]$_{7-4}$ (HL)←[ROM addr]$_{3-0}$	Load Accumulator and Memory from Table	0	1	0	1	1	1	1	0	5E	1	2	
LAMTL (μPD7500, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, μPD7519, only)	ROM addr = PC_{11-8}, A_{3-0}, $(HL)_{3-0}$ A←[ROM addr]$_{7-4}$ (HL)←[ROM addr]$_{3-0}$	Load Accumulator and Memory from Table Long	0 0	0 0	1 1	1 1	1 0	1 1	1 0	1 0	3F 34	2	2	
LDEI data	D←D_{7-4} E←D_{3-0}	Load DE register pair with immediate data	0 D_7	1 D_6	0 D_5	0 D_4	1 D_3	1 D_2	1 D_1	1 D_0	4F 00-FF	2	2	
LDI data	D←D_{3-0}	Load D register with immediate data	0 0	0 0	1 1	1 0	1 D_3	1 D_2	1 D_1	0 D_0	3E 20-2F	2	2	
LEI data	E←D_{3-0}	Load E register with immediate data	0 0	0 0	1 0	1 0	1 D_3	1 D_2	1 D_1	0 D_0	3E 00-0F	2	2	
LHI data	H←D_{3-0}	Load H register with immediate data	0 0	0 0	1 1	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 30-3F	2	2	
LHLI data	H←D_{7-4} L←D_{3-0}	Load HL register pair with immediate data	0 D_7	1 D_6	0 D_5	0 D_4	1 D_3	1 D_2	1 D_1	0 D_0	4E 00-FF	2	2	String
LHLT taddr	ROM addr = 0C0H + D_{3-0} H←[ROM addr]$_{7-4}$ L←[ROM addr]$_{3-0}$	Load HL register pair from ROM Table	1	1	0	0	D_3	D_2	D_1	D_0	C0-CF	1	2	String
LLI data	L←D_{3-0}	Load L register with immediate data	0 0	0 0	1 0	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 10-1F	2	2	
			Store											
ST	(HL)←A	Store A to Memory	0	1	0	1	0	1	1	1	57	1	1	
			Transfer											
TAD	D←A	Transfer A to D	0 1	0 0	1 1	1 0	1 1	1 0	1 1	0 0	3E AA	2	2	
TAE	E←A	Transfer A to E	0 1	0 0	1 0	1 0	1 1	1 0	1 1	0 0	3E 8A	2	2	
TAH	H←A	Transfer A to H	0 1	0 0	1 1	1 1	1 1	1 0	1 1	0 0	3E BA	2	2	
TAL	L←A	Transfer A to L	0 1	0 0	1 0	1 1	1 1	1 0	1 1	0 0	3E 9A	2	2	
TDA	A←D	Transfer D to A	0 1	0 0	1 1	1 0	1 1	1 0	1 1	0 1	3E AB	2	2	
TEA	A←E	Transfer E to A	0 1	0 0	1 0	1 0	1 1	1 0	1 1	0 1	3E 8B	2	2	
THA	A←H	Transfer H to A	0 1	0 0	1 1	1 1	1 1	1 0	1 1	0 1	3E BB	2	2	
TLA	A←L	Transfer L to A	0 1	0 0	1 0	1 1	1 1	1 0	1 1	0 1	3E 9B	2	2	
			Exchange											
XAD	A↔D	Exchange A with D	0	1	0	0	1	0	1	0	4A	1	1	
XADR addr	A↔(D_{7-0})	Exchange A with directly addressed RAM	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	1 D_0	39 00-FF	2	2	
XAE	A↔E	Exchange A with E	0	1	0	0	1	0	1	1	4B	1	1	
XAH	A↔H	Exchange A with H	0	1	1	1	1	0	1	0	7A	1	1	
XAL	A↔L	Exchange A with L	0	1	1	1	1	0	1	1	7B	1	1	
XAM rp	A↔(rp) rp = DL, DE, HL−, HL+, HL if rp = HL−, skip if borrow if rp = HL+, skip if overflow	Exchange A with Memory, Possible Skip	0	1	0	D_2	0	1	D_1	D_0	44, 45 54-56	1	1+S	See explanation or "rp" in symbol definitions
XHDR addr	H↔(D_{7-0})	Exchange H with directly addressed RAM	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	0 D_0	3A 00-FF	2	2	
XLDR addr	L↔(D_{7-0})	Exchange L with directly addressed RAM	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	1 D_0	3B 00-FF	2	2	

Instruction Set "A" (Cont.)

For the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, and μPD7519 devices only

Mnemonic	Function	Description	Instruction Code								Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
Arithmetic														
ACSC	A, C←A + (HL) + C skip if carry	Add with carry; skip if carry	0	1	1	1	1	1	0	0	7C	1	1 + S	Carry = 1
ADSC	A←A + D	Add D to A, skip if overflow	0 1	0 0	1 1	1 0	1 1	1 0	1 0	0 1	3E A9	2	2 + S	Overflow
AESC	A←A + E	Add E to A, skip if overflow	0 1	0 0	1 0	1 0	1 1	1 0	1 0	0 1	3E 89	2	2 + S	Overflow
AHSC	A←A + H	Add H to A, skip if overflow	0 1	0 0	1 1	1 1	1 1	1 0	1 0	0 1	8E B9	2	2 + S	Overflow
AISC data	A←A + D_{3-0} skip if overflow	Add immediate skip if overflow	0	0	0	0	D_3	D_2	D_1	D_0	00-0F	1	1 + S	Overflow
ALSC	A←A + L	Add H to A, skip if overflow	0 1	0 0	1 0	1 1	1 1	1 0	1 0	0 1	3E 99	2	2 + S	Overflow
ASC	A←A + (HL) skip if overflow	Add memory; skip if overflow	0	1	1	1	1	1	0	1	7C	1	1 + S	Carry = 1
SDSB	A←A − D skip if borrow	Subtract D from A, skip if borrow	0 1	0 0	1 1	1 0	1 1	1 0	1 0	0 0	3E A8	2	2 + S	Borrow
SESB	A←A − E skip if borrow	Subtract E from A, skip if borrow	0 1	0 0	1 0	1 0	1 1	1 0	1 0	0 0	3E 88	2	2 + S	Borrow
SHSB	A←A − H	Subtract H from A, skip if borrow	0 1	0 0	1 1	1 1	1 1	1 0	1 0	0 0	3E B8	2	2 + S	Borrow
SLSB	A←A − L	Subtract L from A, skip if borrow	0 1	0 0	1 0	1 1	1 1	1 0	1 0	1 0	3E 98	2	2 + S	Borrow
Logical														
ANL	A←A AND (HL)	AND Accumulator and Memory	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 0	3F B2	2	2	
EXL	A←A XOR (HL)	Exclusive-Or Accumulator and Memory	0	1	1	1	1	1	1	0	7E	1	1	
ORL	A←A OR (HL)	OR Accumulator and Memory	0 1	0 0	1 1	1 1	1 0	1 1	1 1	1 0	3F B6	2	2	
Accumulator														
CMA	A←NOT A	Complement Accumulator	0	1	1	1	1	1	1	1	7F	1	1	
RAL	C←A_3 A_3←A_2 A_2←A_1 A_1←A_0 A_0←C (old)	Rotate Accumulator left through Carry	0 1	0 0	1 1	1 1	1 0	1 1	1 1	1 1	3F B7	2	2	
RAR	C←A_0 A_0←A_1 A_1←A_2 A_2←A_3 A_3←C (old)	Rotate Accumulator right through Carry	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 1	3F B3	2	2	
Program Status Word														
RC	C←0	Reset Carry	0	1	1	1	1	0	0	0	78	1	1	
SC	C←1	Set Carry	0	1	1	1	1	0	0	1	79	1	1	
Increment and Decrement														
DDE	DE←DE − 1	Decrement DE	0 1	0 0	1 0	1 0	1 1	1 1	1 0	0 0	3E 8C	2	2	
DDRS addr	(D_{7-0})←(D_{7-0}) − 1 skip if (D_{7-0}) = FH	Decrement directly addressed RAM; skip if borrow	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	0 D_0	3C 00-FF	2	2 + S	(D_{7-0}) = FH
DES	E←E − 1 skip if E = FH	Decrement E; skip if borrow	0	1	0	0	1	0	0	0	48	1	1 + S	E = FH
DHL	HL←HL − 1	Decrement HL	0 1	0 0	1 0	1 1	1 1	1 1	1 0	0 0	3E 9C	2	2	
DLS	L←L − 1 skip if L = FH	Decrement L; skip if borrow	0	1	0	1	1	0	0	0	58	1	1 + S	L = FH
IDE	DE←DE + 1	Increment DE	0 1	0 0	1 0	1 0	1 1	1 1	1 0	0 1	3E 8D	2	2	
IDRS addr	(D_{7-0})←(D_{7-0}) − 1 skip if (D_{7-0}) = 0H	Increment directly addressed; skip if overflow	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0	3D 00-FF	2	2 + S	(D_{7-0}) = 0H
IES	E←E + 1 skip if E = 0H	Increment E; skip if overflow	0	1	0	0	1	0	0	1	49	1	1 + S	E = 0H
IHL	HL←HL + 1	Increment HL	0 1	0 0	1 0	1 1	1 1	1 1	1 0	0 1	3E 9D	2	2	
ILS	L←L + 1 skip if L = 0H	Increment L; skip if overflow	0	1	0	1	1	0	0	1	59	1	1 + S	L = 0H 1
Bit Manipulation														
RMB bit	(HL)$_{bit}$←0 bit = B_{1-0} (0-3)	Reset Memory bit	0	1	1	0	1	0	B_1	B_0	68-6B	1	1	
SMB bit	(HL)$_{bit}$←1 bit = B_{1-0} (0-3)	Set Memory bit	0	1	1	0	1	1	B_1	B_0	6C-6F	1	1	

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Instruction Set "A" (Cont.)

For the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, and μPD7519 devices only

Mnemonic	Function	Description	Instruction Code									Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
			Branch											
CALL addr	(SP – 1)←PC_{7-4} (SP – 2)←PC_{3-0} (SP – 3)←PSW (SP – 4)←PC_{11-18} SP←SP – 4 BANK←0 PC_{11}←0 PC_{10-0}←D_{10-0}	Call subroutine	0 D_7	0 D_6	1 D_5	1 D_4	0 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	30-37 00-FF	2	2	
CALT addr	(SP – 1)←PC_{7-4} (SP – 2)←PC_{3-0} (SP – 3)←PSW (SP – 4)←PC_{11-8} ROM addr = 0C0H + D_{5-0} BANK←0 PC_{11-10}←00 PC_{9-7}←[ROM addr]$_{7-5}$ PC_{6-5}←00 PC_{4-0}←[ROM addr]$_{4-0}$	Call subroutine through ROM Table (single byte)	1	1	D_5	D_4	D_3	D_2	D_1	D_0	D0-FF	1	2	
JAM data	PC_{11-8}←D_{3-0} PC_{7-4}←A PC_{3-0}←(HL)	Vectored Jump on Accumulator and Memory	0 0	0 0	1 0	1 1	1 D_3	1 D_2	1 D_1	1 D_0	3F 10-1F	2	2	
JCP addr	PC_{5-0}←D_{5-0}	Jump within current page	1	0	D_5	D_4	D_3	D_2	D_1	D_0	80-BF	1	1	
JMP addr	PC_{11-0}←D_{11-0}	Jump to specified address	0 D_7	0 D_6	1 D_5	0 D_4	D_{11} D_3	D_{10} D_2	D_9 D_1	D_8 D_0	20-2F 00-FF	2	2	
JUMPL addr	BANK←D_{12} PC_{11-0}←D_{11-0}	Jump Long to specified address	0 0 D_7	0 0 D_6	1 D_{12} D_5	1 0 D_4	1 D_{11} D_3	1 D_{10} D_2	1 D_9 D_1	1 D_8 D_0	3F 00-0F 20-2F 00-FF	3	3	
RT	PC_{11-8}←(SP) BANK←(SP + 1) PC_{3-0}←(SP + 2) PC_{7-4}←(SP + 3) SP←SP + 4	Return from Subroutine	0	1	0	1	0	0	1	1	53	1	1	
RTPSW	PC_{11-8}←(SP) PSW←(SP + 1) PC_{3-0}←(SP + 2) PC_{7-4}←(SP + 3) SP←SP + 4	Return from Subroutine and restore PSW	0	1	0	0	0	0	1	1	43	1	2	
RTS	PC_{11-8}←(SP) BANK←(SP + 1) PC_{3-0}←(SP + 2) PC_{7-4}←(SP + 3) SP←(SP + 4) Skip unconditionally	Return from Subroutine; then skip next instruction	0	1	0	1	1	0	1	1	5B	1	1 + S	Unconditional
			Stack											
POPDE	E←(SP) D←(SP + 1) SP←SP + 2	Pop DE register pair off Stack	0 1	0 0	1 0	1 0	1 1	1 1	1 1	0 1	3E 8F	2	2	
POPHL	L←(SP) H←(SP + 1) SP←SP + 2	Pop HL register pair off Stack	0 1	0 0	1 0	1 1	1 1	1 1	1 1	0 1	3E 9F	2	2	
PSHDE	(SP – 1)←D (SP – 2)←E SP←SP – 2	Push DE register pair on Stack	0 1	0 0	1 0	1 0	1 1	1 1	1 1	0 0	3E 8E	2	2	
PSHHL	(SP – 1)←H (SP – 2)←L SP←SP – 2	Push HL register pair on Stack	0 1	0 0	1 0	1 1	1 1	1 1	1 1	0 0	3E 9E	2	2	
TAMSP	SP_{7-4}←A SP_{3-1}←$(HL)_{3-1}$ SP_0←0	Transfer Accumulator and Memory to Stack Pointer	0 0	0 0	1 1	1 1	1 0	1 0	1 0	1 1	3F 31	2	2	
TSPAM	A←SP_{7-4} $(HL)_{3-1}$←SP_{3-1} $(HL)_0$←0	Transfer Stack Pointer to Accumulator and Memory	0 0	0 0	1 1	1 1	1 0	1 1	1 0	1 1	3F 35	2	2	
			Conditional Skip											
SKABT bit	Skip if A_{bit} = 1 bit = $B_{1-0(0-3)}$	Skip if Accumulator bit true	0	1	1	1	0	1	B_1	B_0	74-77	1	1 + S	A_{bit} = 1
SKAEI data	Skip if A = D_{3-0}	Skip if Accumulator equals immediate data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	3F 60-6F	2	2 + S	A = D_{3-0}
SKAEM	Skip if A = (HL)	Skip if Accumulator equals Memory	0	1	0	1	1	1	1	1	5F	1	1 + S	A = (HL)
SKC	Skip if C = 1	Skip if Carry	0	1	0	1	1	0	1	0	5A	1	1 + S	C = 1
SKDEI data	Skip if D = D_{3-0}	Skip if D equals immediate data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	0 D_0	3E 60-6F	2	2 + S	D = D_{3-0}
SKEEI data	Skip if E = D_{3-0}	Skip if E equals immediate data	0 0	0 1	1 0	1 0	1 D_3	1 D_2	1 D_1	0 D_0	3E 40-4F	2	2 + S	E = D_{3-0}
SKHEI data	Skip if H = D_{3-0}	Skip if H equals immediate data	0 0	0 1	1 1	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 70-7F	2	2 + S	H = D_{3-0}

Instruction Set "A" (Cont.)

For the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, and μPD7519 devices only

Mnemonic	Function	Description	Instruction Code								Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
Conditional Skip (Cont.)														
SKLEI data	Skip if L = D_{3-0}	Skip if L equals immediate data	0 0	0 1	1 0	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 50-5F	2	2+S	L = D_{3-0}
SKMBF bit	Skip if $(HL)_{bit}$ = 0 bit = B_{1-0}(0-3)	Skip if Memory bit false	0	1	1	0	0	0	B_1	B_0	60-63	1	1+S	$(HL)_{bit}$ = 0
SKMBT bit	Skip if $(HL)_{bit}$ = 1 bit = B_{1-0}(0-3)	Skip if Memory bit true	0	1	1	0	0	1	B_1	B_0	64-67	1	1+S	$(HL)_{bit}$ = 1
SKMEI	Skip if (HL) = D_{3-0}	Skip if Memory equals immediate data	0 0	0 1	1 1	1 1	1 D_3	1 D_2	1 D_1	1 D_0	3F 70-7F	2	2+S	(HL) = D_{3-0}
Timer/Event Counter														
TAMMOD	TMR_{7-4}←A TMR_{3-0}←(HL)	Transfer Accumulator and Memory to Timer Modulo Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 1	3F 3F	2	2	
TCNTAM	A←TCR_{7-4} (HL)←TCR_{3-0}	Transfer Timer Count Register to Accumulator and Memory	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 1	3F 3B	2	2	
TIMER	TCR_{7-0}←0 IRF_T←0	Start Timer	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 0	3F 32	2	2	
Interrupt Control														
DI data	IME F/F←0 if data = 0 IER_{3-0}←IER_{3-0} AND NOT D_{3-0} if data < > 0	Disable Interrupt, Interrupt Master Enable F/F or specified	0 1	0 0	1 0	1 0	1 D_3	1 D_2	1 D_1	1 D_0	3F 80-8F	2	2	
EI data	IME F/F←1 if data = 0 IER_{3-0}←IER_{3-0} OR D_{3-0} if data < > 0	Enable Interrupt, Interrupt Master Enable F/F or specified	0 1	0 0	1 0	1 1	1 D_3	1 D_2	1 D_1	1 D_0	3F 90-8F	2	2	
SKI data	Skip if IRF_n AND D_{3-0} < > 0 IRF_n←IRF_n AND NOT D_{3-0}	Skip if Interrupt Request Flag is true	0 0	0 1	1 0	1 0	1 D_3	1 D_2	1 D_1	1 D_0	3F 40-4F	2	2+S	IRF_n = 1
Serial Interface														
SIO	SIOCR←0 $IRF_{0/S}$←0	Start Serial I/O Operation	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 1	3F 33	2	2	
TAMSIO	SIO_{7-4}←A SIO_{3-0}←(HL)	Transfer Accumulator and Memory to SI Shift Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 0	3F 3E	2	2	
TSIOAM	A←SIO_{7-4} (HL)←SIO_{3-0}	Transfer SI Shift Register to Accumulator and Memory	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 0	3F 3A	2	2	
Parallel I/O														
ANP data	$P(P_{3-0})$←$P(P_{3-0})$ AND D_{3-0}	AND output port latch with immediate data	0 D_3	1 D_2	0 D_1	0 D_0	1 P_3	1 P_2	0 P_1	0 P_0	4C 00-FF	2	2	
IP port	A←$P(P_{3-0})$	Input from port, immediate address	0 1	0 1	1 0	1 0	1 P_3	1 P_2	1 P_1	1 P_0	3F C0-CF	2	2	
IP1 (except μPD7507S)	A←P(1)	Input from Port 1	0	1	1	1	0	0	0	1	71	1	1	
IP54	A←P(5) (HL)←P(4)	Input Byte from Ports 5 and 4	0 0	0 0	1 1	1 1	1 1	1 0	1 0	1 0	3F 38	2	2	
IPL	A←P(L)	Input from Port specified by L	0	1	1	1	0	0	0	0	70	1	1	
OP port	$P(P_{3-0})$←A	Output to port, immediate address	0 1	0 1	1 1	1 0	1 P_3	1 P_2	1 P_1	1 P_0	3F E0-EF	2	2	
OP3	P(3)←A	Output to Port 3	0	1	1	1	0	0	1	1	73	1	1	
OP54	P(5)←A P(4)←(HL)	Output Byte to Ports 5 and 4	0 0	0 0	1 1	1 1	1 1	1 1	1 0	1 0	3F 3C	2	2	
OPL	P(L)←A	Output to port specified by L	0	1	1	1	0	0	1	0	72	1	1	
ORP data	$P(P_{3-0})$←(P_{3-0}) OR D_{3-0}	OR output port latch with immediate data	0 D_3	1 D_2	0 D_1	0 D_0	1 P_3	1 P_2	0 P_1	1 P_0	4D 00-FF	2	2	
RPBL	μPD82C43 I/O Expander Port (L_{3-2}) bit (L_{1-0})←0	Reset Port Bit specified by L	0	1	0	1	1	1	0	0	5C	1	1	
SPBL	μPD82C43 I/O Expander Port (L_{3-2}) bit (L_{1-0})←1	Set Port Bit specified by L	0	1	0	1	1	1	0	1	5D	1	1	
CPU Control														
HALT		Enter HALT Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 0	3F 36	2	2	
NOP		No operation	0	0	0	0	0	0	0	0	00	1	1	
STOP		Enter STOP Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 1	3F 37	2	2	

Instruction Set "B"

For the μPD7500, μPD7501, and μPD7506 devices only

Mnemonic	Function	Description	Instruction Code									Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
		Load												
LADR addr	A←(D_{6-0})	Load Accumulator from directly addressed RAM	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	0 D_0	38 00-5F	2	2	
LAI data	A←D_{3-0}	Load Accumulator with immediate data	0	0	0	1	D_3	D_2	D_1	D_0	10-1F	1	1	String
LAM rp	A←(rp) rp = HL−, HL+, HL If rp = HL−, skip if borrow if rp = HL+, skip if overflow	Load Accumulator from Memory, possible skip	0	1	0	1	0	0	D_1	D_0	50-52	1	1+S	See explanation of "rp" in symbol definitions
LAMT	ROM addr = PC_{10-6}, 0, C, A_{3-0} A←[ROM addr]$_{7-4}$ (HL)←[ROM addr]$_{3-0}$	Load Accumulator and Memory from Table	0	1	0	1	1	1	1	0	5E	1	2	
LAMTL	ROM addr = PC_{10-8}, A_{3-0}, $(HL)_{3-0}$ A←[ROM addr]$_{7-4}$ (HL)←[ROM addr]$_{3-0}$	Load Accumulator and Memory from Table Long	0 0	0 0	1 1	1 1	1 0	1 1	1 0	1 0	3F 34	2	2	
LHI data	H_3←0 H_{2-0}←D_{2-0}	Load H register with immediate data	0	0	1	0	1	D_2	D_1	D_0	28-2F	1	1	
LHLI data	H_{3-1}←0 H_0←D_4 L←D_{3-0}	Load HL register pair with immediate data	1	1	0	D_4	D_3	D_2	D_1	D_0	C0-DF	1	1	String
		Store												
ST	(HL)←A	Store A to Memory	0	1	0	1	0	1	1	1	57	1	1	
STII data	(HL)←D_{3-0} L←L + 1	Store immediate data and increment L	0	1	0	0	D_3	D_2	D_1	D_0	40-4F	1	1	
		Exchange												
XADR addr	A↔(D_{6-0})	Exchange A with directly addressed RAM	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	1 D_0	39 00-5F	2	2	
XAH	A↔H	Exchange A with H	0	1	1	1	1	0	1	0	7A	1	1	
XAL	A↔L	Exchange A with L	0	1	1	1	1	0	1	1	7B	1	1	
XAM rp	A↔(rp) rp = HL−, HL+, HL If rp = HL−, skip if borrow if rp = HL+, skip if overflow	Exchange A with Memory, Possible Skip	0	1	0	1	0	1	D_1	D_0	54-56	1	1+S	See explanation or "rp" in symbol definitions
XHDR addr	H↔(D_{6-0})	Exchange H with directly addressed RAM	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	0 D_0	3A 00-5F	2	2	
XLDR addr	L↔(D_{6-0})	Exchange L with directly addressed RAM	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	1 D_0	3B 00-5F	2	2	
		Arithmetic												
ACSC	A, C←A ± (HL) + C skip if carry	Add with carry; skip if carry	0	1	1	1	1	1	0	0	7C	1	1+S	Carry = 1
AISC data	A←A + D_{3-0} skip if overflow	Add immediate; skip if overflow	0	0	0	0	D_3	D_2	D_1	D_0	00-0F	1	1+S	Overflow
ASC	A←A + (HL) skip if overflow	Add memory; skip if overflow	0	1	1	1	1	1	0	1	7C	1	1+S	Carry = 1
		Logical												
ANL	A←A AND (HL)	AND Accumulator and Memory	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 0	3F B2	2	2	
EXL	A←A XOR (HL)	Exclusive-Or Accumulator and Memory	0	1	1	1	1	1	1	0	7E	1	1	
ORL	A←A OR (HL)	OR Accumulator and Memory	0 1	0 0	1 1	1 1	1 0	1 1	1 1	1 0	3F B6	2	2	
		Accumulator												
CMA	A←NOT A	Complement Accumulator	0	1	1	1	1	1	1	1	7F	1	1	
RAL	C←A_3 A_3←A_2 A_2←A_1 A_1←A_0 A_0←C (old)	Rotate Accumulator left through Carry	0 1	0 0	1 1	1 1	1 0	1 1	1 1	1 1	3F B7	2	2	
RAR	C←A_0 A_0←A_1 A_1←A_2 A_2←A_3 A_3←C (old)	Rotate Accumulator right through Carry	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 1	3F B3	2	2	
		Program Status Word												
RC	C←0	Reset Carry	0	1	1	1	1	0	0	0	78	1	1	
SC	C←1	Set Carry	0	1	1	1	1	0	0	1	79	1	1	

Instruction Set "B" (Cont.)

For the μPD7500, μPD7501, and μPD7506 devices only

Mnemonic	Function	Description	Instruction Code								Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
Increment and Decrement														
DDRS addr	$(D_{6\text{-}0}) \leftarrow (D_{6\text{-}0}) - 1$ skip if $(D_{6\text{-}0})$ = FH	Decrement directly addressed RAM; skip if borrow	0 0	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	0 D_0	3C 00-5F	2	2+S	$(D_{6\text{-}0})$ = FH
DLS	$L \leftarrow L - 1$ skip if L = FH	Decrement L; skip if borrow	0	1	0	1	1	0	0	0	58	1	1+S	L = FH
IDRS addr	$(D_{6\text{-}0}) \leftarrow (D_{6\text{-}0}) + 1$ skip if $(D_{6\text{-}0})$ = 0H	Increment directly addressed; skip if overflow	0 0	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0	3D 00-5F	2	2+S	$(D_{6\text{-}0})$ = 0H
ILS	$L \leftarrow L + 1$ skip if L = 0H	Increment L; skip if overflow	0	1	0	1	1	0	0	1	59	1	1+S	L = 0H
Bit Manipulation														
RMB bit	$(HL)_{bit} \leftarrow 0$ bit = $B_{1\text{-}0}$ (0-3)	Reset Memory bit	0	1	1	0	1	0	B_1	B_0	68-6B	1	1	
SMB bit	$(HL)_{bit} \leftarrow 1$ bit = $B_{1\text{-}0}$ (0-3)	Set Memory bit	0	1	1	0	1	1	B_1	B_0	6C-6F	1	1	
Branch														
CALL addr	$(SP-1) \leftarrow PC_{7\text{-}4}$ $(SP-2) \leftarrow PC_{3\text{-}0}$ $(SP-3) \leftarrow PSW$ $(SP-4) \leftarrow PC_{10\text{-}8}$ $SP \leftarrow SP-4$ $BANK \leftarrow 0$ $PC_{10\text{-}0} \leftarrow D_{10\text{-}0}$	Call subroutine	0 D_7	0 D_6	1 D_5	1 D_4	0 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	30-37 00-FF	2	2	
CAL addr	$(SP-1) \leftarrow PC_{7\text{-}4}$ $(SP-2) \leftarrow PC_{3\text{-}0}$ $(SP-3) \leftarrow PSW$ $(SP-4) \leftarrow PC_{10\text{-}8}$ $BANK \leftarrow 0$ $PC_{10\text{-}0} \leftarrow 001D_4D_3000D_2D_1D_0$	Call short to CAL address subroutine	1	1	1	D_4	D_3	D_2	D_1	D_0	E0-FF	1	2	
JAM data	$PC_{10\text{-}8} \leftarrow D_{2\text{-}0}$ $PC_{7\text{-}4} \leftarrow A$ $PC_{3\text{-}0} \leftarrow (HL)$	Vectored Jump on Accumulator and Memory	0 0	0 0	1 0	1 1	1 0	1 D_2	1 D_1	1 D_0	3F 10-17	2	2	
JCP addr	$PC_{5\text{-}0} \leftarrow D_{5\text{-}0}$	Jump within current page	1	0	D_5	D_4	D_3	D_2	D_1	D_0	80-BF	1	1	
JMP addr	$PC_{10\text{-}0} \leftarrow D_{10\text{-}0}$	Jump to specified address	0 D_7	0 D_6	1 D_5	0 D_4	0 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	20-27 00-FF	2	2	
JMPL addr	$BANK \leftarrow D_{12}$ $PC_{11\text{-}0} \leftarrow D_{11\text{-}0}$	Jump Long to specified address	0 0 D_7	0 0 D_6	1 D_{12} D_5	1 0 D_4	1 D_{11} D_3	1 D_{10} D_2	1 D_9 D_1	1 D_8 D_0	3F 00-0F 20-2F 00-FF	3	3	
RT	$PC_{10\text{-}8} \leftarrow (SP)$ $BANK \leftarrow (SP+1)$ $PC_{3\text{-}0} \leftarrow (SP+2)$ $PC_{7\text{-}4} \leftarrow (SP+3)$ $SP \leftarrow SP+4$	Return from Subroutine	0	1	0	1	0	0	1	1	53	1	1	
RTS	$PC_{10\text{-}8} \leftarrow (SP)$ $BANK \leftarrow (SP+1)$ $PC_{3\text{-}0} \leftarrow (SP+2)$ $PC_{7\text{-}4} \leftarrow (SP+3)$ $SP \leftarrow SP+4$ Skip unconditionally	Return from Subroutine; then skip next instruction	0	1	0	1	1	0	1	1	5B	1	1+S	Unconditional
Stack														
TAMSP	$SP_{7\text{-}4} \leftarrow A$ $SP_{3\text{-}1} \leftarrow (HL)_{3\text{-}1}$ $SP_0 \leftarrow 0$	Transfer Accumulator and Memory to Stack Pointer	0 0	0 0	1 1	1 1	1 0	1 0	1 0	1 1	3F 31	2	2	
TSPAM	$A \leftarrow SP_{7\text{-}4}$ $(HL)_{3\text{-}1} \leftarrow SP_{3\text{-}1}$ $(HL)_0 \leftarrow 0$	Transfer Stack Pointer to Accumulator and Memory	0 0	0 0	1 1	1 1	1 0	1 1	1 0	1 1	3F 35	2	2	
Conditional Skip														
SKABT bit	Skip if A_{bit} = 1 bit = $B_{1\text{-}0}$(0-3)	Skip if Accumulator bit true	0	1	1	1	0	1	B_1	B_0	74-77	1	1+S	A_{bit} = 1
SKAEI data	Skip if A = $D_{3\text{-}0}$	Skip if Accumulator equals immediate data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	3F 60-6F	2	2+S	A = $D_{3\text{-}0}$
SKAEM	Skip if A = (HL)	Skip if Accumulator equals Memory	0	1	0	1	1	1	1	1	5F	1	1+S	A = (HL)
SKC	Skip if C = 1	Skip if Carry	0	1	0	1	1	0	1	0	5A	1	1+S	C = 1
SKLEI data	Skip if L = $D_{3\text{-}0}$	Skip if L equals immediate data	0 0	0 1	1 0	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 50-5F	2	2+S	L = $D_{3\text{-}0}$
SKMBF bit	Skip if $(HL)_{bit}$ = 0 bit = $B_{1\text{-}0}$(0-3)	Skip if Memory bit false	0	1	1	0	0	0	B_1	B_0	60-63	1	1+S	$(HL)_{bit}$ = 0
SKMBT bit	Skip if $(HL)_{bit}$ = 1 bit = $B_{1\text{-}0}$(0-3)	Skip if Memory bit true	0	1	1	0	0	1	B_1	B_0	64-67	1	1+S	$(HL)_{bit}$ = 1
SKMEI	Skip if (HL) = $D_{3\text{-}0}$	Skip if Memory equals immediate data	0 0	0 1	1 1	1 1	1 D_3	1 D_2	1 D_1	1 D_0	3F 70-7F	2	2+S	(HL) = $D_{3\text{-}0}$

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Instruction Set "B" (Cont.)

For the μPD7500, μPD7501, and μPD7506 devices only

Mnemonic	Function	Description	Instruction Code								Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
Timer/Event Counter														
TAMMOD	$TMR_{7-4} \leftarrow A$ $TMR_{3-0} \leftarrow (HL)$	Transfer Accumulator and Memory to Timer Modulo Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 1	3F 3F	2	2	
TCNTAM (except μPD7506)	$A \leftarrow TCR_{7-4}$ $(HL) \leftarrow TCR_{3-0}$	Transfer Timer Count Register to Accumulator and Memory	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 1	3F 3B	2	2	
TIMER	$TCR_{7-0} \leftarrow 0$ $IRF_T \leftarrow 0$	Start Timer	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 0	3F 32	2	2	
Interrupts														
SKI data	Skip if IRF_n AND $D_{3-0} <> 0$ $IRF_n \leftarrow IRF_n$ AND NOT D_{3-0}	Skip if Interrupt Request Flag is true	0 0	0 1	1 0	1 0	1 0	1 D_2	1 D_1	1 D_0	3F 40-47	2	2+S	$IRF_n = 1$
Serial Interface														
SIO (except μPD7506)	$SIOCR \leftarrow 0$ $IRF_{0/S} \leftarrow 0$	Start Serial I/O Operation	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 1	3F 33	2	2	
TAMSIO (except μPD7506)	$SIO_{7-4} \leftarrow A$ $SIO_{3-0} \leftarrow (HL)$	Transfer Accumulator and Memory to SIO Shift Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 0	3F 3E	2	2	
TSIOAM (except μPD7506)	$A \leftarrow SIO_{7-4}$ $HL \leftarrow SIO_{3-0}$	Transfer SIO Shift Register to Accumulator and Memory	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 0	3F 3A	2	2	
Parallel I/O														
IP port	$A \leftarrow P(P_{3-0})$	Input from port, immediate address	0 1	0 1	1 0	1 0	1 P_3	1 P_2	1 P_1	1 P_0	3F C0-CF	2	2	
IP1	$A \leftarrow (1)$	Input from Port 1	0	1	1	1	0	0	0	1	71	1	1	
IP54	$A \leftarrow P(5)$ $(HL) \leftarrow P(4)$	Input Byte from Ports 5 and 4	0 0	0 0	1 1	1 1	1 1	1 0	1 0	1 0	3F 38	2	2	
IPL	$A \leftarrow P(L)$	Input from Port specified by L	0	1	1	1	0	0	0	0	70	1	1	
OP port	$P(P_{3-0}) \leftarrow A$	Output to port, immediate address	0 1	0 1	1 1	1 0	1 P_3	1 P_2	1 P_1	1 P_0	3F E0-EF	2	2	
OP3 (except μPD7506)	$P(3) \leftarrow A$	Output to Port 3	0	1	1	1	0	0	1	1	73	1	1	
OP54	$P(5) \leftarrow A$ $P(4) \leftarrow (HL)$	Output Byte to Ports 5 and 4	0 0	0 0	1 1	1 1	1 1	1 1	1 0	1 0	3F 3C	2	2	
OPL	$P(L) \leftarrow A$	Output to port specified by L	0	1	1	1	0	0	1	0	72	1	1	
RPBL	μPD82C43 I/O Expander Port (L_{3-2}) bit $(L_{1-0}) \leftarrow 0$	Reset Port Bit Specified by L	0	1	0	1	1	1	0	0	5C	1	1	
SPBL	μPD82C43 I/O Expander Port (L_{3-2}) bit $(L_{1-0}) \leftarrow 1$	Set Port Bit Specified by L	0	1	0	1	1	1	0	1	5D	1	1	
CPU Control														
HALT		Enter HALT Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 0	3F 36	2	2	
NOP		No operation	0	0	0	0	0	0	0	0	00	1	1	
STOP		Enter STOP Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 1	3F 37	2	2	

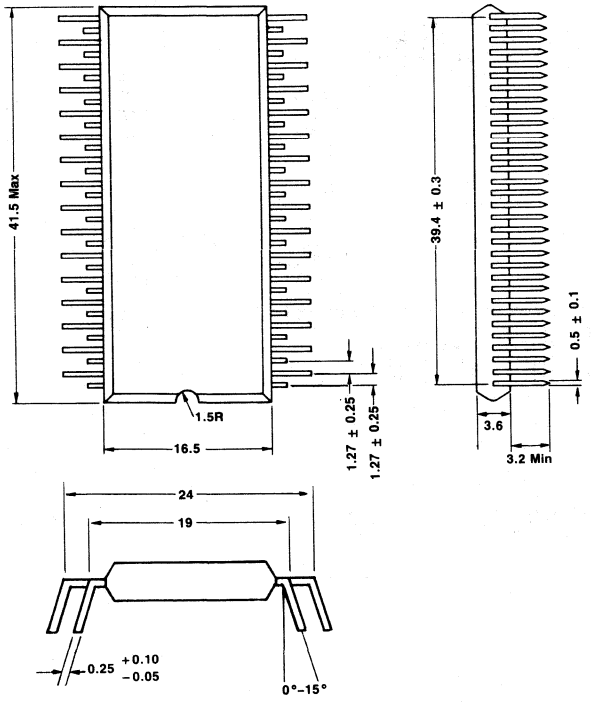
Development Tools

For software development, editing, debugging, and assembly into object code, the NDS Development System, designed and manufactured by NEC Electronics U.S.A., Inc., is available. Additionally, for systems supporting either the ISIS-II (® Intel Corp.), CP/M (® Digital Research Corp.) or FDOS-II (® Motorola, Inc.,) operating systems, or Fortran IV ANSI 1966 V3.9, the ASM75 Cross-Assembler is available.

Once software development is complete, the code can be completely evaluated and debugged with hardware by the Evakit-7500 Evaluation Board. Available options include the Evakit-7500-LCD LCD driver board (for the μPD7501, μPD7502, and μPD7503), Evakit-7500-VFD Vacuum Fluorescent Display driver board (for the μPD7508A and μPD7519), and the Evakit-7500-RTT Real Time Tracer. The SE-7502 System Emulation Board will emulate complete functionality of the μPD7501, μPD7502, or μPD7503 for demonstrating your final system design. The SE-7508 System Emulation Board will emulate complete functionality of the μPD7506, μPD7507, μPD7507S, μPD7508, or μPD7508A for demonstrating your final system design. All of these boards take advantage of the capabilities of the μPD7500 Rom-less evaluation chip to perform their tasks.

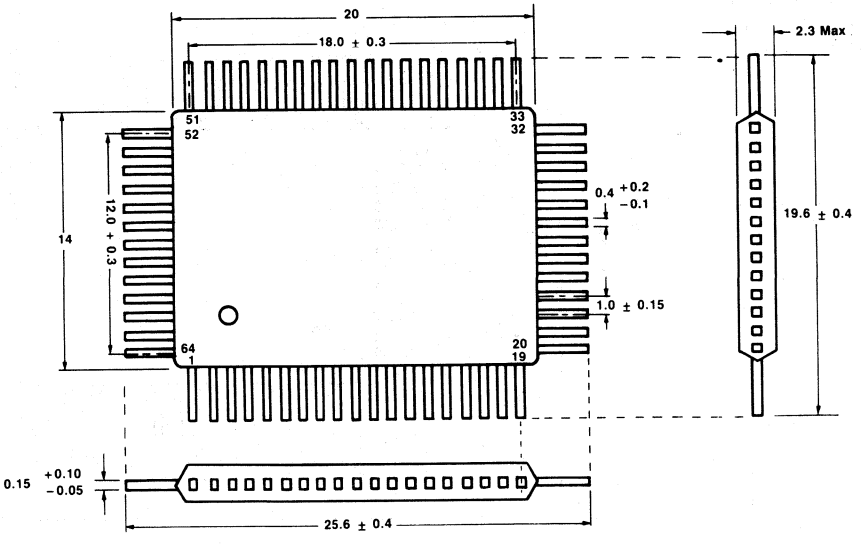
Complete operation details on any μPD7500 Series CMOS 4-Bit Microcomputer can be found in the μPD7500 Series CMOS 4-Bit Microcomputer Technical Manual.

Package Outline
μPD7500G
μPD7519G-XXX-36



Package Outlines

μPD7501G-XXX-11
μPD7502G-XXX-11
μPD7503G-XXX-11

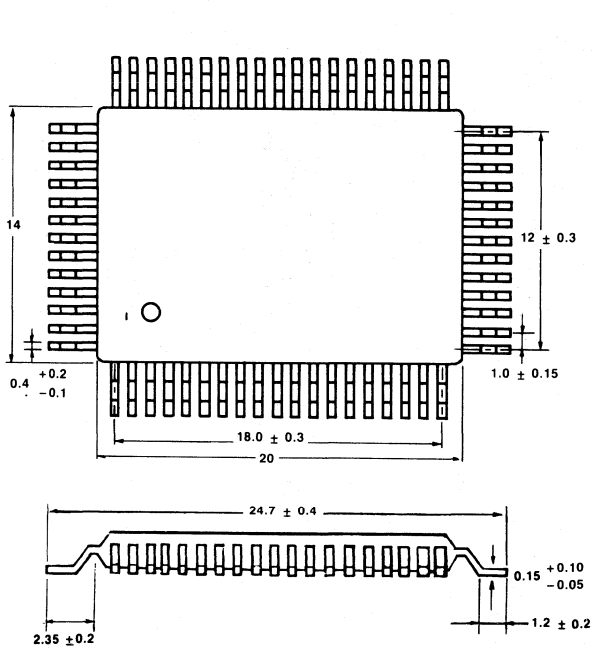


XXX denotes mask number assigned by factory at time of code submission

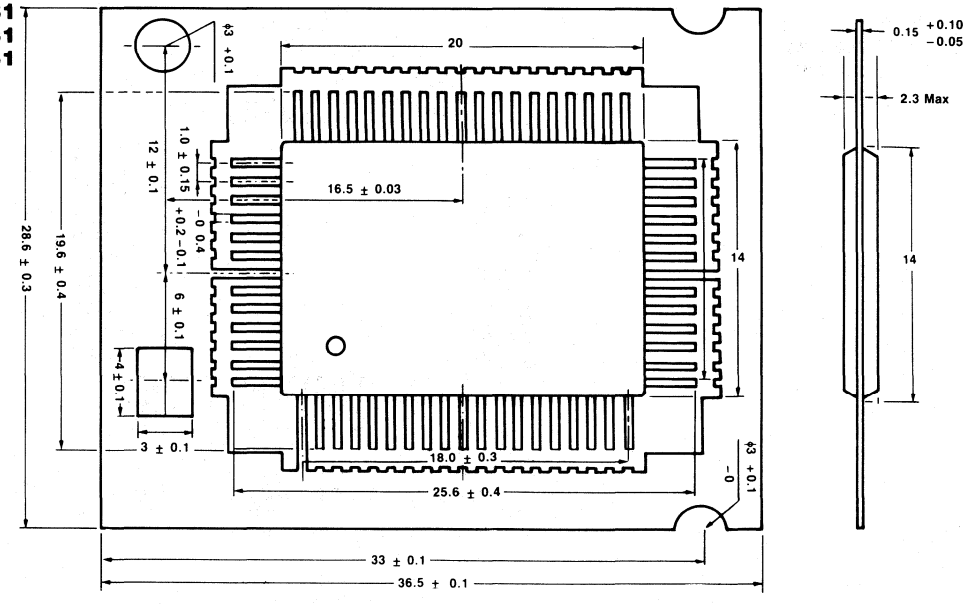
Use I.C. Socket IC-51-59S.

Package Outlines

μPD7501G-XXX-12
μPD7502G-XXX-12
μPD7503G-XXX-12



μPD7501G-XXX-B1
μPD7502G-XXX-B1
μPD7503G-XXX-B1

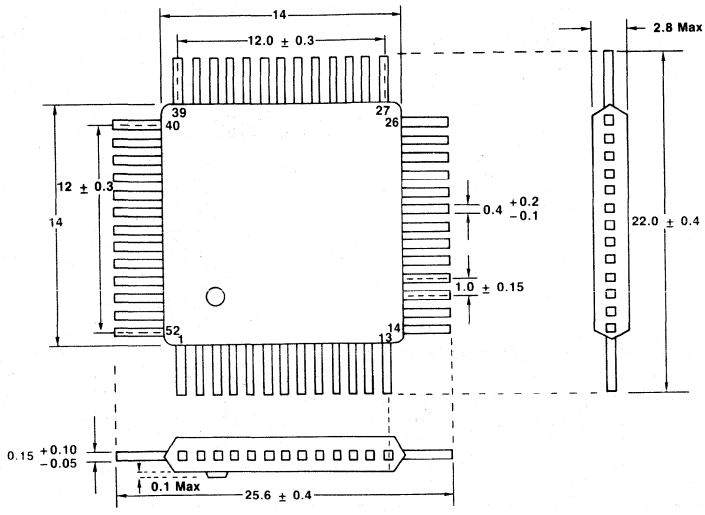


XXX denotes mask number assigned by factory at time of code submission.

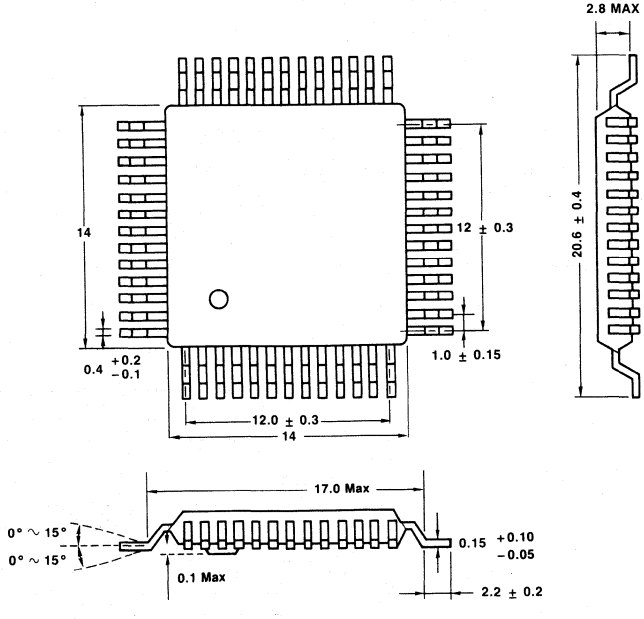
Use I.C. Socket IC-51-59S.

Package Outlines

μPD7506G-XXX-01
μPD7507G-XXX-01
μPD7508G-XXX-01



μPD7506G-XXX-00
μPD7507G-XXX-00
μPD7508G-XXX-00



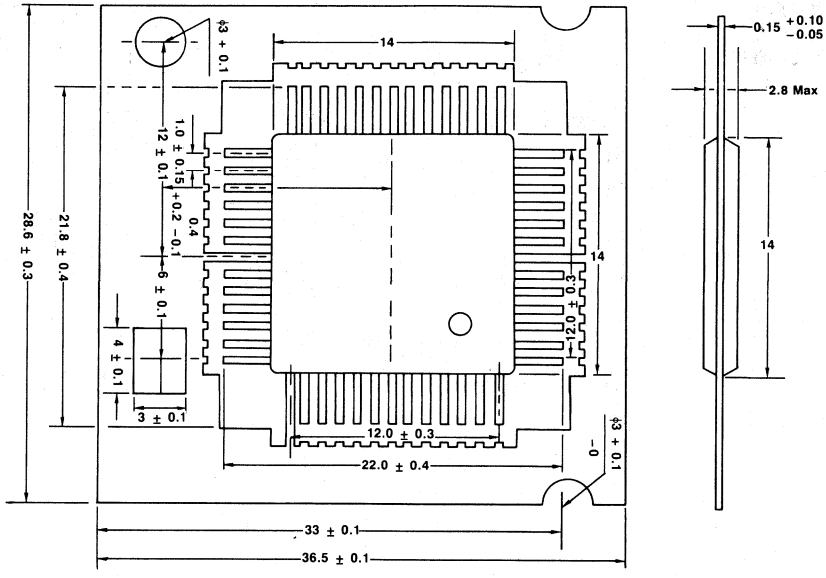
XXX denotes mask number assigned by factory at time of code submission.

Use I.C. Socket IC-53-11.

6

Package Outlines

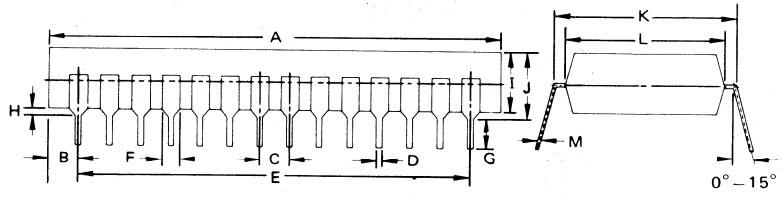
μPD7506G-XXX-A1
μPD7507G-XXX-A1
μPD7508G-XXX-A1



"XXX" denotes mask number assigned by factory at time of code submission.

Use I.C. Socket IC-53-11.

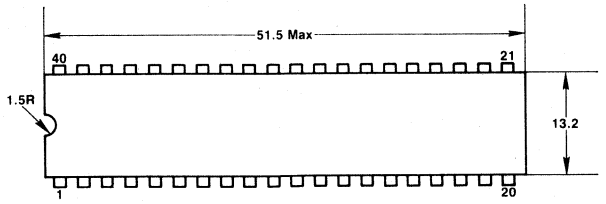
μPD7506C-XXX
μPD7507SC-XXX

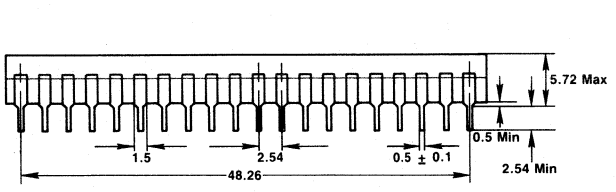


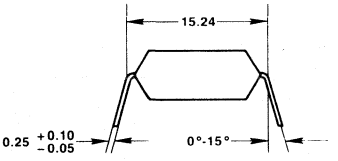
Item	Millimeters	Inches
A	38.0 MAX	1.496 MAX
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	0.25 +0.10 −0.05	0.01 +0.004 −0.002

Package Outlines

μPD7507C-XXX
μPD7508C-XXX
μPD7508AC-XXX







6

PRELIMINARY

μPD7501
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER WITH LCD CONTROLLER/DRIVER

Description

The μPD7501 is a CMOS 4-bit single chip microcomputer which has the μPD750x architecture.

The μPD7501 contains a 1024 x 8-bit ROM, and a 96 x 4-bit RAM.

The μPD7501 contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7501 typically executes 63 instructions of the μPD7500 series "B" instruction set with a 10μs instruction cycle time.

The μPD7501 has two external and two internal edge-triggered testable interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements. The on-board LCD controller/driver supervises all of the timing required by the 24 Port S segment drivers and the 4 Port COM backplane drivers, for either a 12-digit 7-segment quadriplexed LCD, or an 8-digit 7-segment triplexed LCD.

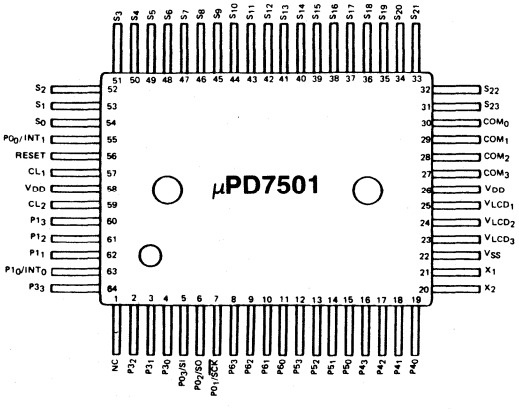
The μPD7501 provides 24 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit input Port 1, the 4-bit output Port 3, and the 4-bit I/O Ports 4, 5, and 6. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7501 is available in a space-saving 64-pin flat plastic package.

The μPD7501 is upward compatible with the μPD7502 and the μPD7503.

Pin Identification

Pin No.	Pin Symbol	Function
1	NC	No connection.
2-4, 64	$P3_3$-$P3_0$	4-bit latched tri-state output Port 3 (active high).
5	$P0_3$/SI	4-bit input Port 0/serial I/O interface (active high).
6 7 55	$P0_2$/SO $P0_1$/$\overline{SCK}$ $P0_0$/INT_1	This port can be configured either as a parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer, comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_1.
8-11	$P6_3$-$P6_0$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
12-15	$P5_3$-$P5_0$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
16-19	$P4_3$-$P4_0$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
20, 21	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
22	V_{SS}	Ground.
23-25	V_{LCD_3}, V_{LCD_2}, V_{LCD_1}	LCD bias voltage supply inputs to LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.
26, 58	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
27-30	COM_3-COM_0	LCD backplane driver outputs.
31-54	S_{23}-S_0	LCD segment driver outputs.
56	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7501 after power-up.
57, 59	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
60-63	$P1_3$-$P1_0$ (PI_0/INT_0)	4-bit input Port 1 (active high). Line $P1_0$ is also shared with external interrupt INT_0.

Pin Configuration



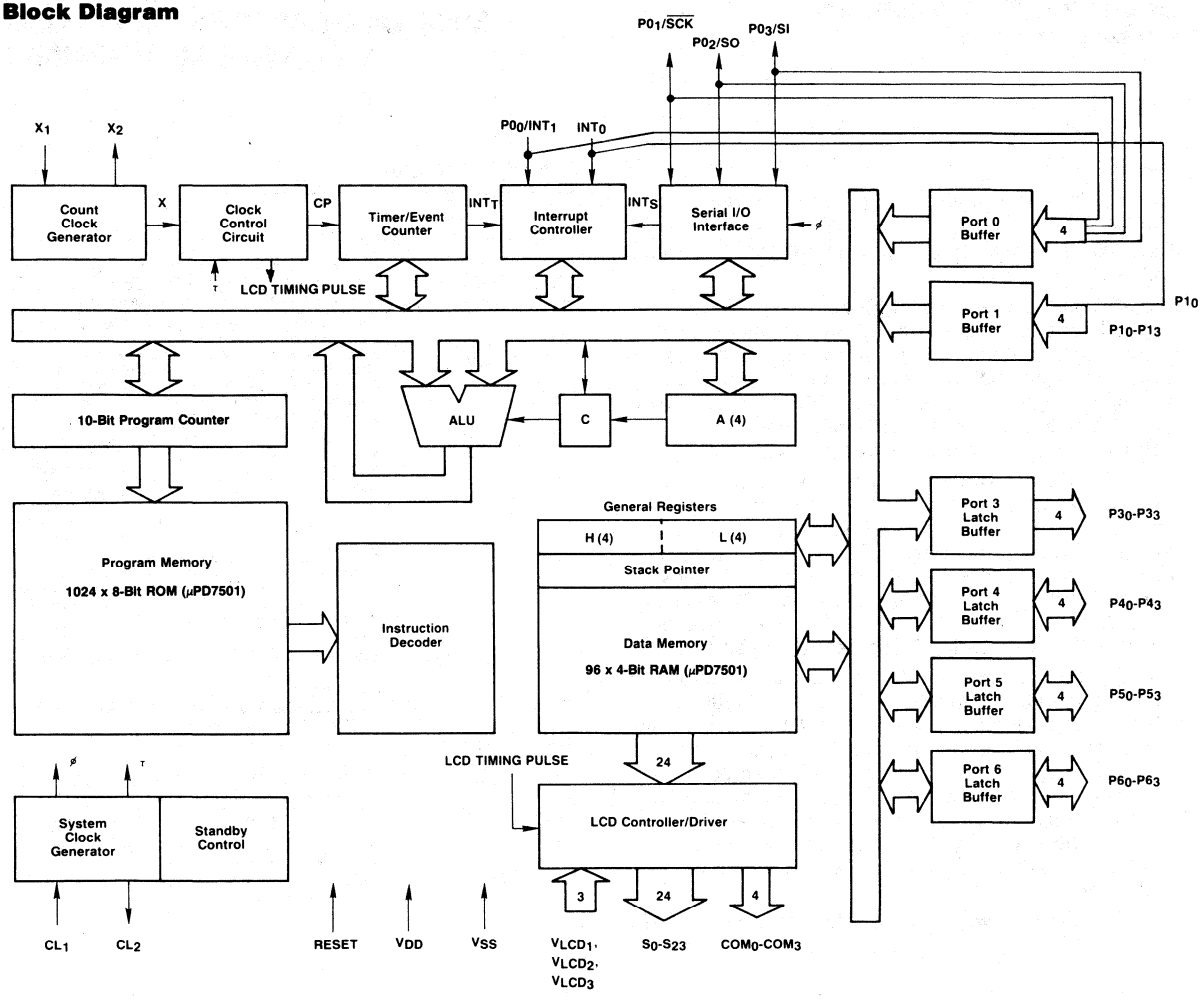
Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA I_{OL} = 30mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6

Block Diagram



DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi H}$	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi L}$	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other than CL_1, X_1	$V_I = V_{DD}$
	$I_{L\phi_H}$			10		CL_1, X_1	
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	$I_{L\phi_L}$			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0 mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100 μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400 μA	
Output Leakage Current High	I_{LO_H}			3	μA	$V_O = V_{DD}$	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Output Impedance	R_{COM}			5	kΩ	COM_0 to COM_3, 2.7V ≤ V_{LCD} ≤ V_{DD}	V_{DD} = 5V ± 10%
			5				V_{DD} = 2.7V to 5.5V
	R_S			20		S_0 to S_{23}, 2.7V ≤ V_{LCD} ≤ V_{DD}	V_{DD} = 5V ± 10%
			20				V_{DD} = 2.7V to 5.5V
Supply Voltage	V_{DDDR}	2.0			V	Data Retention Mode	
Supply Current	I_{DD_O}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			150	400			V_{DD} = 3V ± 10%
	I_{DD_S}		2	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.5	10			V_{DD} = 3V ± 10%
	I_{DDDR}		0.4	10		Data Retention Mode	V_{DDDR} = 2.0V

AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
System Clock Oscillation Frequency	t_ϕ	120	200	280	KHz	CL_1, CL_2 R/C Clock R = 82 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 5V ± 10%
		60	100	130		R = 160 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
	$t_{\phi Ext}$	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	$t_{r\phi}$, $t_{f\phi}$			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	$t_{\phi W_H}$, $t_{\phi W_L}$	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_x	25	32	50	KHz	X_1, X_2 Crystal Oscillator	
	f_{xExt}	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{rx}, t_{fx}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{xW_H}, t_{xW_L}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Cycle Time	t_{CY_K}	4.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Pulse Width	t_{KW_H}, t_{KW_L}	1.8			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7v to 5.5V
		3.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
SI Setup Time to $\overline{SCK}$↑	t_{IS}	300			ns		
SI Hold Time after $\overline{SCK}$↑	t_{IH}	450			ns		
SO Delay Time after $\overline{SCK}$↓	t_{OD}			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	$t_{I_0W_H}$, $t_{I_0W_L}$	10			μs		
INT_1 Pulse Width	$t_{I_1W_H}$, $t_{I_1W_L}$	$2/f_\phi$			μs		
RESET Pulse Width	t_{RW_H}, t_{RW_L}	10			μs		
RESET Setup Time	t_{RS}	0			ns		
RESET Hold Time	t_{RH}	0			ns		

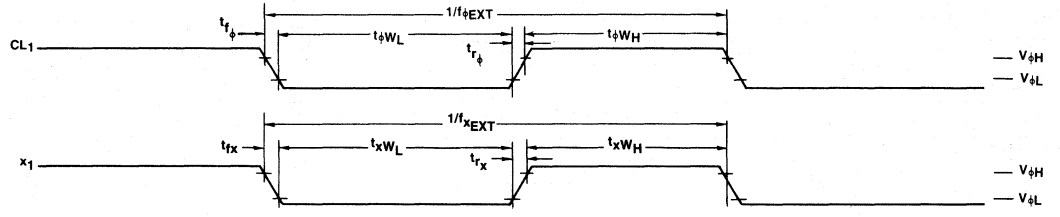
Capacitance

T_a = 25°C, V_{DD} = 0V

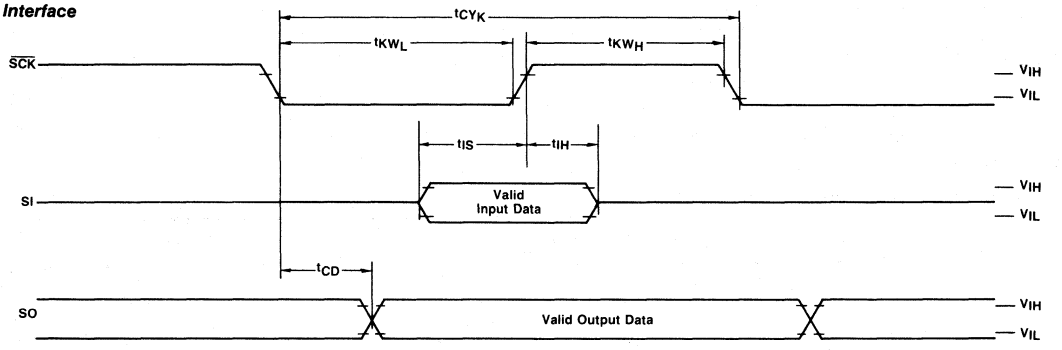
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			15		

Timing Waveforms

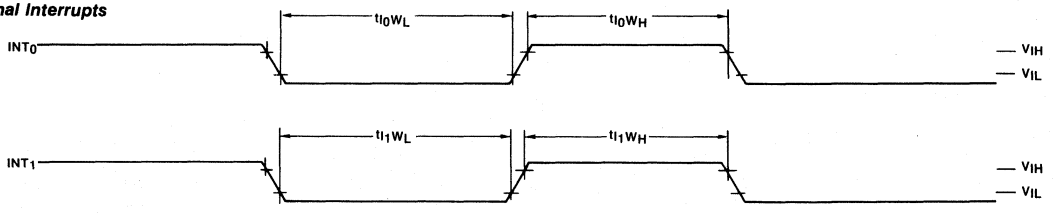
Clocks



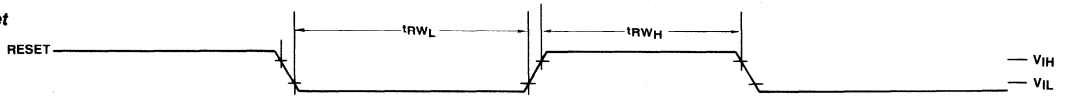
Serial Interface



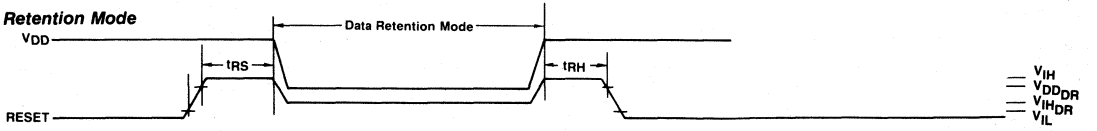
External Interrupts



Reset



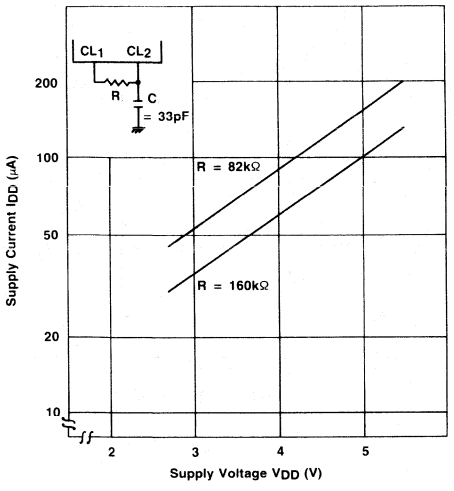
Data Retention Mode



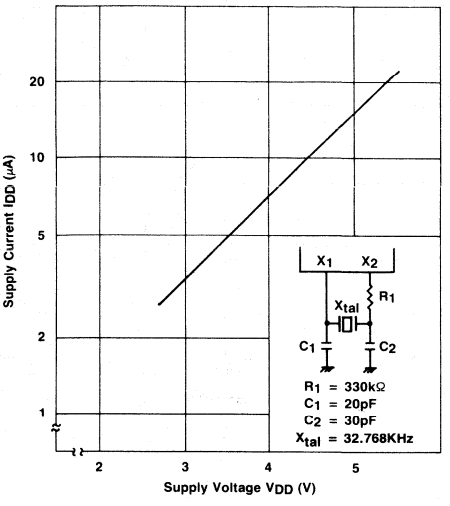
Operating Characteristics

Typical, T_a = 25°C

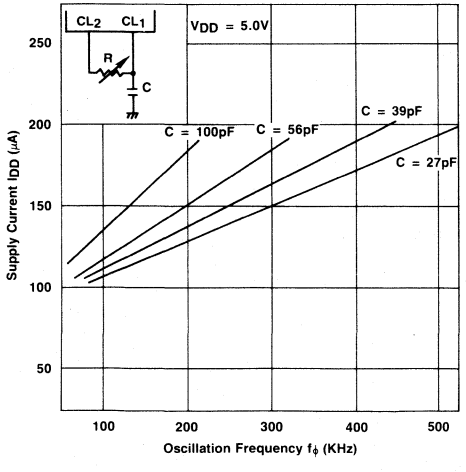
Supply Current vs Supply Voltage (Note ①)



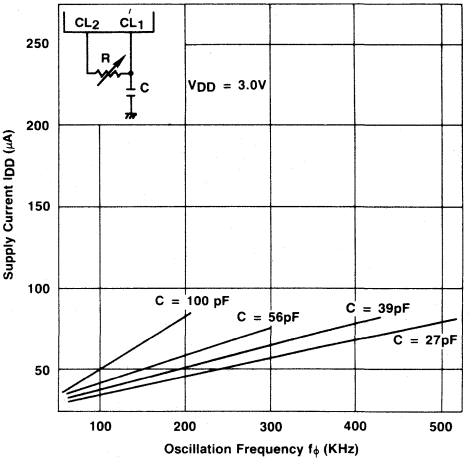
Supply Current vs Supply Voltage (Note ②)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Notes:

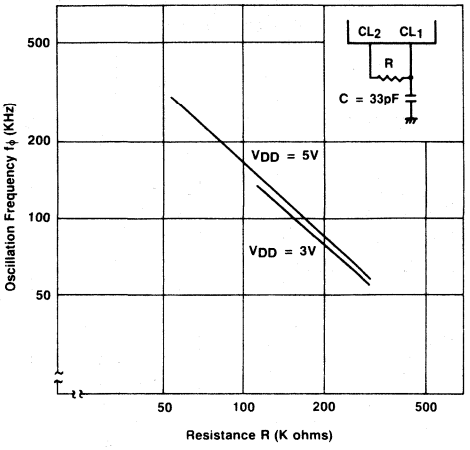
① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.

② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

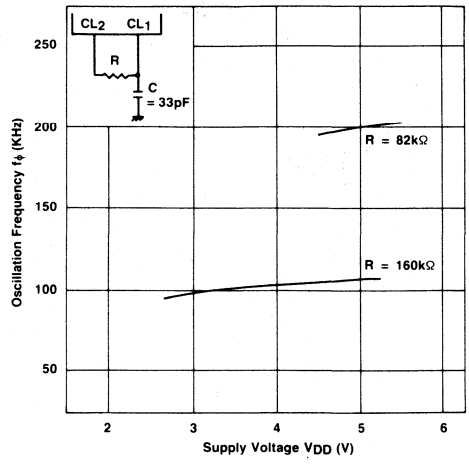
Operating Characteristics (Cont.)

Typical, T_a = 25°C

System Clock Oscillation Frequency
vs
Resistance



System Clock Oscillation Frequency
vs
Supply Voltage



μPD7502
μPD7503
CMOS 4-BIT SINGLE CHIP MICROCOMPUTERS WITH LCD CONTROLLER/DRIVER

Description

The μPD7502 and the μPD7503 are pin-compatible CMOS 4-bit single chip microcomputers which have the same μPD750x architecture.

The μPD7502 contains a 2048 x 8-bit ROM, and a 128 x 4-bit RAM. The μPD7503 contains a 4096 x 8-bit ROM, and a 224 x 4-bit RAM.

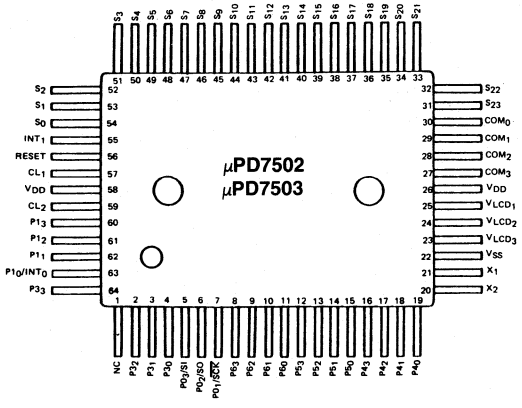
Both the μPD7502 and the μPD7503 contain four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7502 and the μPD7503 typically execute 92 instructions of the μPD7500 series "A" instruction set with a 10μs instruction cycle time.

The μPD7502 and the μPD7503 have two external and two internal edge-triggered hardware vectored interrupts. They also contain an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements. The on-board LCD controller/driver supervises all of the timing required by the 24 Port S segment drivers and the 4 Port COM backplane drivers, for either a 12-digit 7-segment quadriplexed LCD, or an 8-digit 7-segment triplexed LCD.

Both the μPD7502 and the μPD7503 provide 23 I/O lines, organized into the 3-bit input/serial interface Port 0, the 4-bit input Port 1, the 4-bit output Port 3, and the 4-bit I/O Ports 4, 5, and 6. They are manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7502 and the μPD7503 are available in a space-saving 64-pin flat plastic package.

The μPD7502 is downward compatible with the μPD7501.

Pin Configuration



Pin Names

Pin No.	Symbol	Function
1	NC	No connection.
2-4, 64	$P3_3$-$P3_0$	4-bit latched tristate output Port 3 (active high).
5	$P0_3$/SI	3-bit input Port 0/serial I/O interface (active high).
6	$P0_2$/SO	This port can be configured either as a parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active high), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer, comprise the 8-bit serial I/O interface.
7	$P0_1/\overline{SCK}$	
8-11	$P6_3$-$P6_0$	4-bit input/latched tristate output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
12-15	$P5_3$-$P5_0$	4-bit input/latched tristate output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
16-19	$P4_3$-$P4_0$	4-bit input/latched tristate output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
20, 21	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
22	V_{SS}	Ground.
23-25	V_{LCD_3}, V_{LCD_2}, V_{LCD_1}	LCD bias voltage supply inputs to LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.
26, 58	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
27-30	COM_3-COM_0	LCD backplane driver outputs.
31-54	S_{23}-S_0	LCD segment driver outputs.
55	INT_1	External Interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
56	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7502 or μPD7503 after power-up.
57, 59	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
60-63	$P1_3$-$P1_0$ (PI_0/INT_0)	4-bit input Port 1 (active high). Line $P1_0$ is also shared with external interrupt INT_0, which is a rising edge-triggered interrupt.

Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 30mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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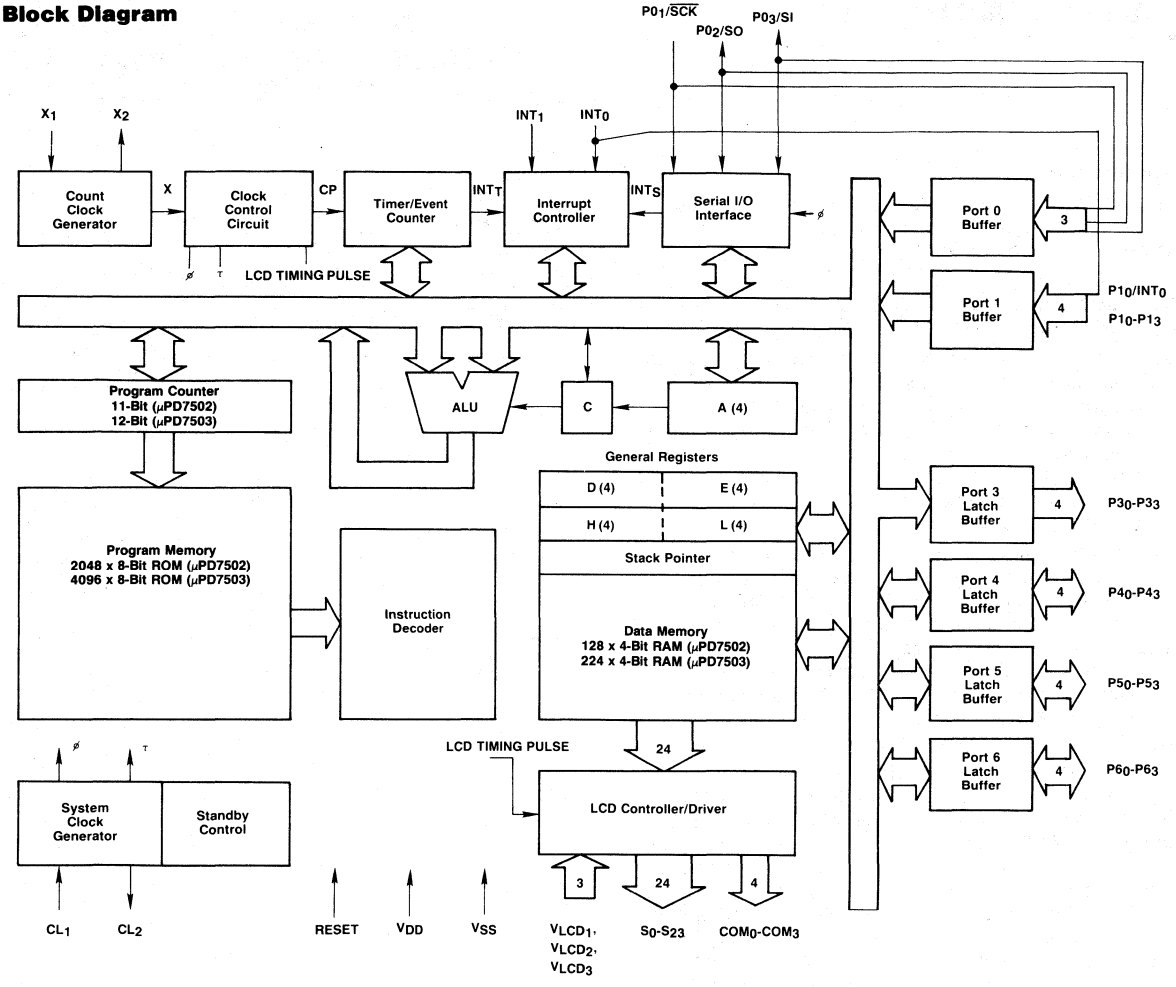
Block Diagram



Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1 MHz,
Output Capacitance	C_O			15	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			15		

DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi H}$	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	$V_{IH_{DR}}$	0.9 $V_{DD_{DR}}$		$V_{DD_{DR}}$ + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi L}$	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other than CL_1, X_1	V_I = V_{DD}
	$I_{L\phi_H}$			10		CL_1, X_1	
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	$I_{L\phi_L}$			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0 mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100 μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400 μA	
Output Leakage Current High	I_{LO_H}			3	μA	V_O = V_{DD}	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Output Impedance	R_{COM}			5	kΩ	COM_0 to COM_3, 2.7V ≤ V_{LCD} ≤ V_{DD}	V_{DD} = 5V ± 10%
			5				V_{DD} = 2.7V to 5.5V
	R_S			20		S_0 to S_{23}, 2.7V ≤ V_{LCD} ≤ V_{DD}	V_{DD} = 5V ± 10%
			20				V_{DD} = 2.7V to 5.5V
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_O}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			150	400			V_{DD} = 3V ± 10%
	I_{DD_S}		2	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.5	10			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode	$V_{DD_{DR}}$ = 2.0V

AC Characteristics

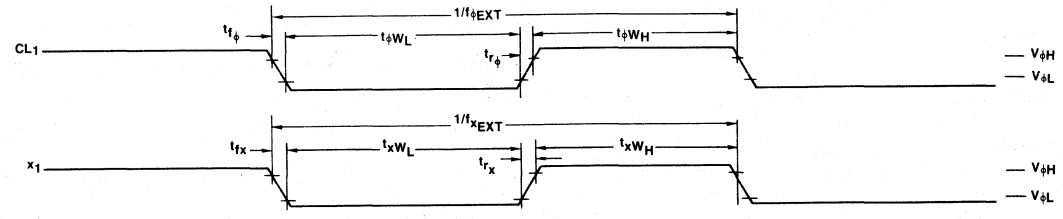
T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
System Clock Oscillation Frequency	f_ϕ	120	200	280	kHz	R = 82 kΩ ± 2%, C = 33 pF ± 5%	V_{DD} = 5V ± 10%
		60	100	130		CL_1, CL_2 R = 160 kΩ ± 2%, R/C Clock C = 33 pF ± 5%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
	$f_{\phi_{Ext}}$	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	$t_{r\phi}$, $t_{f\phi}$			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	$t_\phi W_H$, $t_\phi W_L$	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_x	25	32	50	kHz	X_1, X_2 Crystal Oscillator	
	$f_{x_{Ext}}$	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{rx}, t_{fx}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{xW_H}, t_{xW_L}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Cycle Time	t_{CY_K}	4.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Pulse Width	t_{KW_H}, t_{KW_L}	1.8			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7v to 5.5V
		3.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
SI Setup Time to SCK↑	t_{IS}	300			ns		
SI Hold Time after SCK↑	t_{IH}	450			ns		
SO Delay Time after $\overline{SCK}$↓	t_{OD}			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	$t_{I_0W_H}$, $t_{I_0W_L}$	10			μs		
INT_1 Pulse Width	$t_{I_1W_H}$, $t_{I_1W_L}$	$2/f_\phi$			μs		
RESET Pulse Width	t_{RW_H}, t_{RW_L}	10			μs		
RESET Setup Time	t_{RS}	0			ns		
RESET Hold Time	t_{RH}	0			ns		

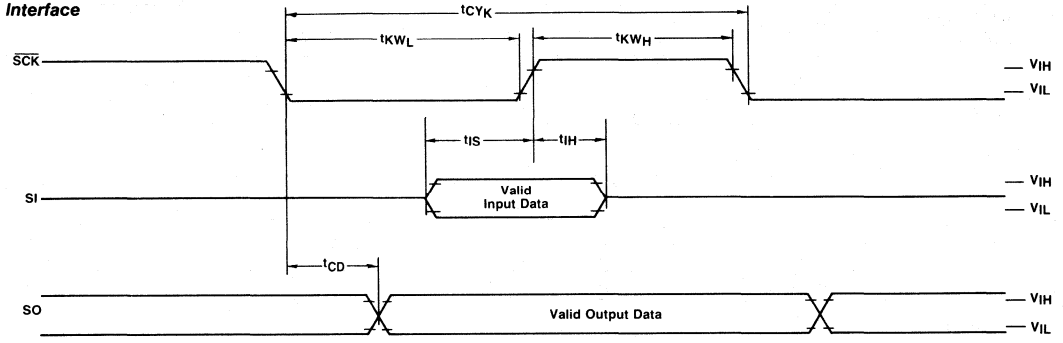
6

Timing Waveforms

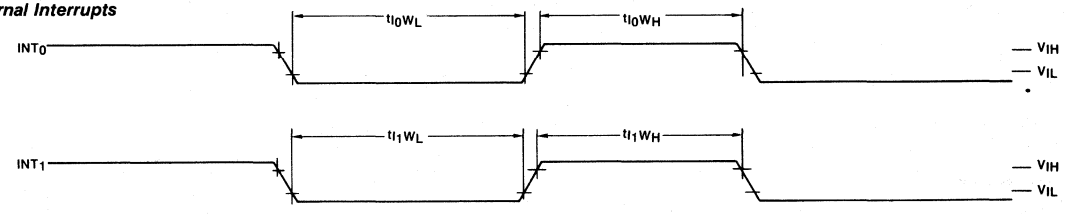
Clocks



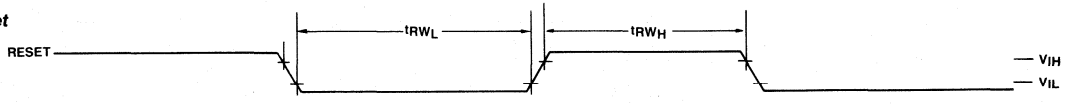
Serial Interface



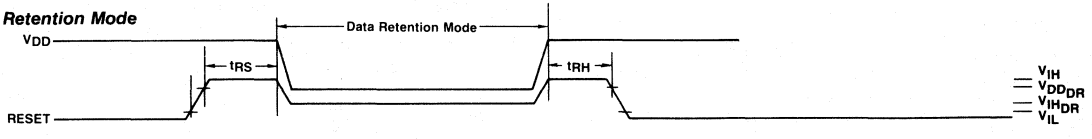
External Interrupts



Reset



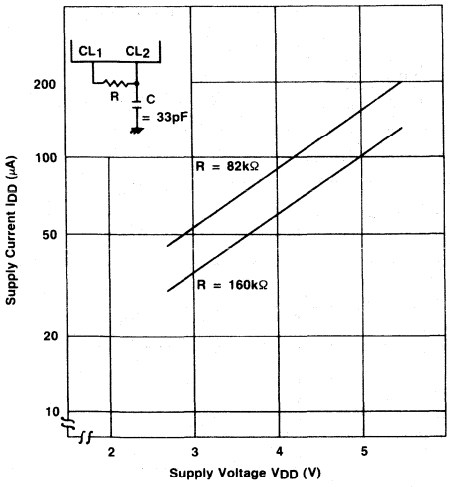
Data Retention Mode



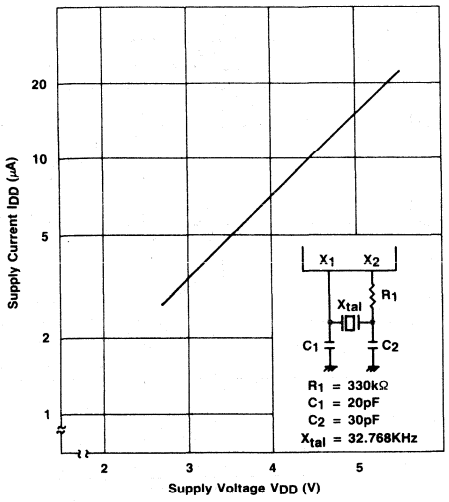
Operating Characteristics

Typical, T_a = 25°C

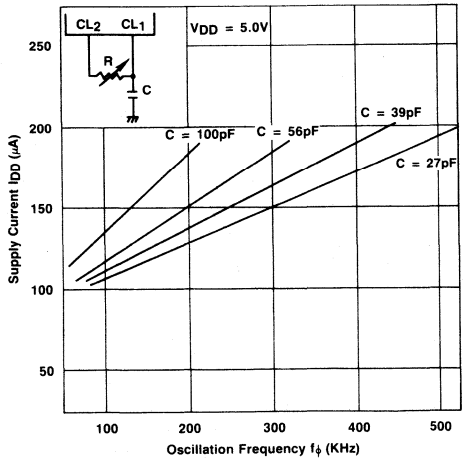
Supply Current vs Supply Voltage (Note ①)



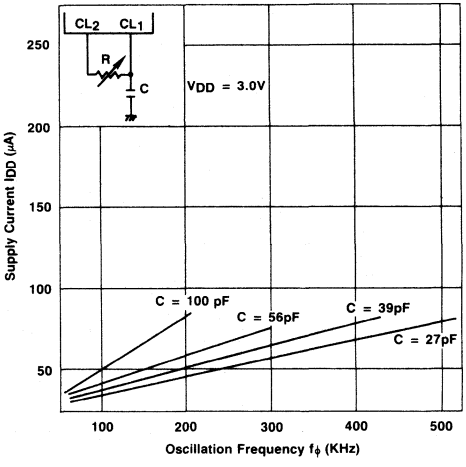
Supply Current vs Supply Voltage (Note ②)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Notes:

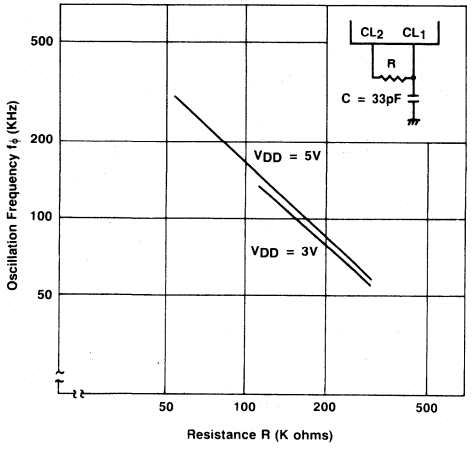
① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.

② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

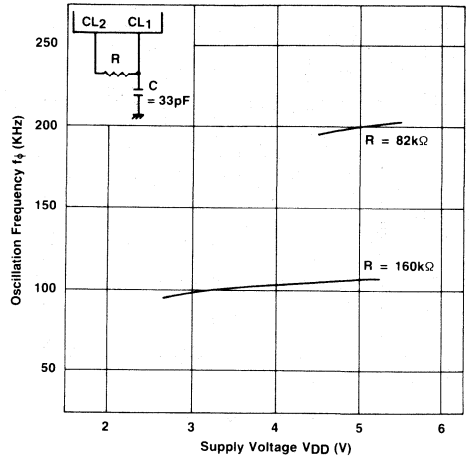
Operating Characteristics (Cont.)

Typical, T_a = 25°C

System Clock Oscillation Frequency
vs
Resistance



System Clock Oscillation Frequency
vs
Supply Voltage



μPD7506
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

Description

The μPD7506 is a CMOS 4-bit single chip microcomputer which has the μPD750x architecture.

The μPD7506 contains a 1024 x 8-bit ROM, and a 64 x 4-bit RAM.

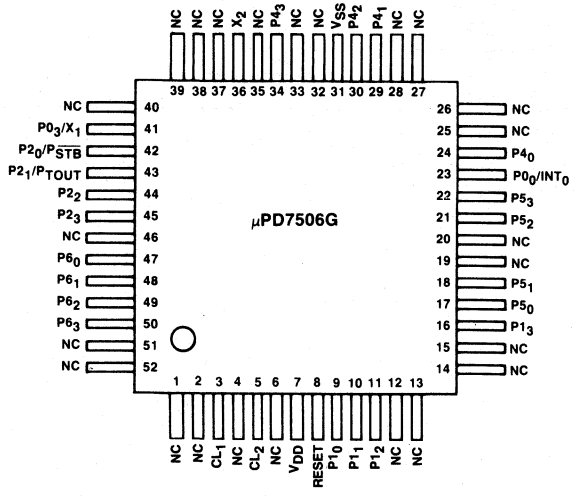
The μPD7506 contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7506 typically executes 58 instructions of the μPD7500 series "B" instruction set with a 10μs instruction cycle time.

The μPD7506 has one external and one internal edge-triggered testable interrupts. It also contains an 8-bit timer/event counter to help reduce software requirements.

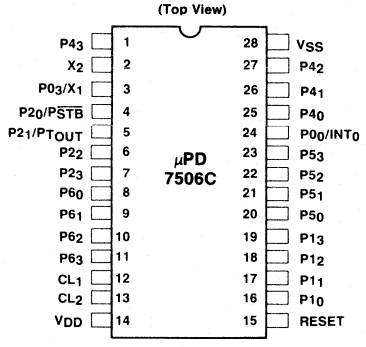
The μPD7506 provides 22 I/O lines, organized into the 2-bit input Port 0, the 4-bit output Port 2, and the 4-bit I/O Ports 1, 4, 5, and 6. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 600μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7506 is available either in a 28-pin dual-in-line plastic package, or in a space-saving 52-pin flat plastic package.

The μPD7506 is upward compatible with the μPD7507 and the μPD7507S.

Pin Configuration



Pin Configuration (Cont.)



Pin Names

40-Pin DIP	52-Pin Flat	Symbol	Function
1, 25-27	24, 29, 30, 34	$P4_0$-$P4_3$	4-bit input/latched tristate output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
2, 3	36, 41	X_2,$P0_3$/ X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting. Line X_1 is always shared with Port 0 input $P0_3$.
4-7	42-45	$P2_0$-$P2_3$ $P2_0$/$\overline{STB}$ $P2_1$/PT_{OUT}	4-bit latched tristate output Port 2 (active high). Line $P2_0$ is also shared with $\overline{STB}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with PT_{OUT}, the timer-out F/F signal (active high).
8-11	47-50	$P6_0$-$P6_3$	4-bit input/latched tristate output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
12, 13	3, 5	CL_1, CL_2	System clock input (active high). Connect 120kΩ resistor across CL_1 and CL_2. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
14	7	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
15	8	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7507 or μPD7508 after power-up.
16-19	9-11, 16	$P1_0$-$P1_3$	4-bit input/tristate output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0$/$\overline{STB}$ pulse.
20-23	16-18, 21	$P5_0$-$P5_3$	4-bit input/latched tristate output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
24, 3	23, 41	$P0_0$/INT_0 $P0_3$/X_1	2-bit input Port 0 (active high). Line $P0_0$ is always shared with external interrupt INT_0 (active high). Line $P0_3$ is always shared with crystal clock/external event input X_1 (active high).
28	31	V_{SS}	Ground.
—	1, 2, 4, 6 12-15, 19, 20, 25-28, 32, 33, 35, 37-40, 46, 51, 52	NC	No connection.

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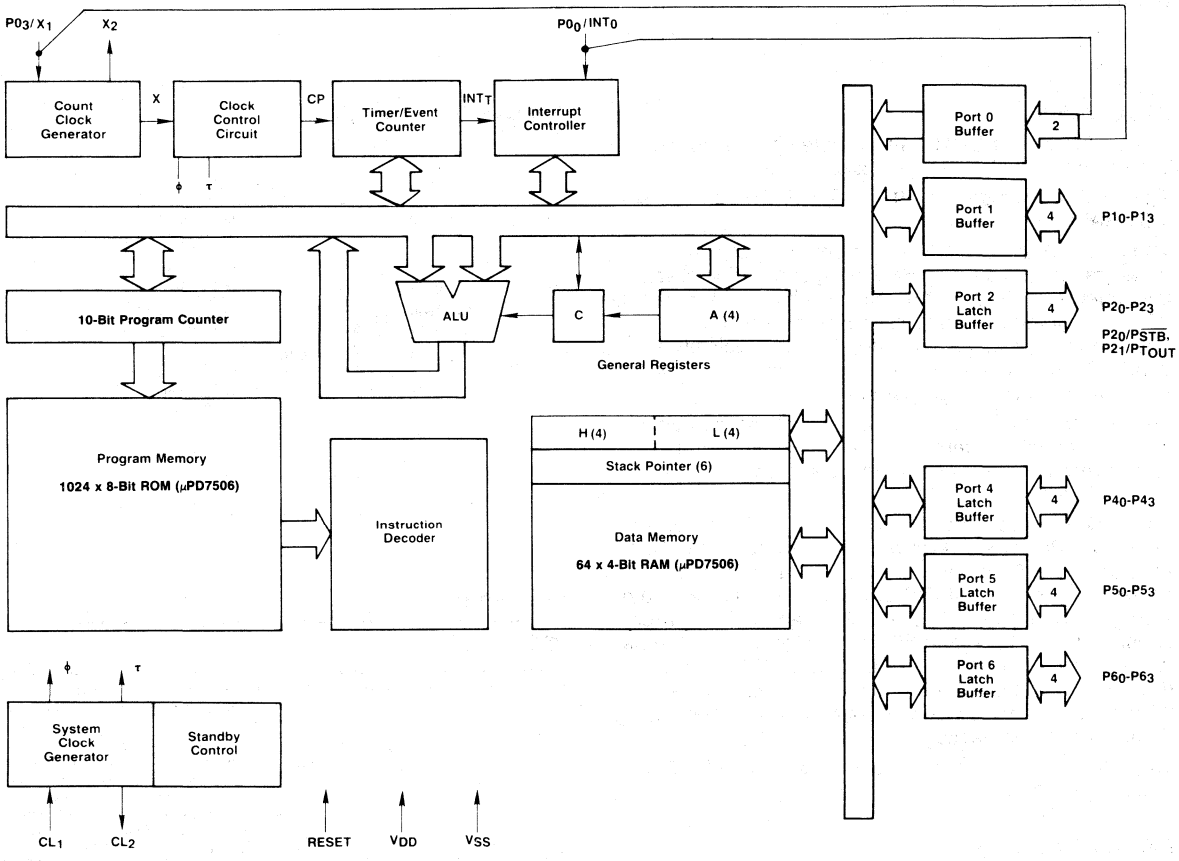
Block Diagram



Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 32mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1MHz, Unmeasured pins returned to V_{SS}
Output Capacitance	C_O			15		
Input/Output Capacitance	$C_{I/O}$			15		

DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi H}$	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	$V_{IH_{DR}}$	0.9 $V_{DD_{DR}}$		$V_{DD_{DR}}$ + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi L}$	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other than CL_1, X_1	V_I = V_{DD}
	$I_{L\phi_H}$			10		CL_1, X_1	
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	$I_{L\phi_L}$			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400μA	
Output Leakage Current High	I_{LO_H}			3	μA	V_O = V_{DD}	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_O}		200	600	μA	Normal Operation	V_{DD} = 5V ± 10%
			100	300			V_{DD} = 3V ± 10%
	I_{DD_S}		1	10		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.3	5			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode	$V_{DD_{DR}}$ = 2.0V

AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
System Clock Oscillation Frequency	f_ϕ	120	200	260	kHz	R = 120 kΩ ± 2%	V_{DD} = 5V ± 10%
		60	100	130		CL_1, CL_2 R = 240 kΩ ± 2%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
	$f_{\phi Ext}$	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	$t_{r\phi}$, $t_{f\phi}$			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	$t_{\phi W_H}$, $t_{\phi W_L}$	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_X	25	32	50	kHz	X_1, X_2 Crystal Oscillator	
	$f_{X_{Ext}}$	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{rx}, t_{fx}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{xW_H}, t_{xW_L}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
Port 1 Output Setup Time to $P_{\overline{STB}}$↑	t_{P_1S}	1/(2f_ϕ-800)			ns	V_{DD} = 5V ± 10%	
		1/(2f_ϕ-2000)				V_{DD} = 2.7V to 5.5V	
Port 1 Output Hold Time after $P_{\overline{STB}}$↑	t_{P_1H}	300	350	500	ns	V_{DD} = 5V ± 10%	
		300		1500		V_{DD} = 2.7V to 5.5V	
$P_{\overline{STB}}$ Pulse Width	t_{SW_L}	1/(2f_ϕ-800)			ns	V_{DD} = 5V ± 10%	
		1/(2f_ϕ-2000)				V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	$t_{I_0W_H}$, $t_{I_0W_L}$	10			μs		
RESET Pulse Width	t_{RW_H}, t_{RW_L}	10			μs		
RESET Setup Time	t_{RS}	0			ns		
RESET Hold Time	t_{RH}	0			ns		

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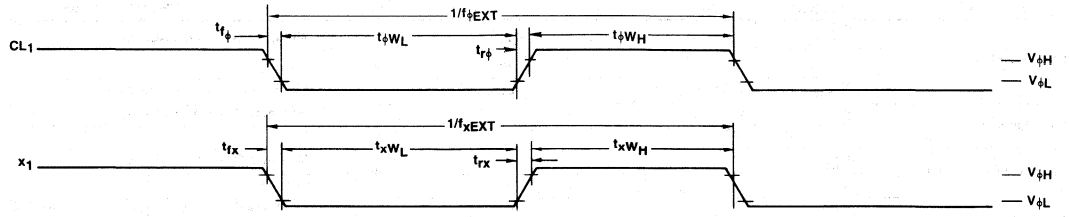
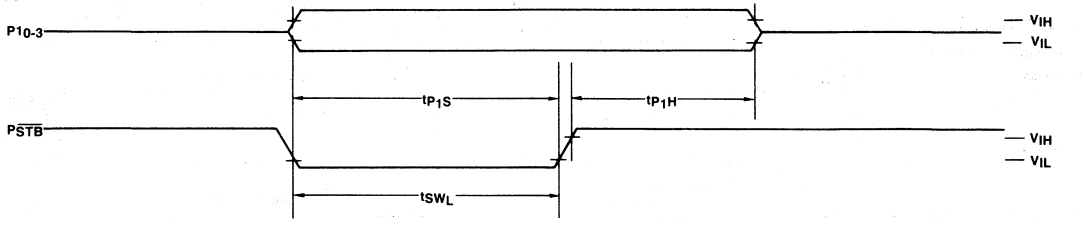
Timing Waveforms

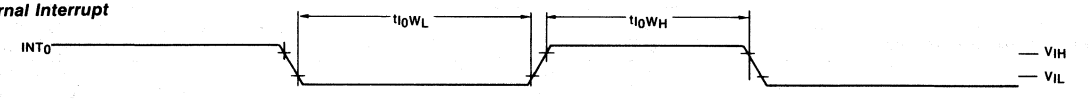
Clocks



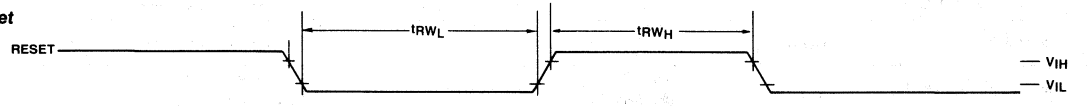
Output Strobe



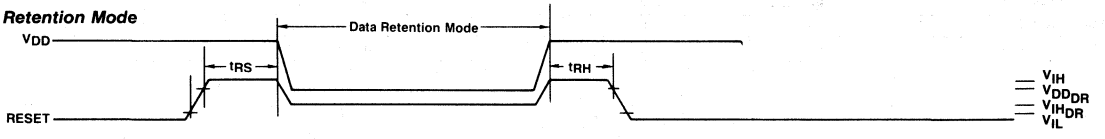
External Interrupt



Reset



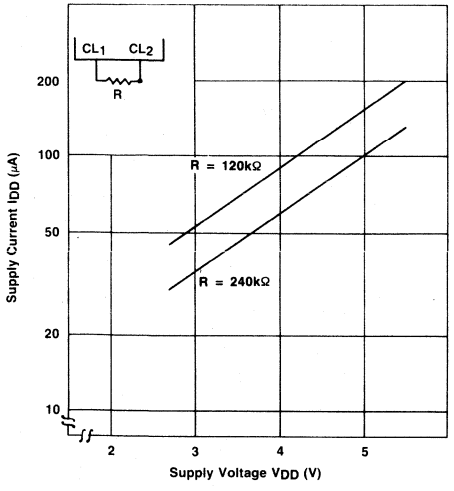
Data Retention Mode



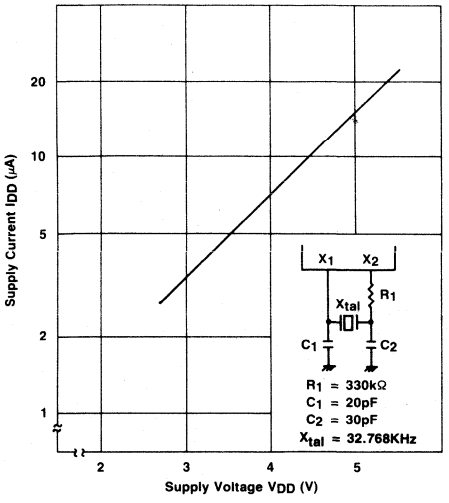
Operating Characteristics

Typical, T_a = 25°C

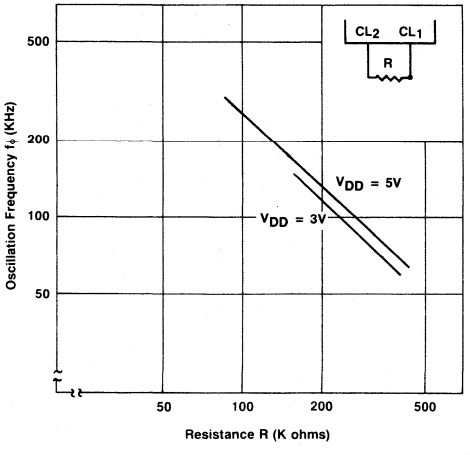
Supply Current vs Supply Voltage (Note ①)



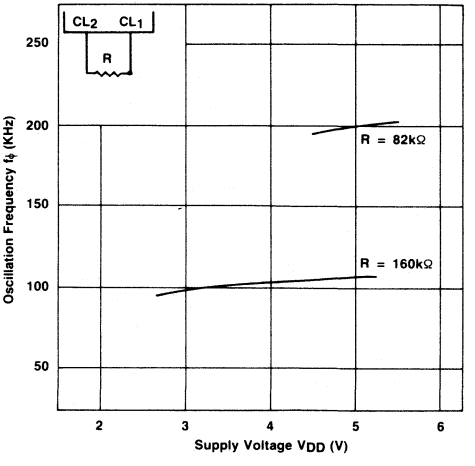
Supply Current vs Supply Voltage (Note ②)



System Clock Oscillation Frequency vs Resistance



System Clock Oscillation Frequency vs Supply Voltage



Notes:

① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.

② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

μPD7507
μPD7508
CMOS 4-BIT SINGLE CHIP MICROCOMPUTERS

Description

The μPD7507 and the μPD7508 are pin-compatible CMOS 4-bit single chip microcomputers which have the same μPD750x architecture.

The μPD7507 contains a 2048 x 8-bit ROM, and a 128 x 4-bit RAM. The μPD7508 contains a 4096 x 8-bit ROM, and a 224 x 4-bit RAM.

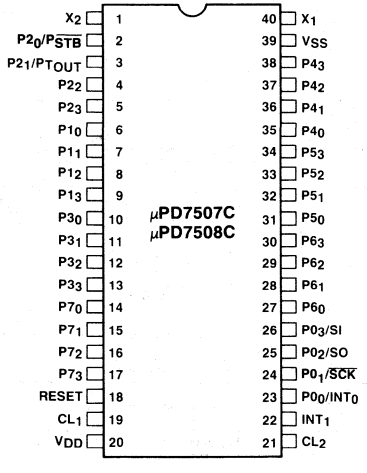
Both the μPD7507 and the μPD7508 contain four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7507 and the μPD5708 typically execute 92 instructions of the μPD7500 series "A" instruction set with a 10μs instruction cycle time.

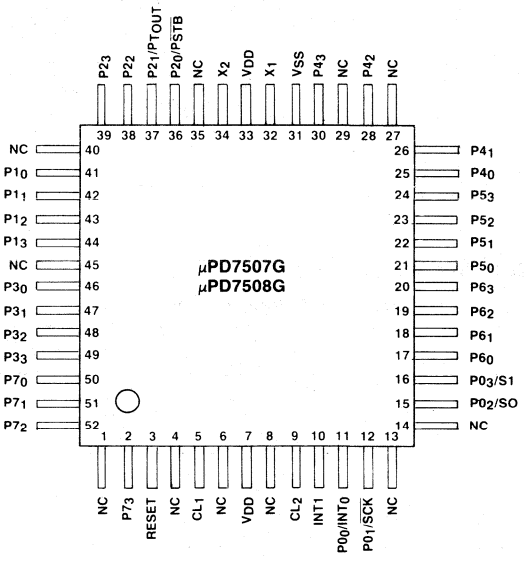
The μPD7507 and the μPD7508 have two external and two internal edge-triggered hardware vectored interrupts. They also contain an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

Both the μPD7507 and the μPD7508 provide 32 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit input Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, 6, and 7. They are manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7507 and the μPD7508 are available in either a 40-pin dual-in-line plastic package or in a space-saving 52-pin flat plastic package.

The μPD7507 is downward compatible with the μPD7506 and the μPD7507S.

Pin Configuration





Pin Identification

40-Pin DIP	52-Pin Flat	Symbol	Function
1, 40	32, 34	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
2-5	36-39	$P2_0$-$P2_3$ $P2_0/\overline{PSTB}$ $P2_1/PT_{OUT}$	4-bit latched tri-state output Port 2 (active high). Line $P2_0$ is also shared with $\overline{PSTB}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with PT_{OUT}, the timer-out F/F signal (active high).
6-9	41-44	$P1_0$-$P1_3$	4-bit input/tri-state output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0/\overline{PSTB}$ pulse.
10-13	46-49	$P3_0$-$P3_3$	4-bit input/latched tri-state output Port 3 (active high).
14-17	50-52, 2	$P7_0$-$P7_3$	4-bit input/latched tri-state output Port 7 (active high).
18	3	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7507 or μPD7508 after power-up.
19, 21	5, 9	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
20	7, 33	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
22	10	INT_1	External Interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
23-26	11, 12 15, 16	$P0_0/INT_0$ $P0_1/\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input Port 0/Serial I/O Interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_0 (active high) which is a rising edge-triggered interrupt.

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Pin Identification (Cont.)

40-Pin DIP	52-Pin Flat	Symbol	Function
27-30	17-20	$P6_0$-$P6_3$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
31-34	21-24	$P5_0$-$P5_3$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
35-38	25, 26, 28, 30	$P4_0$-$P4_3$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
39	31	V_{SS}	Ground.
—	1, 4, 6, 8, 13, 14, 27, 29, 35, 40, 45	NC	No connection.

Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 30mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi H}$	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi L}$	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other than CL_1, X_1	V_I = V_{DD}
	$I_{L\phi_H}$			10		CL_1, X_1	
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	$I_{L\phi_L}$			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0 mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100 μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400 μA	
Output Leakage Current High	I_{LO_H}			3	μA	V_O = V_{DD}	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Supply Voltage	V_{DDDR}	2.0			V	Data Retention Mode	
Supply Current	I_{DD_O}		300	900		Normal Operation	V_{DD} = 5V ± 10%
			150	400			V_{DD} = 3V ± 10%
	I_{DD_S}		2	20	μA	Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.5	10			V_{DD} = 3V ± 10%
	I_{DDDR}		0.4	10		Data Retention Mode	V_{DDDR} = 2.0V

AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
System Clock Oscillation Frequency	f_ϕ	120	200	280	KHz	CL_1, CL_2 R = 120 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 5V ± 10%
		60	100	130		R = 250 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
	$f_{\phi EXT}$	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	$t_{r\phi}$, $t_{f\phi}$			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	$t_{\phi W_H}$, $t_{\phi W_L}$	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_x	25	32	50	KHz	X_1, X_2 Crystal Oscillator	
	f_{xExt}	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{rx}, t_{fx}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{xW_H}, t_{xW_L}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V

AC Characteristics (Cont.)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
$\overline{SCK}$ Cycle Time	t_{CYK}	4.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Pulse Width	t_{KW_H}, t_{KW_L}	1.8			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7v to 5.5V
		3.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
SI Setup Time to $\overline{SCK}$↑	t_{IS}	300			ns		
SI Hold Time after $\overline{SCK}$↑	t_{IH}	450			ns		
SO Delay Time after $\overline{SCK}$↓	t_{OD}			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
Port 1 Output Setup Time to $P_{\overline{STB}}$↑	t_{P_1S}	1/(2f_ϕ-800)			ns	V_{DD} = 5V ± 10%	
		1/(2f_ϕ-2000)				V_{DD} = 2.7V to 5.5V	
Port 1 Output Hold Time after $P_{\overline{STB}}$↑	t_{P_1H}	300	350	500	ns	V_{DD} = 5V ± 10%	
		300		1500		V_{DD} = 2.7V to 5.5V	
$P_{\overline{STB}}$ Pulse Width	t_{SW_L}	f/(2f_ϕ-800)			ns	V_{DD} = 5V ± 10%	
		f/(2f_ϕ-2000)				V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	$t_{I_0W_H}$, $t_{I_0W_L}$	10			μs		
INT_1 Pulse Width	$t_{I_1W_H}$, $t_{I_1W_L}$	2/f_ϕ			μs		
RESET Pulse Width	t_{RW_H}, t_{RW_L}	10			μs		
RESET Setup Time	t_{RS}	0			ns		
RESET Hold Time	t_{RH}	0			ns		

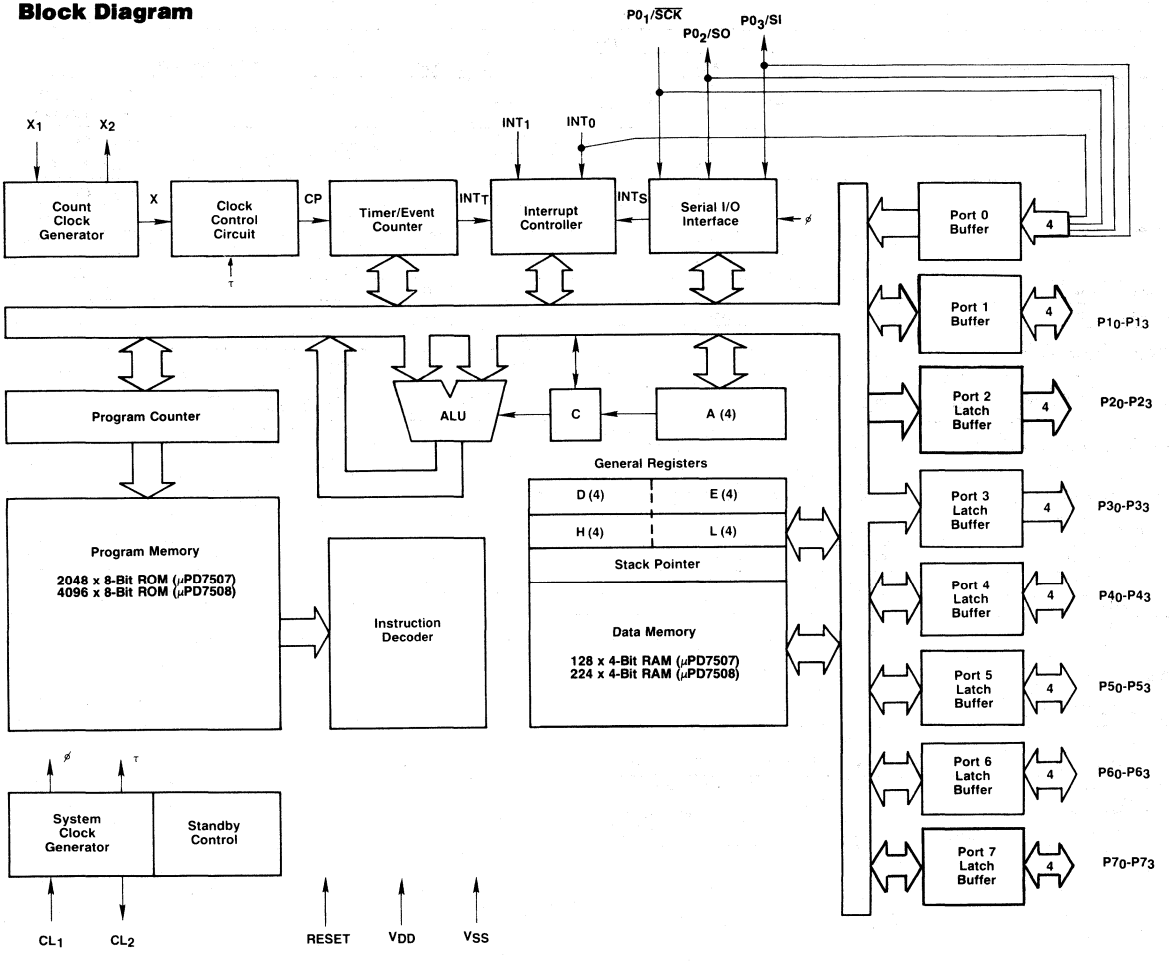
Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			15		

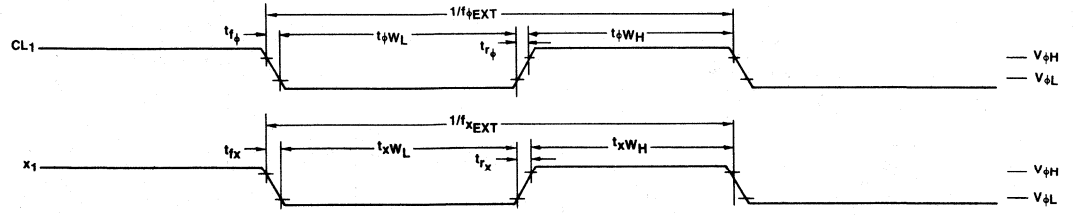
6

Block Diagram

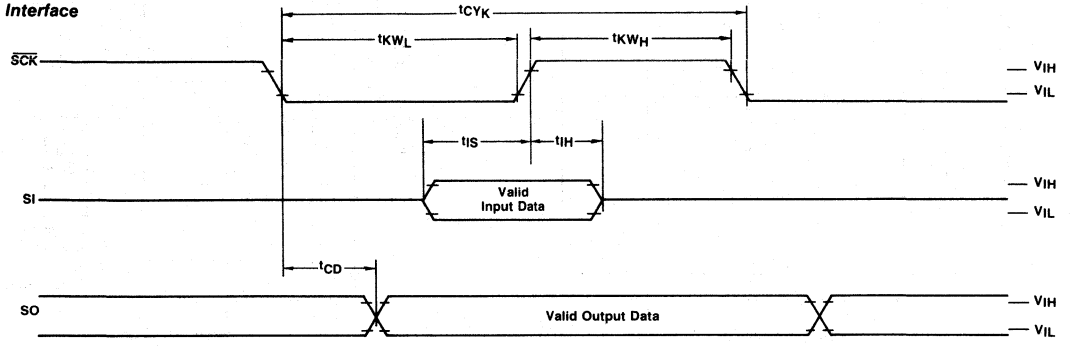


Timing Waveforms

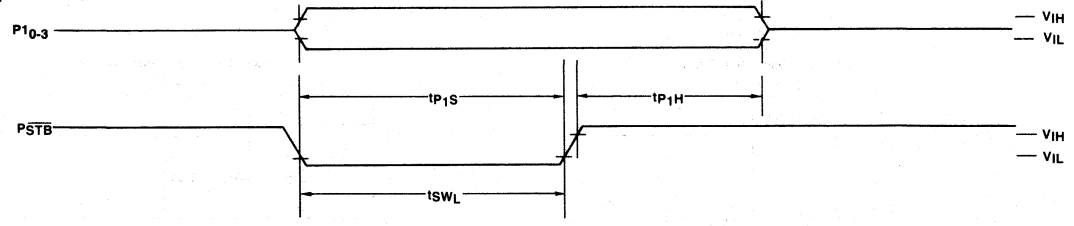
Clocks



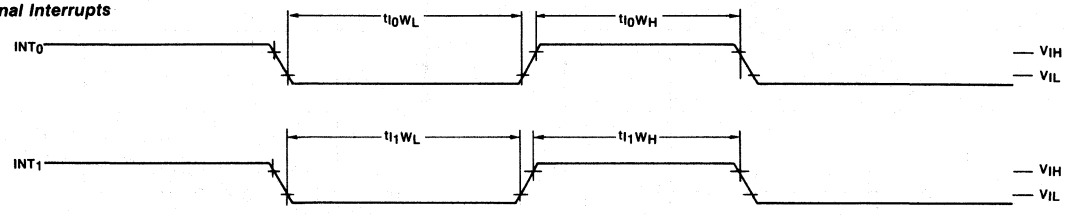
Serial Interface



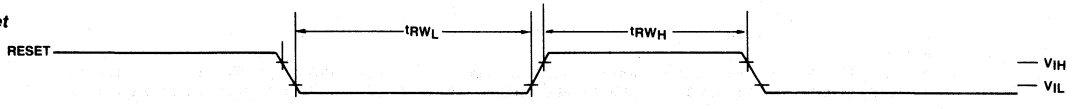
Output Strobe



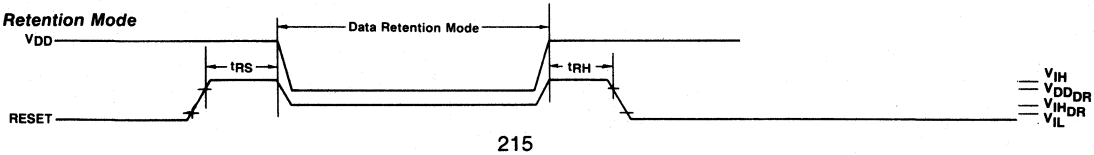
External Interrupts



Reset

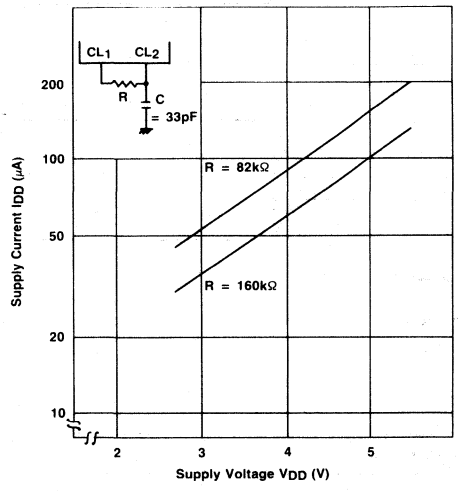


Data Retention Mode

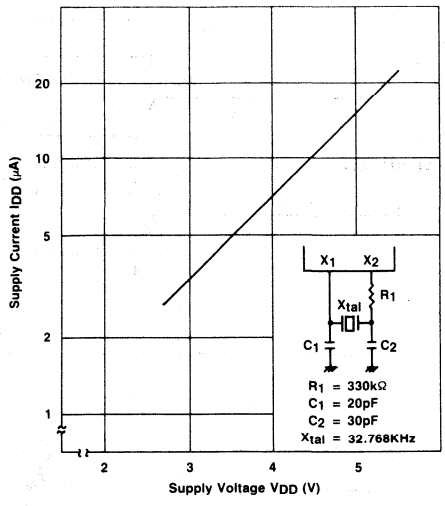


Operating Characteristics (Typical, T_a = 25°C)

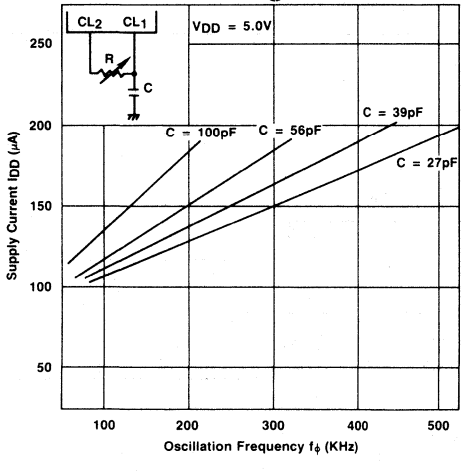
Supply Current vs Supply Voltage (Note ①)



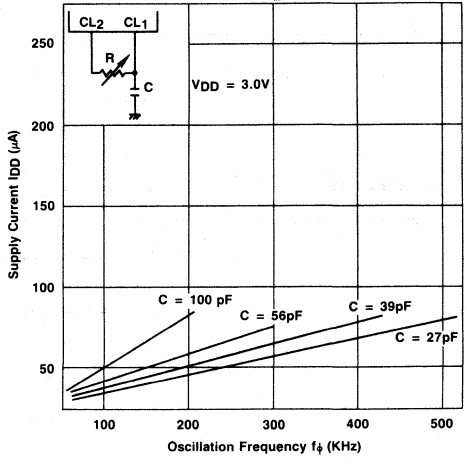
Supply Current vs Supply Voltage (Note ②)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Supply Current vs System Clock Oscillation Frequency Note ①)



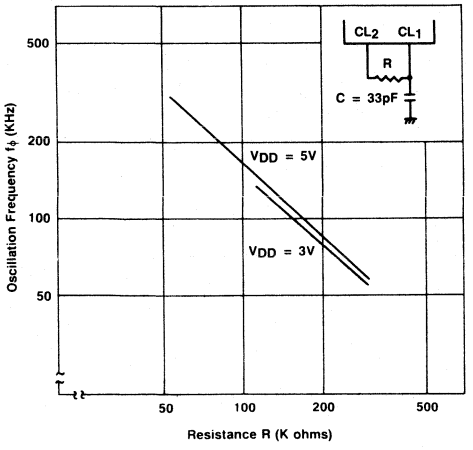
Notes:

① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.

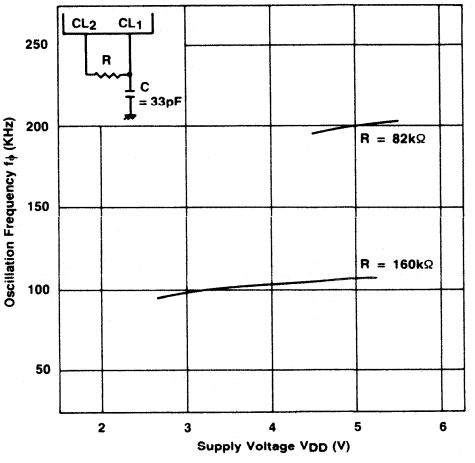
② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

Operating Characteristics (Cont.)
(Typical, T_a = 25°C)

System Clock Oscillation Frequency
vs
Resistance



System Clock Oscillation Frequency
vs
Supply Voltage



6

PRELIMINARY

μPD7507S
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

Description

The μPD7507S is a CMOS 4-bit single chip microcomputer which has the same μPD750x architecture.

The μPD7507S contains a 2048 x 8-bit ROM, and a 128 x 4-bit RAM.

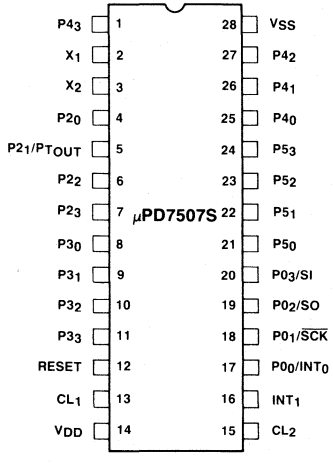
The μPD7507S contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7507S typically executes 91 instructions of the μPD7500 series "A" instruction set with a 10μs instruction cycle time.

The μPD7507S has two external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

The μPD7507S provides 20 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit output Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 4 and 5. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7507S is available in a 28-pin dual-in-line plastic package.

The μPD7507S is upward compatible with the μPD7507, and downward compatible with the μPD7506.

Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Function
1, 25-27	$P4_0$-$P4_3$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
2, 3	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
4-7	$P2_0$-$P2_3$ $P2_1/PT_{OUT}$	4-bit latched tri-state output Port 2 (active high). Line $P2_1$ is shared with PT_{OUT}, the timer-out F/F signal (active high).
8-11	$P3_0$-$P3_3$	4-bit input/latched tri-state output Port 3 (active high).
12	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7507 or μPD7508 after power-up.
13, 15	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
14	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
16	INT_1	External Interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
17-20	$P0_0/INT_0$ $P0_1/\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input Port 0/serial I/O interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_0 (active high) which is a rising edge-triggered interrupt.
21-24	$P5_0$-$P5_3$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
28	V_{SS}	Ground.

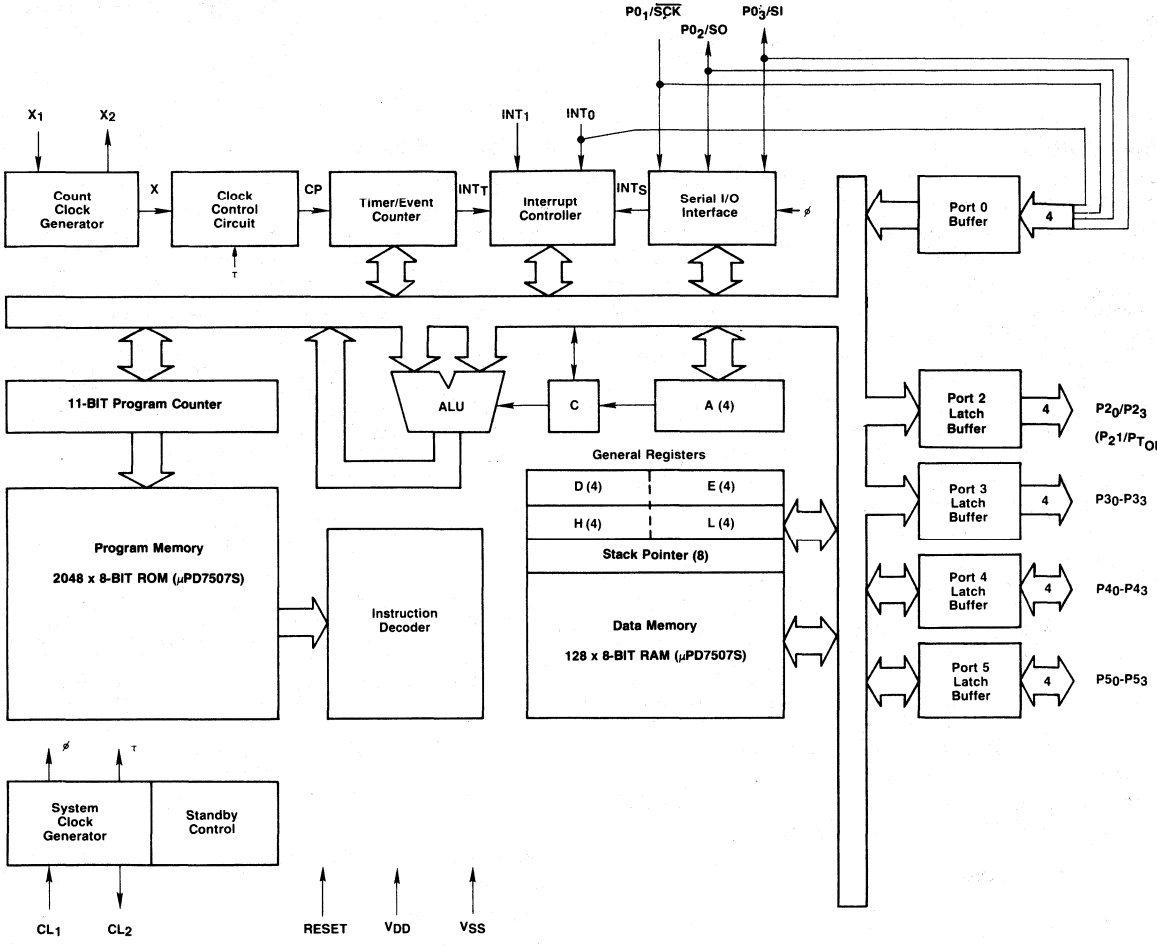
Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 30mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6

Block Diagram



DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi H}$	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	$V_{IH_{DR}}$	0.9 $V_{DD_{DR}}$		$V_{DD_{DR}}$ + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi L}$	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other than CL_1, X_1	$V_I = V_{DD}$
	$I_{L\phi_H}$			10		CL_1, X_1	
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	$I_{L\phi_L}$			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0 mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100 μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400 μA	
Output Leakage Current High	I_{LO_H}			3	μA	$V_O = V_{DD}$	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_O}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			150	400			V_{DD} = 3V ± 10%
	I_{DD_S}		2	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.5	10			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode	$V_{DD_{DR}}$ = 2.0V

AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
System Clock Oscillation Frequency	t_ϕ	120	200	280	KHz	CL_1, CL_2 R/C Clock: R = 82 kΩ ± 2%, C = 33 pF ± 5%	V_{DD} = 5V ± 10%
		60	100	130		R = 160 kΩ ± 2%, C = 33 pF ± 5%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
	$t_{\phi Ext}$	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	$t_{r\phi}$, $t_{f\phi}$			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	$t_{\phi W_H}$, $t_{\phi W_L}$	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_x	25	32	50	KHz	X_1, X_2 Crystal Oscillator	
	$f_{x_{Ext}}$	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{rx}, t_{fx}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{xW_H}, t_{xW_L}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Cycle Time	t_{CY_K}	4.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Pulse Width	t_{KW_H}, t_{KW_L}	1.8			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7V to 5.5V
		3.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
SI Setup Time to $\overline{SCK}$↑	t_{IS}	300			ns		
SI Hold Time after $\overline{SCK}$↑	t_{IH}	450			ns		
SO Delay Time after $\overline{SCK}$↓	t_{OD}			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	$t_{I_0W_H}$, $t_{I_0W_L}$	10			μs		
INT_1 Pulse Width	$t_{I_1W_H}$, $t_{I_1W_L}$	$2/f_\phi$			μs		
RESET Pulse Width	t_{RW_H}, t_{RW_L}	10			μs		
RESET Setup Time	t_{RS}	0			ns		
RESET Hold Time	t_{RH}	0			ns		

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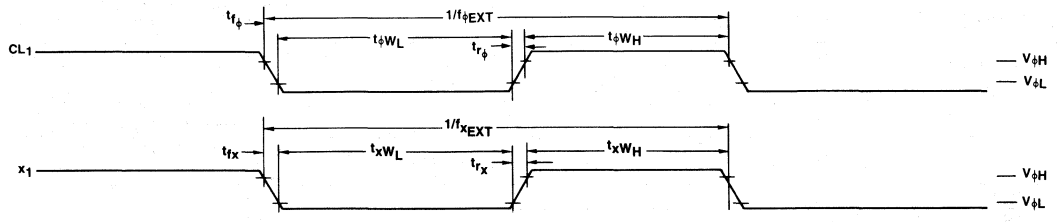
Capacitance

T_a = 25°C, V_{DD} = 0V

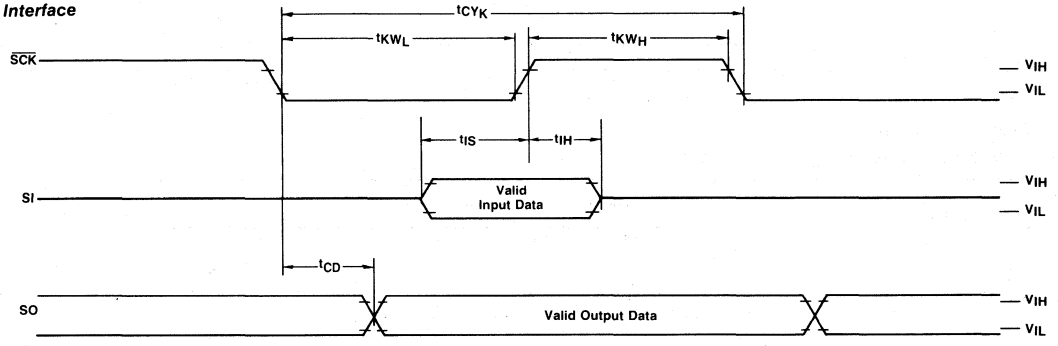
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			15		

Timing Waveforms

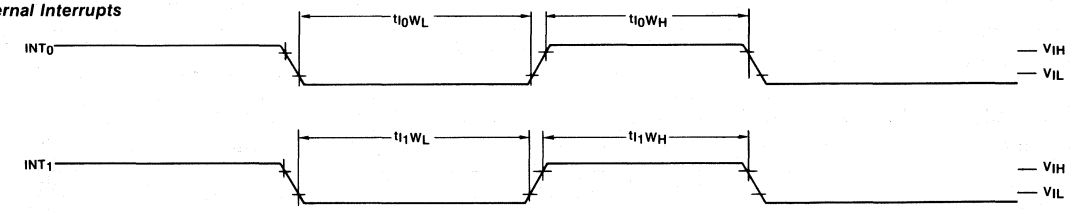
Clocks



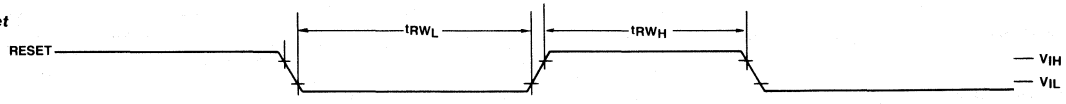
Serial Interface



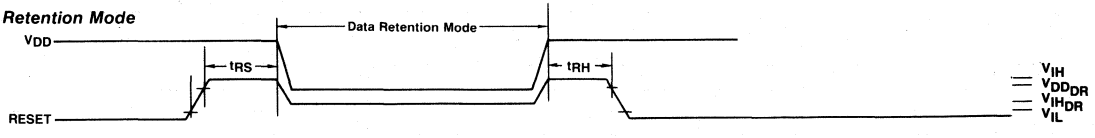
External Interrupts



Reset

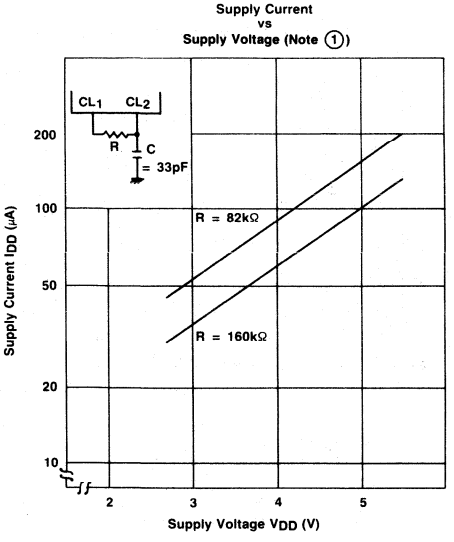


Data Retention Mode

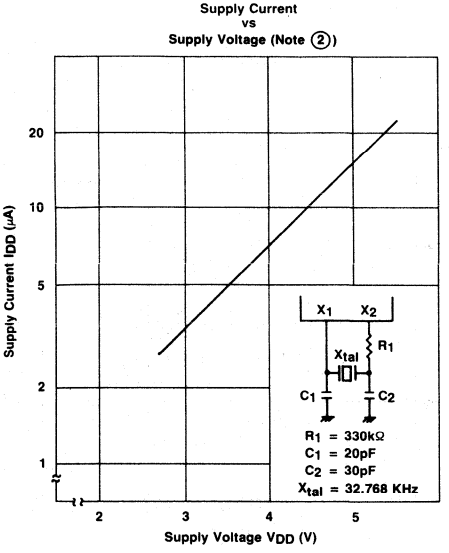


Operating Characteristics (Typical, T_a = 25°C)

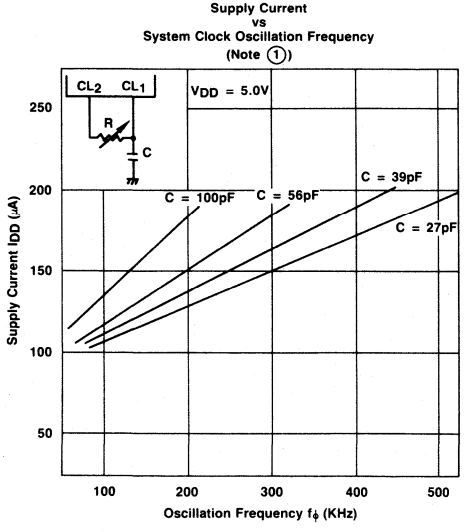
Supply Current vs Supply Voltage (Note ①)



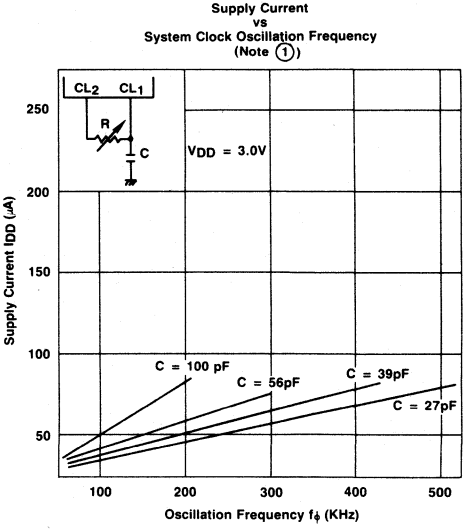
Supply Current vs Supply Voltage (Note ②)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Supply Current vs System Clock Oscillation Frequency (Note ①)

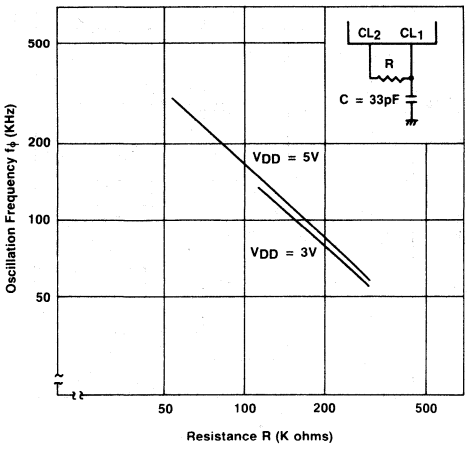


Notes:
① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.
② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

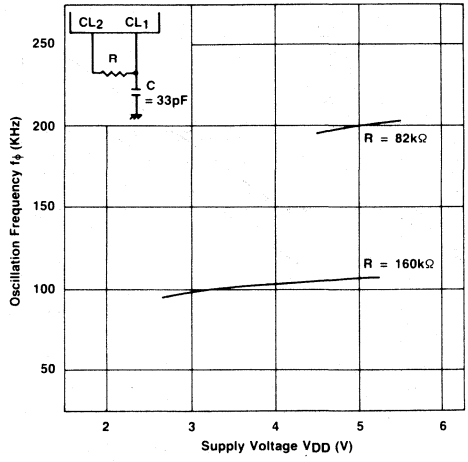
6

Operating Characteristics (Cont.)
(Typical, T_a = 25°C)

System Clock Oscillation Frequency
vs
Resistance



System Clock Oscillation Frequency
vs
Supply Voltage



μPD7508A
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

Description

The μPD7508A is a CMOS 4-bit single chip microcomputer which has the μPD750x architecture. It is identical to the μPD7508, except for a slightly smaller RAM, and 16 lines of vacuum fluorescent display drive capability.

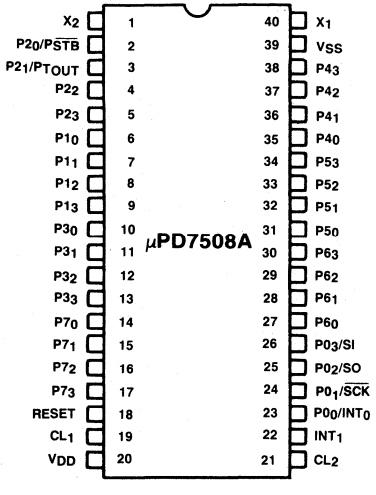
The μPD7508A contains a 4096 x 8-bit ROM, and a 208 x 4-bit RAM.

The μPD7508A contains four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7508A typically executes 92 instructions of the μPD7500 series "A" instruction set with a 10μs instruction cycle time.

The μPD7508A has two external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

The μPD7508A provides 32 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit output Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, 6, and 7. Ports 3, 4, 5, and 6 are capable of being pulled to −35V in order to drive vacuum fluorescent displays directly. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7508A is available in a 40-pin dual-in-line plastic package.

Pin Configuration



Pin Names

40-Pin DIP	Symbol	Function
1, 40	X_2, X_1	Crystal clock external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
2-5	$P2_0$-$P2_3$ $P2_0$/$\overline{STB}$ $P2_1$/PT_{OUT}	4-bit latched tristate output Port 2 (active high). Line $P2_0$ is also shared with $\overline{STB}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with PT_{OUT}, the timer out F/F signal (active high).
6-9	$P1_0$-$P1_3$	4-bit input/tristate output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0$/$\overline{STB}$ pulse.
10-13	$P3_0$-$P3_3$	4-bit input/latched tristate output Port 3 (active high).
14-17	$P7_0$-$P7_3$	4-bit input/latched tristate output Port 7 (active high).
18	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7507 or μPD7508 after power-up.
19, 21	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33 pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
20	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
22	INT_1	External Interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
23-26	$P0_0$/INT_0 $P0_1$/$\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input Port 0/serial I/O interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_0 (active high) which is a rising edge-triggered interrupt.
27-30	$P6_0$-$P6_3$	4-bit input/latched tristate output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
31-34	$P5_0$-$P5_3$	4-bit input/latched tristate output Port 5 (active high). Can also perform 8-bit parallel I/O conjunction with Port 4.
35-38	$P4_0$-$P4_3$	4-bit input/latched tristate output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
39	V_{SS}	Ground.

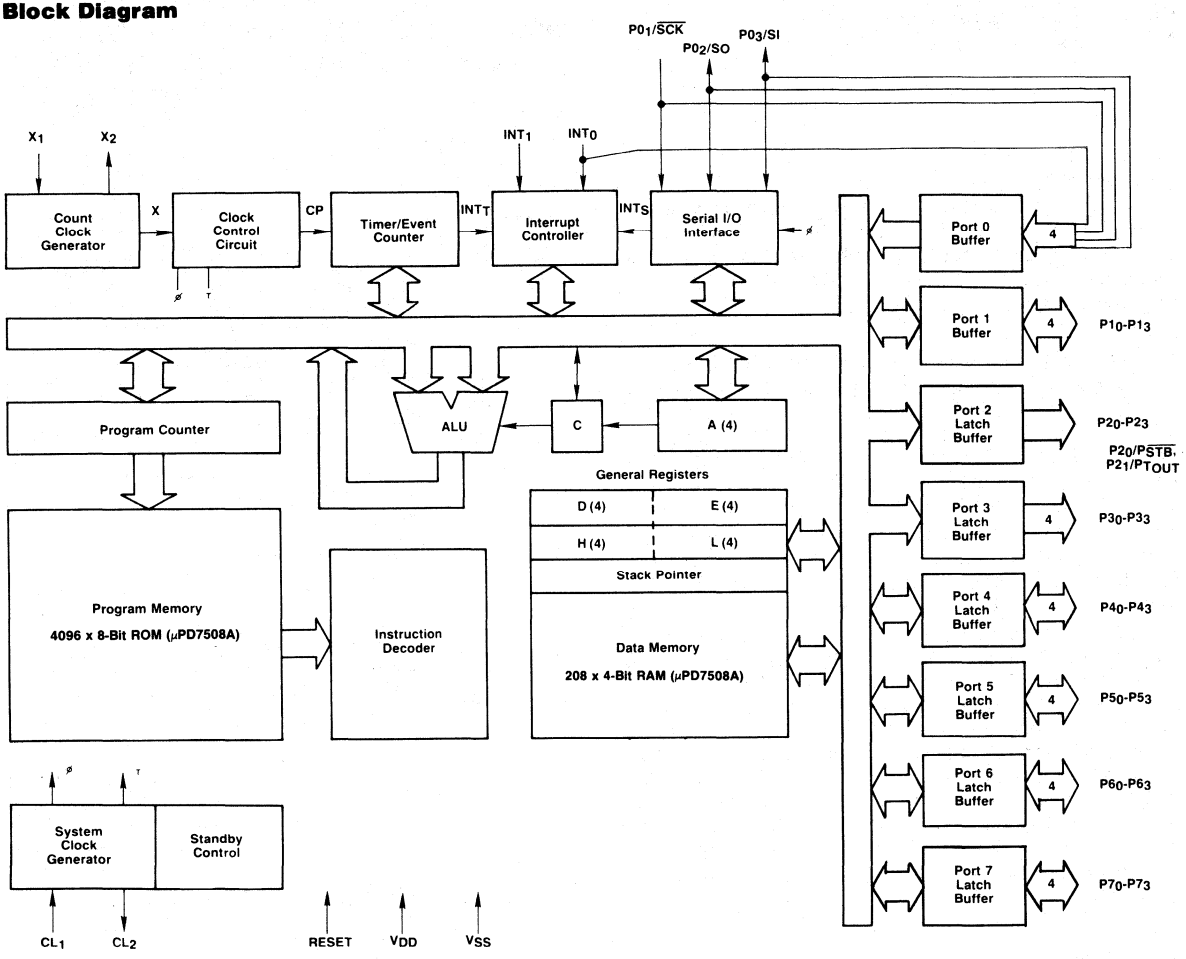
Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
Input Voltages, Ports 4, 5, and 6	(V_{DD} − 40.0)V to (V_{DD} + 0.3)V
All Other Input Ports	−0.3V to V_{DD} +0.3V
Output Voltages, Ports 3, 4, 5, and 6	(V_{DD} − 40.0)V to (V_{DD} + 0.3)V
All Other Output Ports	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −150mA
	I_{OL} = 50mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6

Block Diagram



DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	$V_{\phi H}$	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	$V_{IH_{DR}}$	0.9$V_{DD_{DR}}$		$V_{DD_{DR}}$ + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL_1}	0		0.3V_{DD}	V	All Inputs Other than CL_1, X_1, Ports 4, 5, and 6	
	V_{IL_2}	V_{DD} − 35.0		0.3V_{DD}		Ports 4, 5, and 6	
	$V_{\phi L}$	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LIH_1}			3	μA	All Inputs Other than CL_1, X_1, Ports 4, 5, and 6	V_I = V_{DD}
	I_{LIH_2}			60		Ports 4, 5, and 6,	V_I = V_{DD}
	$I_{L\phi H}$			10		CL_1, X_1	
Input Leakage Current Low	I_{LIL_1}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	I_{LIL_2}			−30		Ports 4, 5, and 6,	V_I = −30.0V
	$I_{L\phi L}$			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400μA	
Output Leakage Current High	I_{LOH_1}			3	μA	V_O = V_{DD}	
	I_{LOH_2}			30	μA	Ports 3, 4, 5, and 6,	V_O = −30V
Output Leakage Current Low	I_{LOL_2}			−3	μA	V_O = 0V	
	I_{LOL_2}			−30	μA	Ports 3, 4, 5, and 6,	V_O = −30V
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_O}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			150	400			V_{DD} = 3V ± 10%
	I_{DD_S}		2	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.5	10			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode, $V_{DD_{DR}}$ = 2.0V	

Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			20	pF	f = 1MHz,
Output Capacitance	C_O			20	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			20		

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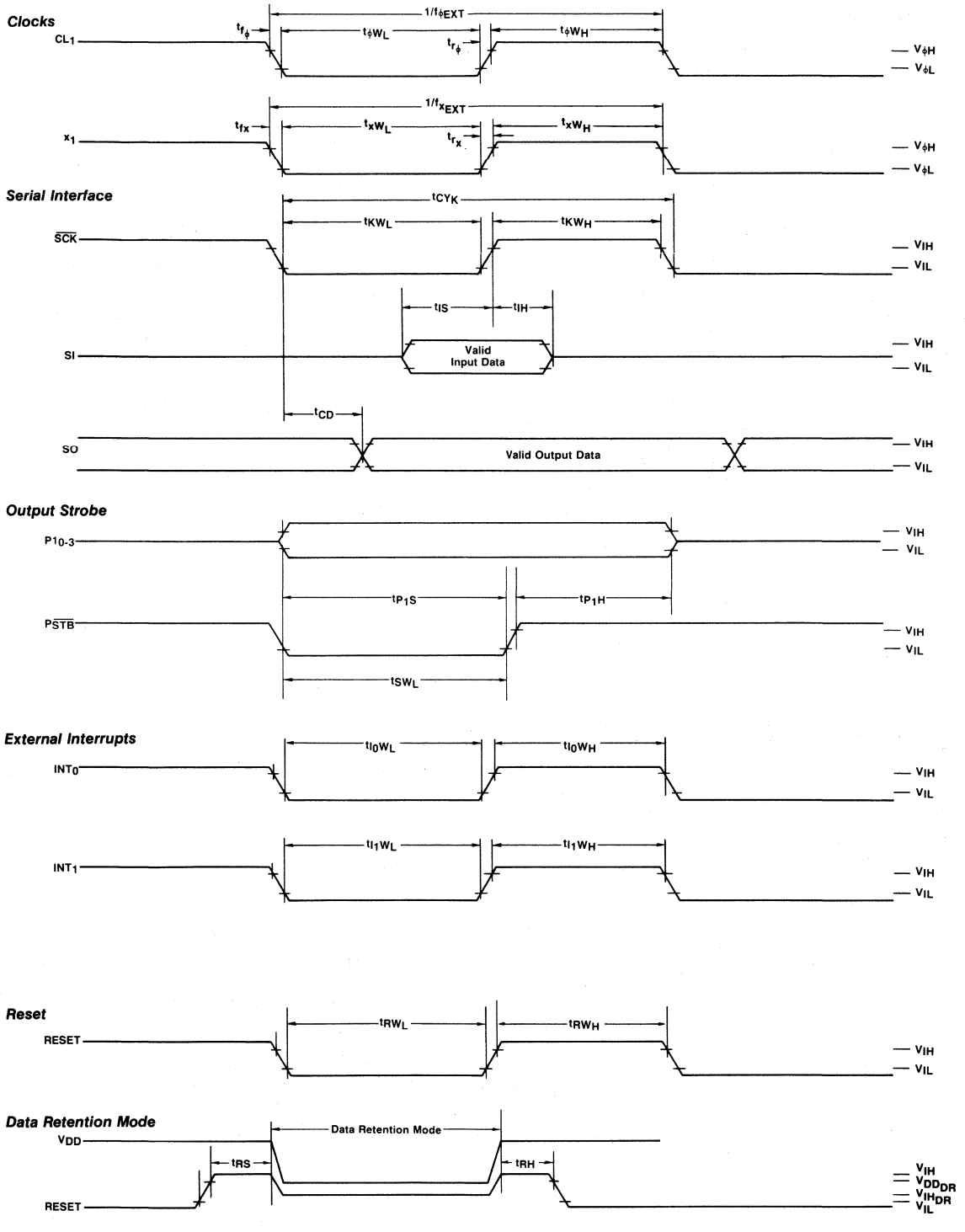
AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions		
System Clock Oscillation Frequency	f_ϕ	120	200	280	KHz	CL_1, CL_2 R/C Clock	R = 82kΩ ± 2%, C = 33pF ± 5%	V_{DD} = 5V ± 10%
		60	100	130			R = 160kΩ ±2%, C = 33pF ± 5%	V_{DD} = 3V ± 10%
		60		180				V_{DD} = 2.7V to 5.5V
	$f_{\phi Ext}$	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%	
		10		135			V_{DD} = 2.7V to 5.5V	
System Clock Rise and Fall Times	$t_{r\phi}$, $t_{f\phi}$			0.2	μs	CL_1, External Clock		
System Clock Pulse Width	$t_{\phi W_H}$, $t_{\phi W_L}$	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%	
		3.5		50			V_{DD} = 2.7V to 5.5V	
Counter Clock Oscillation Frequency	f_x	25	32	50	KHz	X_1, X_2 Crystal Oscillator		
	f_{xExt}	0		300		X_1, External Pulse Input		V_{DD} = 5V ± 10%
		0		135				V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{rx}, t_{fx}			0.2	μs	X_1, External Pulse Input		
Counter Clock Pulse Width	t_{xW_H}, t_{xW_L}	1.5			μs	X_1, External Pulse Input		V_{DD} = 5V ± 10%
		3.5						V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Cycle Time	t_{CY_K}	4.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%	
		7.0					V_{DD} = 2.7V to 5.5V	
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%	
		14.0					V_{DD} = 2.7V to 5.5V	
$\overline{SCK}$ Pulse Width	t_{KW_H}, t_{KW_L}	1.8			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%	
		3.3					V_{DD} = 2.7V to 5.5V	
		3.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%	
		6.5					V_{DD} = 2.7V to 5.5V	
SI Setup Time to $\overline{SCK}$↑	t_{IS}	300			ns			
SI Hold Time after $\overline{SCK}$↑	t_{IH}	450			ns			
SO Delay Time after $\overline{SCK}$↓	t_{OD}			850	ns	V_{DD} = 5V ±		
				1200		V_{DD} = 2.7V to 5.5V		
Port 1 Output Setup Time to P_{STB}↑	t_{P_1S}	$1/(2f_\phi - 800)$			ns	V_{DD} = 5V ± 10%		
		$1/(2f_\phi - 2000)$				V_{DD} = 2.7V to 5.5V		
Port 1 Output Hold Time after P_{STB}↑	t_{P_1H}	300	350	500	ns	V_{DD} = 5V ± 10%		
		300		1500		V_{DD} = 2.7V to 5.5V		
P_{STB} Pulse Width	t_{SW_L}	$1/(2f_\phi - 800)$			ns	V_{DD} = 5V ± 10%		
		$1/(2f_\phi - 2000)$				V_{DD} = 2.7V to 5.5V		
INT_0 Pulse Width	$t_{I_0W_H}$, $t_{I_0W_L}$	10			μs			
INT_1 Pulse Width	$t_{I_1W_H}$, $t_{I_1W_L}$	$2/f_\phi$			μs			
RESET Pulse Width	t_{RW_H}, t_{RW_L}	10			μs			
RESET Setup Time	t_{RS}	0			ns			
RESET Hold Time	t_{RH}	0			ns			

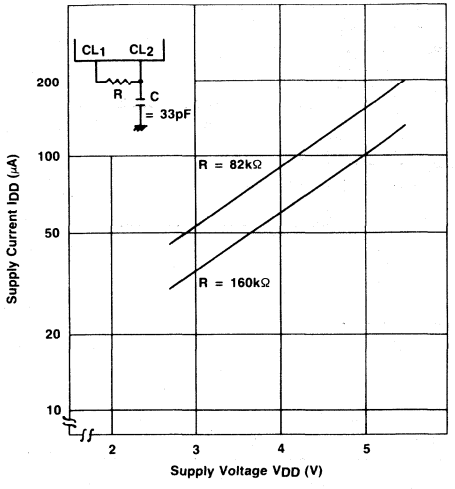
Timing Waveforms



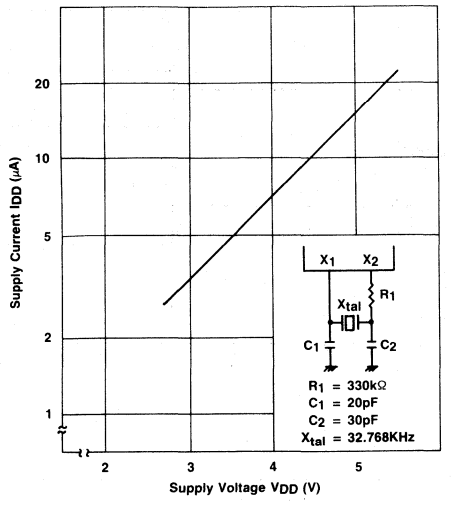
Operating Characteristics

Typical, T_a = 25°C

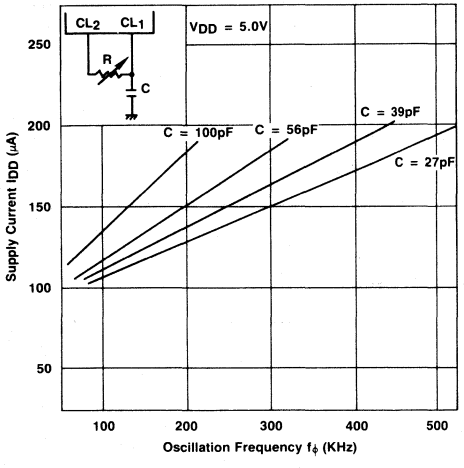
Supply Current vs Supply Voltage (Note ①)



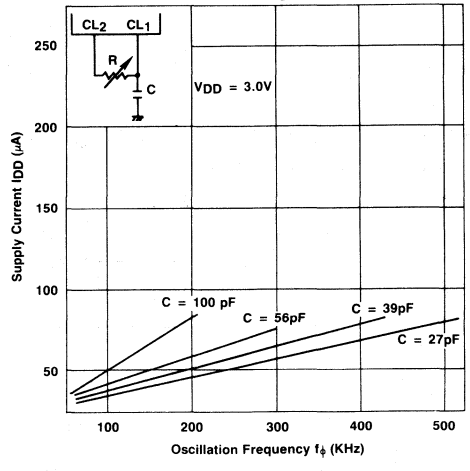
Supply Current vs Supply Voltage (Note ②)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Notes:

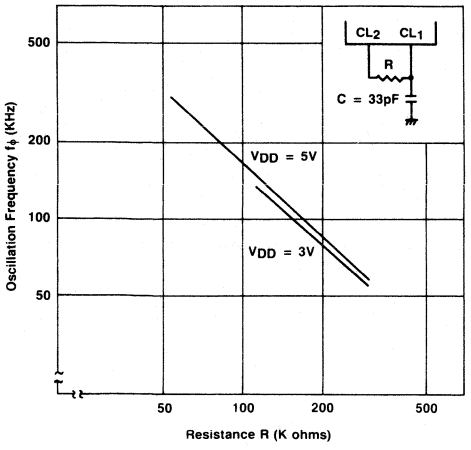
① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.

② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

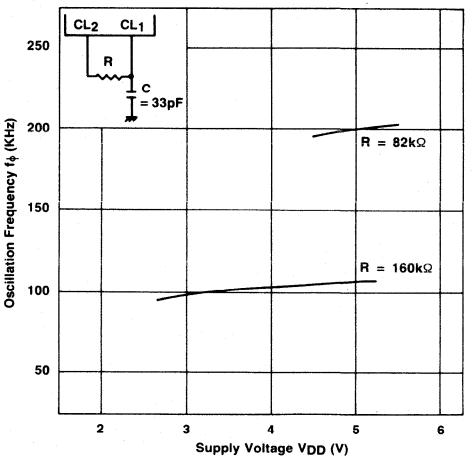
Operating Characteristics (Cont.)

Typical, T_a = 25°C

System Clock Oscillation Frequency
vs
Resistance



System Clock Oscillation Frequency
vs
Supply Voltage



6

PRELIMINARY

μPD7519
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER WITH VACUUM FLUORESCENT DISPLAY CONTROLLER/DRIVER

Description

The μPD7519 is a CMOS 4-bit single chip microcomputer which has the μPD750x architecture.

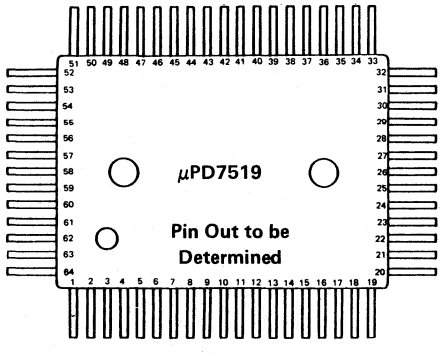
The μPD7519 contains a 4096 x 8-bit ROM, and a 256 x 4-bit RAM.

The μPD7519 contains four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7519 typically executes 92 instructions of the μPD7500 series "A" instruction set with a 10μs instruction cycle time.

The μPD7519 has two external and two internal edge-triggered hardware vectored interrupts. They also contain an 8-bit timer/event counter, an 8-bit serial interface, and a 9-bit D/A programmable pulse generator, to help reduce software requirements. The on-board vacuum fluorescent display controller/driver supervises all of the timing required by the 24 Port S segment drivers either for a 16-digit 7-segment vacuum fluorescent display, or for an 8-character 14-segment vacuum fluorescent display.

The μPD7519 provides 28 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit output Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, and 6. Additionally, Port 1 can be automatically expanded to 16 I/O lines through connection to a μPD82C43. The μPD7519 is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7519 is available in a space-saving 64-pin flat plastic package.

Pin Configuration

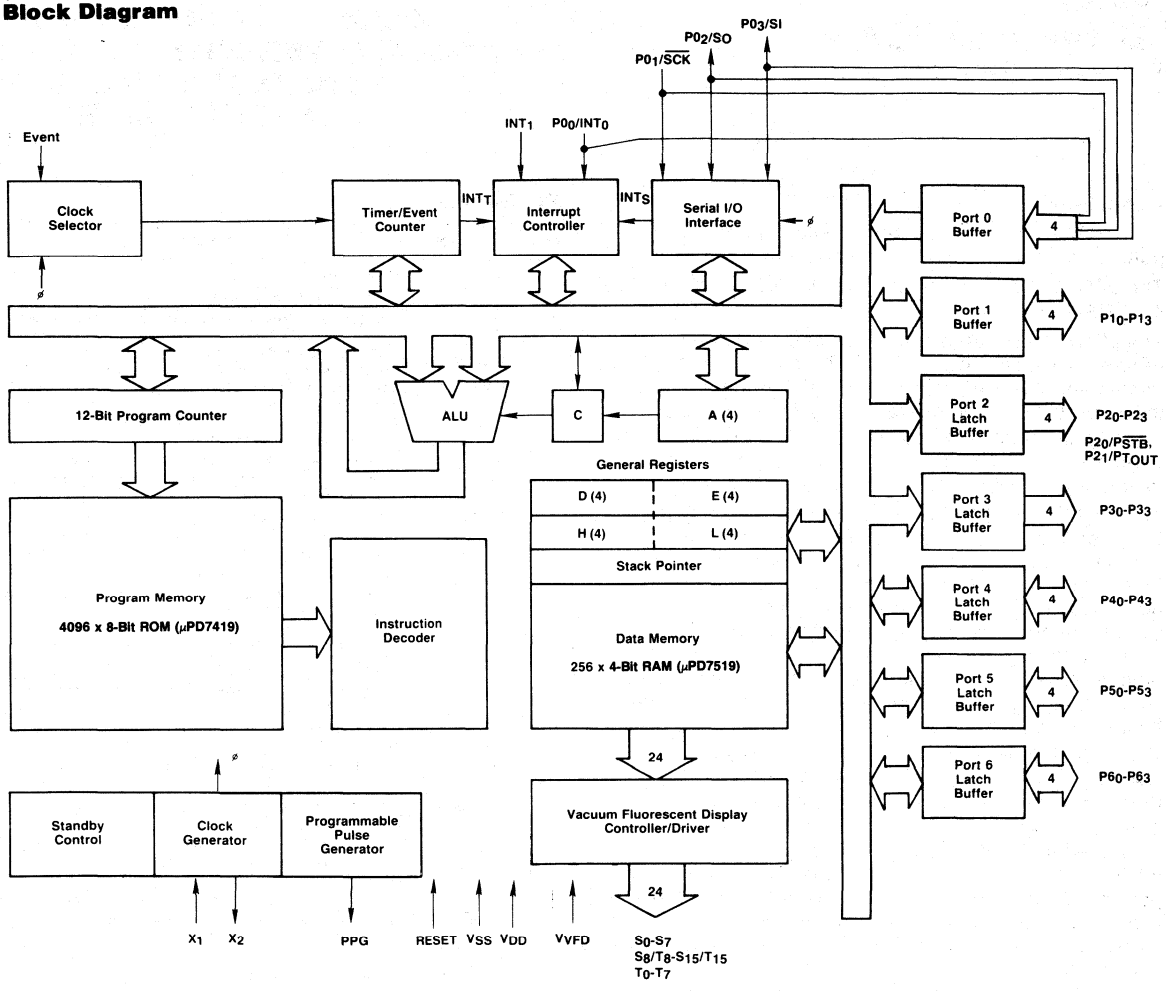


Pin Names

PIN #	SYMBOL	FUNCTION
	NC	No Connection.
	$P3_3$-$P3_0$	4-bit latched tristate output Port 3 (active high).
	$P0_3$/SI $P0_2$/SO $P0_1$/$\overline{SCK}$ $P0_0$/INT_0	4-bit input Port 0/serial I/O interface (active high). This port can be configured either as a parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active high), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_0, which is a rising edge-triggered interrupt.
	$P6_3$-$P6_0$	4-bit input/latched tristate output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
	$P5_3$-$P5_0$	4-bit input/latched tristate output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
	$P4_3$-$P4_0$	4-bit input/latched tristate output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
	X_2, X_1	Crystal clock input (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for system clock operation. Alternatively, an external clock source may be connected to input X_1 while output X_2 is left open.
	V_{SS}	Ground.
	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
	INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7502 or μPD7503 after power-up.
	$P1_3$-$P1_0$	4-bit input/latched tristate output Port 1 (active high).
	$P2_3$-$P2_0$ $P2_0$/$P_{\overline{STB}}$ $P2_1$/P_{TOUT}	4-bit latched output Port 2 (active high). Line $P2_0$ is also shared with $P_{\overline{STB}}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with P_{TOUT}, the timer-out F/F signal (active high).
	PPG	1-bit programmable pulse generator output (active high).
	Event	1-bit external event input for timer/event counter (active high).
	V_{VFD}	Vacuum fluorescent display power supply negative. Apply single voltage between V_{DD} – 35.0 and V_{DD} for proper display operation.
	S_0-S_7 S_8/T_8-S_{15}/T_{15} T_0-T_7	Vacuum fluorescent display outputs (active high). S_0-S_7 are always segment driver outputs, and T_0-T_7 are always digit driver outputs. S_8/T_8-S_{15}/T_{15} can be configured as either segment driver outputs or as digit driver outputs under control of the display mode select register.

6

Block Diagram

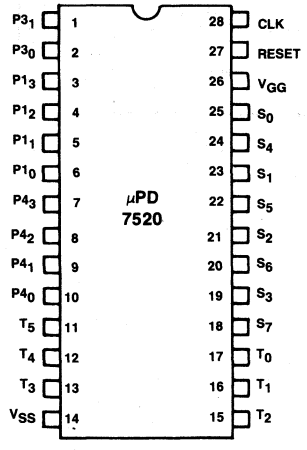


μPD7520
4-BIT SINGLE CHIP MICROCOMPUTER WITH LED DISPLAY CONTROLLER/DRIVER

Description

The μPD7520 is a low-cost 4-bit single chip microcomputer which shares the 4th generation architecture of the μPD7500 series of CMOS 4-bit microcomputers. It contains a 768 x 8-bit ROM and a 48 x 4-bit RAM. It has a 2-level subroutine stack, and executes a 47-instruction subset of the μPD7500 series instruction set. The μPD7520 provides 24 I/O lines, organized into the 4-bit input Port 1, the 4-bit I/O Port 4, the 2-bit output Port 3, the 8-bit output Port S, and the 6-bit output Port T. Ports S and T are controlled by the on-board programmable LED display controller/driver hardware logic block, which automatically directly drives either static or multiplexed common-anode 7-segment LED displays totally transparent to program execution. The μPD7520 is manufactured with a low-power consumption PMOS process, allowing use of a single power supply between −6V and −10V, and is available in a 28-pin dual-in-line plastic package.

Pin Configuration



Pin Names

S_0–S_7	Segment Drive Output Port S
T_0–T_5	Digit Drive Output Port T
$P1_0$–$P1_3$	Input Port 1
$P3_0$–$P3_1$	Output Port 3
$P4_0$–$P4_3$	Input/Output Port 4
CLK	Clock Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Ground

Further details on device operation can be found in the μPD7520 4-Bit Single Chip Microcomputer Technical Manual.

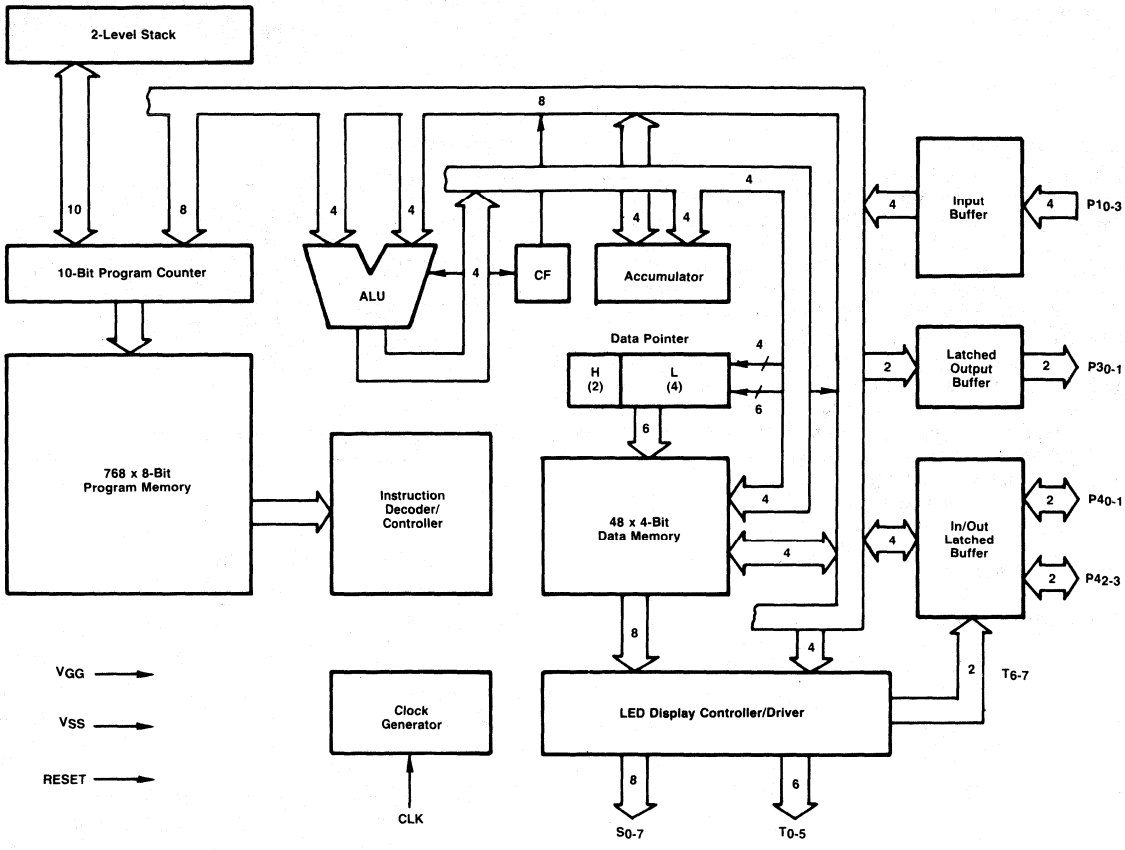
Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage, V_{GG}	−15V to +0.3V
Input Voltages	−15V to +0.3V
Output Voltages	−15V to +0.3V
Output Current (I_{OH} Total)	−100mA
(I_{OL} Total)	90mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6

Block Diagram



DC Characteristics

T_a = −10°C to +70°C, V_{GG} = −6V to −10V, V_{SS} = 0V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input Voltage High	V_{IH}			−2.0	V	Ports 1, 4, RESET; V_{GG} = −9V ± 1V
				−1.8		V_{GG} = −6V to −10V
Input Voltage Low	V_{IL}	V_{GG} + 1.5			V	Ports 1, 4, RESET; V_{GG} = −9V ± 1V
		V_{GG} + 0.8				V_{GG} = −6V to −10V
Clock Voltage High	$V_{\phi H}$			−0.8	V	CLK, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0			V	CLK, External Clock
Input Current High	I_{IH}	45		200	μA	Port 1, RESET; V_I = 0V, V_{GG} = −9V ± 1V
		40		200		V_I = 0V, V_{GG} = −6V to −10V
Input Leakage Current High	I_{LIH}			+5	μA	Port 4, V_I = 0V
Input Leakage Current Low	I_{LIL_1}			−5	μA	Port 1, RESET, V_I = −10V, V_{GG} = −10V
	I_{LIL_2}			−5	μA	Port 4, V_I = −10V
Clock Current High	$I_{\phi H}$			0.5	mA	CLK, External Clock, $V_{\phi H}$ = 0V, V_{GG} = −9V ± 1V
Clock Current Low	$I_{\phi L}$			−2.1	mA	CLK, External Clock, $V_{\phi L}$ = −5V, V_{GG} = −9V ± 1V
Output Voltage Low	V_{OL}	V_{GG} + 0.6			V	Port 3, No Load
Output Current High	I_{OH_1}	−1.0			mA	Port 3, V_O = −1.0V, V_{GG} = −9V ± 1V
		−0.6				Port 3, V_O = −1.0V, V_{GG} = −6V
	I_{OH_2}	−2.0			mA	Port 4, V_O = −1.0V, V_{GG} = −9V ± 1V
		−1.2				Port 4, V_O = −1.0V, V_{GG} = −6V
	I_{OH_3}	−5	−10		mA	Port S, V_O = −2.0V, V_{GG} = −9V ± 1V
		−3	−6			Port S, V_O = −2.0V, V_{GG} = −6V
		−1	−3			Port S, V_O = −1.0V, V_{GG} = −6V to −10V
	I_{OH_4}	−24	−48		mA	Port T, V_O = −2.0V, V_{GG} = −9V ± 1V
		−13	−27			Port T, V_O = −1.0V, V_{GG} = −9V ± 1V
		−9	−18			Port T, V_O = −1.0V, V_{GG} = −6V
Output Current Low	I_{OL_1}	1.0	2.0		mA	Port 3, V_O = V_{GG} + 1.5V, V_{GG} = −9V ± 1V ①
		0.3	0.6			Port 3, V_O = −4.5V, V_{GG} = −6V ①
	I_{OL_2}	4.5	9		mA	Port S, V_O = V_{GG} + 5.0V, V_{GG} = −9V ±1V
		1.0	2.0			Port S, V_O = V_{GG} + 3.5V, V_{GG} = −6V to −10V
Output Leakage Current High	I_{LOH}			+5	μA	Ports 4, T, V_O = 0V
Output Leakage Current Low	I_{LOL_1}			−5.0	μA	Port T, V_O = −10V
	I_{LOL_2}			−5.0		Port 3, V_O = V_{GG}
Supply Current	I_{GG}		−5②	−9.6	mA	No Load

Notes:

① Current within 2.5 ms after turning to the low level (T_a = 25°C).

② T_a = 25°C, V_{GG} = −9V.

AC Characteristics

T_a = −10°C to +70°C, V_{GG} = −6V to −10V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Clock Frequency	f_{osc}	225	300	375	KHz	R_f = 1MΩ, V_{GG} = −9V ± 1V, T_a = 25°C
		180	300	450	KHz	R_f = 1MΩ, V_{GG} = −9V ± 1V
	f_ϕ	100		330	KHz	
Clock Rise and Fall Times	t_r, t_f			2	μs	CLK, External Clock
Clock Pulse Width High	$t_{\phi W_H}$	1.5		3	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	1.5		3	μs	

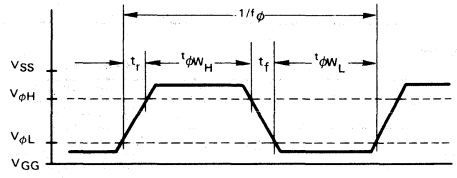
Capacitance

T_a = 25°C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	Port 1, RESET
Output Capacitance	C_O			20	pF	Ports 3, S,T
Input/Output Capacitance	C_{IO}			20	pF	Port 4
Clock Capacitance	C_ϕ			30	pF	CLK

f = 1MHz

Clock Waveform



Development Tools

The NEC Electronics U.S.A.'s NDS Development System is available for the development of software source code, editing, and assembly into object code. In addition, the ASM75 Cross Assembler is available for systems supporting the ISIS-II or the CP/M (® Digital Research Corp.) Operating Systems.

The EVAKIT-7520 Evaluation Board is available for production device evaluation and prototype system debugging.

The ASM75-F9T Cross Assembler is available for systems supporting fortran IV ANSI Standard 1966-V3.9.

Instruction Set Symbol Definitions

The following abbreviations are used in the description of the μPD7520 instruction set:

SYMBOL	EXPLANATION AND USE
A	Accumulator
address	Immediate address
C	Carry Flag
data	Immediate data
D_n	Bit "n" of immediate data or immediate address
H	Register H
HL	Register pair HL
L	Register L
P( )	Parallel Input/Output Port addressed by the value within the brackets
PC_n	Bit "n" of Program Counter
S	Zero when Skip Condition does not occur; the number of bytes in next instruction when Skip Condition occurs
Stack	Stack Register
String	String Effect Skip Condition, whereby succeeding instructions of the same type are executed as NOP instructions
( )	The contents of RAM addressed by the value within the brackets
[ ]	The contents of ROM addressed by the value within the brackets
←	Load, Store, or Transfer
↔	Exchange
—	Complement
⊻	LOGICAL Exclusive-OR

Instruction Set

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
			LOAD										
LAI data	$A \leftarrow D_{3-0}$	Load A with 4 bits of immediate data; execute succeeding LAI instructions as NOP instructions	0	0	0	1	D_3	D_2	D_1	D_0	1	1	String
LHI data	$H \leftarrow D_{1-0}$	Load H with 2 bits of immediate data	0	0	1	0	1	0	D_1	D_0	1	1	
LHLI data	$HL \leftarrow D_{4-0}$	Load HL with 5 bits of immediate data; execute succeeding LHLI instructions as NOP instructions	1	1	0	D_4	D_3	D_2	D_1	D_0	1	1	String
LAMT	$A \leftarrow [PC_{9-6}, 0, C, A]_H$	Load the upper 4 bits of ROM Table Data at address PC_{9-6}, 0, C, A to A	0	1	0	1	1	1	1	0	1	2	
	$(HL) \leftarrow [PC_{9-6}, 0, C, A]_L$	Load the lower 4 bits of ROM Table Data at address PC_{9-6}, 0, C, A to the RAM location addressed by HL											
L	$A \leftarrow (HL)$	Load A with the contents of RAM addressed by HL	0	1	0	1	0	0	1	0	1	1	
LIS	$A \leftarrow (HL)$ $L = L + 1$ Skip if L = 0H	Load A with the contents of RAM addressed by HL; increment L; skip if L = 0H	0	1	0	1	0	0	0	1	1	1 + S	L = 0H
LDS	$A \leftarrow (HL)$ $L = L - 1$ Skip if L = FH	Load A with the contents of RAM addressed by HL; decrement L; skip if L = FH	0	1	0	1	0	0	0	0	1	1 + S	L = FH
LADR address	$A \leftarrow (D_{5-0})$	Load A with the contents of RAM addressed by 6 bits of immediate data	0 0	0 0	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	0 D_0	2	2	

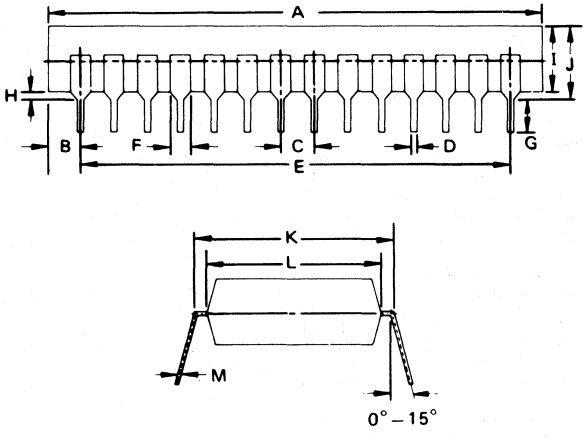
Instruction Set (Cont.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
		STORE											
ST	(HL) ← A	Store A into the RAM location addressed by HL	0	1	0	1	0	1	1	1	1	1	
STII data	(HL) ← D_{3-0} L ← L + 1	Store 4 bits of immediate data into the RAM location addressed by HL; increment L	0	1	0	0	D_3	D_2	D_1	D_0	1	1	
		EXCHANGE											
XAH	A_{1-0} ↔ H_{1-0} A_{3-2} ← 00H	Exchange A with H	0	1	1	1	1	0	1	0	1	1	
XAL	A ↔ L	Exchange A with L	0	1	1	1	1	0	1	1	1	1	
X	A ↔ (HL)	Exchange A with the contents of RAM addressed by HL	0	1	0	1	0	1	1	0	1	1	
XIS	A ↔ (HL) L ← L + 1 Skip if L = 0H	Exchange A with the contents of RAM addressed by HL; increment L; skip if L = 0H	0	1	0	1	0	1	0	1	1	1 + S	L = 0H
XDS	A ↔ (HL) L ← L − 1 Skip if L = FH	Exchange A with the contents of RAM addressed by HL; decrement L; skip if L = FH	0	1	0	1	0	1	0	0	1	1 + S	L = FH
XADR address	A ↔ (D_{5-0})	Exchange A with the contents of RAM addressed by 6 bits of immediate data	0 0	0 0	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	1 D_0	2	2	
		ARITHMETIC AND LOGICAL											
AISC data	A ← A + D_{3-0} Skip if overflow	Add 4 bits of immediate data to A; Skip if overflow is generated	0	0	0	0	D_3	D_2	D_1	D_0	1	1 + S	Overflow
ASC	A ← A + (HL) Skip if overflow	Add the contents of RAM addressed by HL to A; skip if overflow is generated	0	1	1	1	1	1	0	1	1	1 + S	Overflow
ACSC	A, C ← A + (HL) + C Skip if C = 1	Add the contents of RAM addressed by HL and the carry flag to A; skip if carry is generated	0	1	1	1	1	1	0	0	1	1 + S	C = 1
EXL	A ← A ⊻ (HL)	Perform a LOGICAL Exclusive—OR operation between the contents of RAM addressed by HL and A; store the result in A	0	1	1	1	1	1	1	0	1	1	
		ACCUMULATOR AND CARRY FLAG											
CMA	A ← $\overline{A}$	Complement A	0	1	1	1	1	1	1	1	1	1	
RC	C ← 0	Reset Carry Flag	0	1	1	1	1	0	0	0	1	1	
SC	C ← 1	Set Carry Flag	0	1	1	1	1	0	0	1	1	1	
		INCREMENT AND DECREMENT											
ILS	L ← L + 1 Skip if L = 0H	Increment L; Skip if L = 0H	0	1	0	1	1	0	0	1	1	1 + S	L = 0H
IDRS address	(D_{5-0}) ← (D_{5-0}) + 1 Skip if (D_{5-0}) = 0H	Increment the contents of RAM addressed by 6 bits of immediate data; Skip if the contents = 0H	0 0	0 0	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0	2	2 + S	(D_{5-0}) = 0H
DLS	L ← L − 1 Skip if L = FH	Decrement L; Skip if L = FH	0	1	0	1	1	0	0	0	1	1 + S	L = FH
DDRS address	(D_{5-0}) ← (D_{5-0}) − 1 Skip if (D_{5-0}) = FH	Decrement the contents of RAM addressed by 6 bits of immediate data, skip if the contents = FH	0 0	0 0	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	0 D_0	2	2 + S	(D_{5-0}) = FH
		BIT MANIPULATION											
RMB data	$(HL)_{bit}$ ← 0	Reset a single bit (denoted by D_1D_0) of the RAM location addressed by HL to zero	0	1	1	0	1	0	D_1	D_0	1	1	
SMB data	$(HL)_{bit}$ ← 1	Set a single bit (denoted by D_1D_0) of the RAM location addressed by HL to one	0	1	1	0	1	1	D_1	D_0	1	1	
		JUMP, CALL, AND RETURN											
JMP address	PC_{9-0} ← D_{9-0}	Jump to the address specified by 10 bits of immediate data	0 D_7	0 D_6	1 D_5	0 D_4	0 D_3	0 D_2	D_9 D_1	D_8 D_0	2	2	
JAM data	PC_{9-8} ← D_{1-0} PC_{7-4} ← A PC_{3-0} ← (HL)	Jump to the address specified by 2 bits of immediate data, A, and the RAM contents addressed by HL	0 0	0 0	1 0	1 1	1 0	1 0	1 D_1	1 D_0	2	2	

Instruction Set (Cont.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
		JUMP, CALL, AND RETURN											
JCP address	$PC_{5-0} \leftarrow D_{5-0}$	Jump to the address specified by the higher-order bits PC_{9-6} of the PC, and 6 bits of immediate data	1	0	D_5	D_4	D_3	D_2	D_1	D_0	1	1	
CALL address	STACK ← PC + 2 $PC_{9-0} \leftarrow D_{9-0}$	Store a return address (PC + 2) in the stack; call the subroutine program at the location specified by 10 bits of immediate data	0 D_7	0 D_6	1 D_5	1 D_4	0 D_3	0 D_2	D_9 D_1	D_8 D_0	2	2	
CAL address	STACK ← PC + 1 $PC_{9-0} \leftarrow 01D_4D_3$ $000D_2D_1D_0$	Store a return address (PC + 1) in the stack; call the subroutine program at one of the 32 special locations specified by 5 bits of immediate data	1	1	1	D_4	D_3	D_2	D_1	D_0	1	1	
RT	PC ← STACK	Return from Subroutine	0	1	0	1	0	0	1	1	1	1	
RTS	PC ← STACK Skip unconditionally	Return from Subroutine; skip unconditionally	0	1	0	1	1	0	1	1	1	1 + S	Unconditional
		SKIP											
SKC	Skip if C = 1	Skip if carry flag is true	0	1	0	1	1	0	1	0	1	1 + S	C = 1
SKMBT data	Skip if $(HL)_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by HL is true	0	1	1	0	0	1	D_1	D_0	1	1 + S	$(HL)_{bit} = 1$
SKMBF data	Skip if $(HL)_{bit} = 0$	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by HL is false	0	1	1	0	0	0	D_1	D_0	1	1 + S	$(HL)_{bit} = 0$
SKABT data	Skip if $A_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of A is true	0	1	1	1	0	1	D_1	D_0	1	1 + S	$A_{bit} = 1$
SKAEI data	Skip if A = data	Skip if A equals 4 bits of immediata data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	2	2 + S	A = data
SKAEM	Skip if A = (HL)	Skip if A equals the RAM contents addressed by HL	0	1	0	1	1	1	1	1	1	1 + S	A = (HL)
		PARALLEL I/O											
IPL	A ← P(L)	Input the Port addressed by L to A	0	1	1	1	0	0	0	0	1	1	
IP1	A ← P1	Input Port 1 to A	0	1	1	1	0	0	0	1	1	1	
OPL	P(L) ← A	Output A to the port addressed by L	0	1	1	1	0	0	1	0	1	1	
OP3	$P3 \leftarrow A_{1-0}$	Output the lower 2 bits of A to Port 3	0	1	1	1	0	0	1	1	1	1	
		CPU CONTROL											
NOP		Perform no operation; consume one machine cycle	0	0	0	0	0	0	0	0	1	1	

Package Outline μPD7520C



Item	Plastic Millimeters	Inches
A	38.0 MAX	1.496 MAX
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

μPD7500
CMOS 4-BIT MICROPROCESSOR
μPD7500 SERIES ROM-LESS EVALUATION CHIP

Description

The μPD7500 is a CMOS 4-bit microprocessor which has the μPD750x architecture, and also functions as the μPD7500 series ROM-less evaluation chip.

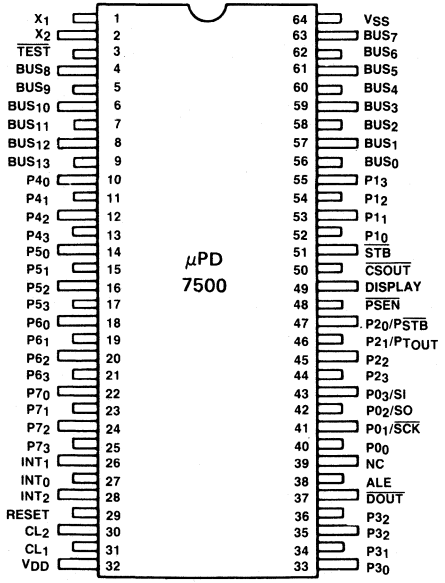
The μPD7500 contains a 256 x 4-bit RAM, and is capable of addressing up to 8192 x 8-bits of external program memory.

The μPD7500 contains four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7500 typically executes either all 110 instructions of the μPD7500 series "A" instruction set, or all 70 instructions of the μPD7500 series "B" instruction set with a 10μs instruction cycle time.

The μPD7500 has three external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements. A display timing pulse is also provided when emulating the μPD7501, μPD7502, the μPD7503, or the μPD7519.

The μPD7500 provides 32 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit output Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, 6, and 7. It is manufactured with a low power consumption CMOS process, allowing the use of a single +5V power supply. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7500 is available in a 64-pin quad-in-line plastic package.

Pin Configuration



Pin Names

Pin No.	Pin Symbol	Function
1, 2	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
3	$\overline{TEST}$	Factory test pin (connect to V_{SS}).
4-9, and 56-63	BUS_0-BUS_{13}	External data bus (active high). Connected to external program memory.
10-13	$P4_0$-$P4_3$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
14-17	$P5_0$-$P5_3$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
18-21	$P6_0$-$P6_3$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
22-25	$P7_0$-$P7_3$	4-bit input/latched tri-state output Port 7 (active high).
26	INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
27	INT_0	External interrupt INT_0 (active high). This is a rising edge-triggered interrupt.
28	INT_2	External interrupt INT_2 (active high). This is a rising edge-triggered interrupt.
29	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7500 after power-up.
30, 31	CL_1, CL_2	System clock input (active high). Connect 82KΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
32	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
33-36	$P3_0$-$P3_3$	4-bit input/latched tri-state output Port 3 (active high).
37	$\overline{DOUT}$	Data output (active low).
38	ALE	Address latch enable (active high).
39	NC	No connection.
40-43	$P0_0$ $P0_1/\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input Port 0/serial I/O interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface.
44-47	$P2_0$-$P2_3$ $P2_0/P\overline{STB}$ $P2_1/PT_{OUT}$	4-bit latched tri-state output Port 2 (active high). Line $P2_0$ is also shared with $P\overline{STB}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with PT_{OUT}, the timer-out F/F signal (active high).
48	$\overline{PSEN}$	Program store enable (active low).
49	DISPLAY	DISPLAY timing pulse (active high).
50	$\overline{CSOUT}$	Chip select output (active low). Connected to μPD82C43.
51	$\overline{STB}$	STROBE output (active low). Connected to μPD82C43.
52-55	$P1_0$-$P1_3$	4-bit input/tri-state output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0/P\overline{STB}$ pulse.
64	V_{SS}	Ground.

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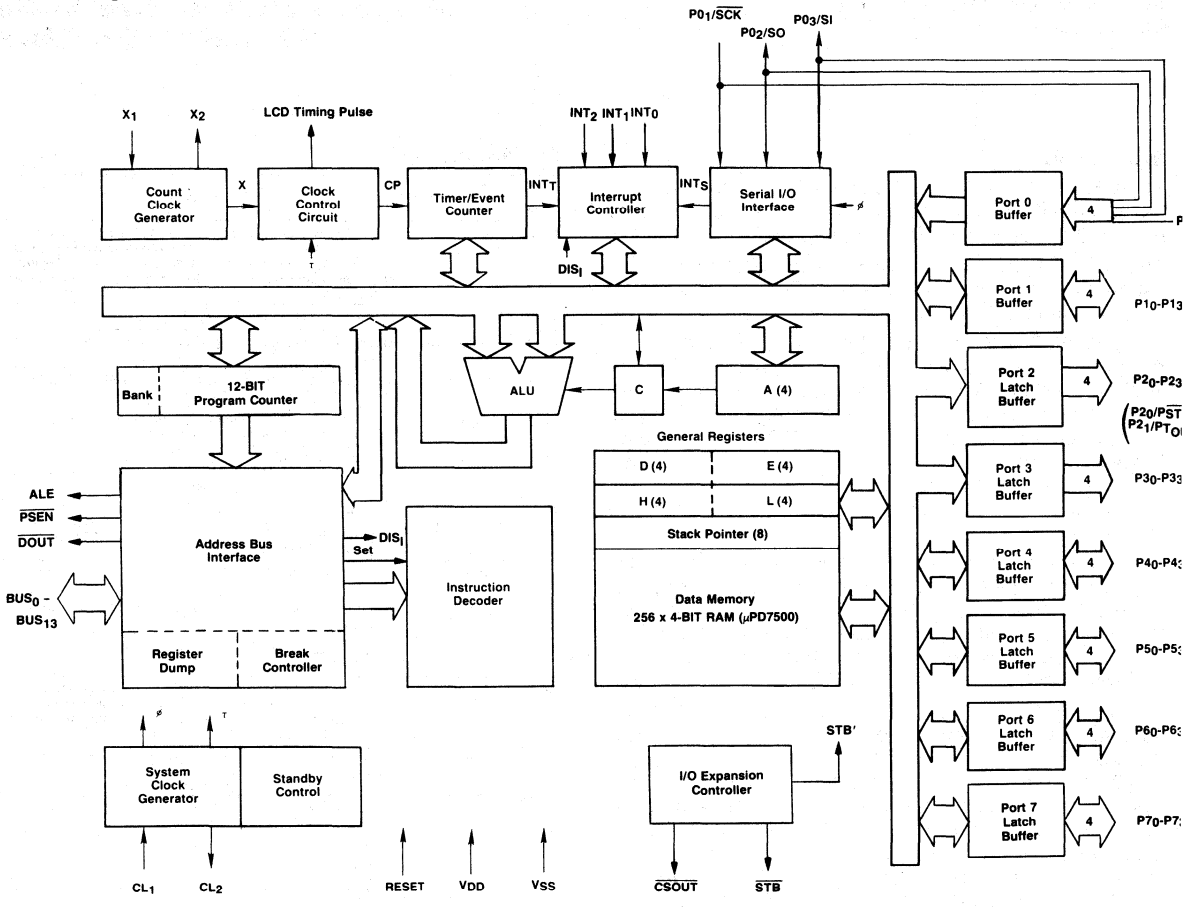
Block Diagram



Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 30mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1
	$V_{\phi H}$	V_{DD} −0.5		V_{DD}		CL_1, X_1
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1
	$V_{\phi L}$	0		0.5		CL_1, X_1
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other V_I = V_{DD} than CL_1, X_1
	$I_{L\phi_H}$			10		CL_1, X_1
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other V_I = 0V than CL_1, X_1
	$I_{L\phi_L}$			−10		CL_1, X_1
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	
Output Voltage Low	V_{OL}			0.4	V	
Output Leakage Current High	I_{LO_H}			3	μA	V_O = V_{DD}
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V
Supply Current	I_{DD_O}			2000	μA	Normal Operation All Output Pins Open No BUS Conflicts
	I_{DD_S}		2	20	μA	Stop Mode, X_1 = 0V
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode $V_{DD_{DR}}$ = 2.0V

Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			15	pF	f = 1MHz
Output Capacitance	C_{OUT}			15	pF	Unmeasured pins returned to V_{SS}
I/O Capacitance	C_{IO}			15	pF	

AC Characteristics

T_a = −10° ∼ +70°C, V_{DD} = 5V ± 10%

Clock Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System Clock Oscillation Frequency	f_ϕ	120	200	280	KHz	R = 82kΩ ± 2% C = 33pF ± 5%
	f_ϕ	10		300	KHz	CL_1, External Clock
CL_1 Input Rise Time	t_{CR}			0.2	μs	
CL_1 Input Fall Time	t_{CF}			0.2	μs	
CL_1 Input Clock Width (High)	t_{CH}	1.5			μs	
CL_1 Input Clock Width (Low)	t_{CL}	1.5			μs	
Count Clock Oscillation Frequency (X_1, X_2)	f_{XX}		32		KHz	Xtal Oscillation
Count Clock Input Frequency (X_1)	f_X	0		300	KHz	
X_1 Input Rise Time	t_{XR}			0.2	μs	
X_1 Input Fall Time	t_{XF}			0.2	μs	
X_1 Input Clock Width (High)	t_{XH}	1.5			μs	
X_1 Input Clock Width (Low)	t_{XL}	1.5			μs	

Bus I/O Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
ALE Pulse Width (High)	t_{LH}	600			ns	
Address Setup Time to ALE↓	t_{AL}	200			ns	
Address Hold Time after ALE↓	t_{LA}	100			ns	
Output Data Setup Time to $\overline{DOUT}$↑	t_{DDO}	200			ns	
Output Data Hold Time after $\overline{DOUT}$↑	t_{DOD}	100			ns	
$\overline{DOUT}$ Pulse Width (Low)	t_{DOL}	600			ns	
ALE → Data Input Valid Time	t_{LDV}			700	ns	
Address → Data Input Valid Time	t_{ADV}			900	ns	
$\overline{PSEN}$ Pulse Width (Low)	t_{PSL}	1200			ns	
$\overline{PSEN}$ → Data Input Valid Time	t_{PSDV}			600	ns	
$\overline{PSEN}$ → Data Float	t_{PSDF}	0			ns	

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Port 1 I/O Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port 1 Output Setup Time to $\overline{STB}\uparrow$	t_{PST}	200			ns	
Port 1 Output Hold Time after $\overline{STB}\uparrow$	t_{STP}	100			ns	Port Output Mode
$\overline{STB}$ Pulse Width (Low)	t_{STL_1}	600			ns	
Output Data Setup Time to $\overline{STB}\uparrow$	t_{DST}	300			ns	
Output Data Hold Time after $\overline{STB}\uparrow$	t_{STD}	100			ns	
$\overline{STB}\downarrow \rightarrow$ Input Data Valid Time	t_{STDV}			850	ns	
$\overline{STB}\downarrow \rightarrow$ Input Data Float Time	t_{STDF}	0			ns	
Control Setup Time to $\overline{STB}\downarrow$	t_{CST}	200			ns	I/O Expander Mode
Control Hold Time after $\overline{STB}\downarrow$	t_{STC}	100			ns	
$\overline{STB}$ Pulse Width (Low)	t_{STL_2}	1200			ns	
$\overline{CSOUT}$ Setup Time to $\overline{STB}\downarrow$	t_{CSST}	200			ns	
$\overline{CSOUT}$ Hold Time after $\overline{STB}\downarrow$	t_{STCS}	100			ns	

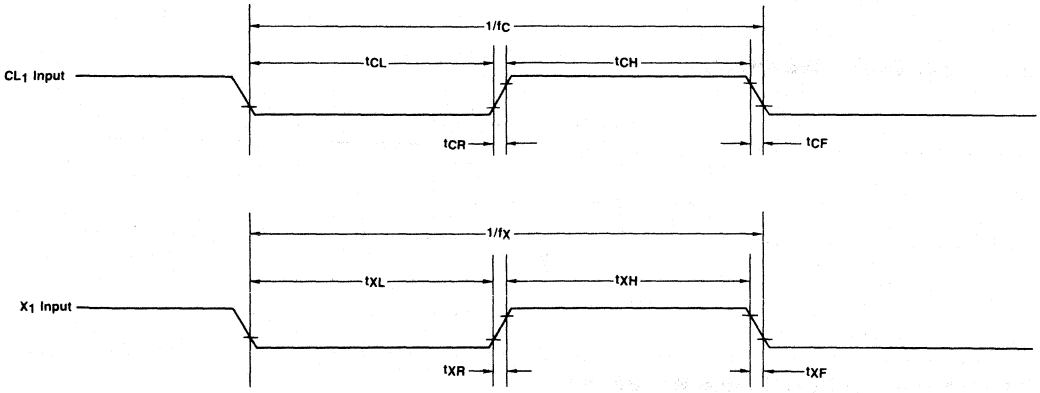
Serial Interface Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ Cycle Time	t_{KCY}	4.0			μs	Input
		6.7			μs	Output
$\overline{SCK}$ Pulse Width High	t_{KH}	1.8			μs	Input
		3.0			μs	Output
$\overline{SCK}$ Pulse Width Low	t_{KL}	1.8			μs	Input
		3.0			μs	Output
SI Setup Time to $\overline{SCK}\uparrow$	t_{SIK}	300			ns	
SI Hold Time after $\overline{SCK}\uparrow$	t_{KSI}	450			ns	
SO Output Delay after $\overline{SCK}\uparrow$	t_{KSO}			850	ns	

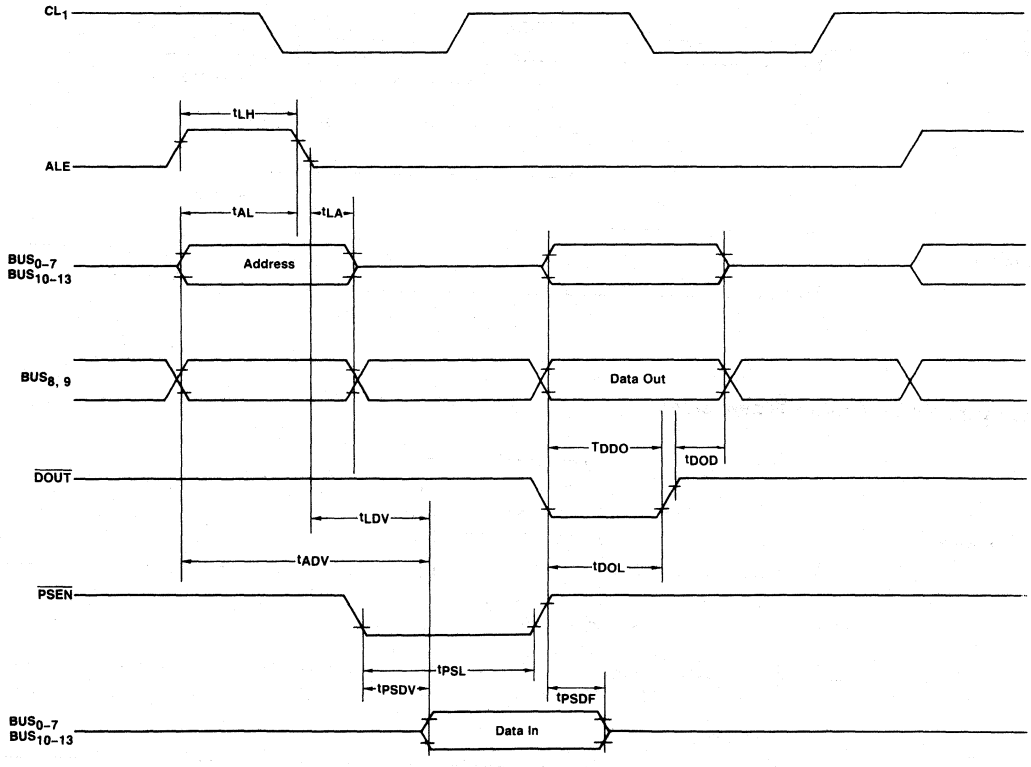
Other Operations

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
INT_0 Pulse Width High	t_{I_0H}	10			μs	
INT_0 Pulse Width Low	t_{I_0L}	10			μs	
INT_1 Pulse Width High	t_{I_1H}	$2/f_\phi$			μs	
INT_1 Pulse Width Low	t_{I_1L}	$2/f_\phi$			μs	
INT_2 Pulse Width High	t_{I_2H}	$2/f_\phi$			μs	
INT_2 Pulse Width Low	t_{I_2L}	$2/f_\phi$			μs	
RESET Pulse Width High	t_{RSH}	10			μs	
RESET Pulse Width Low	t_{RSL}	10			μs	

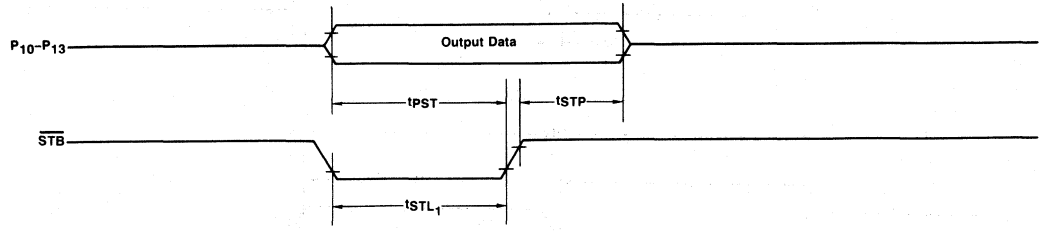
Clock Timing Waveforms



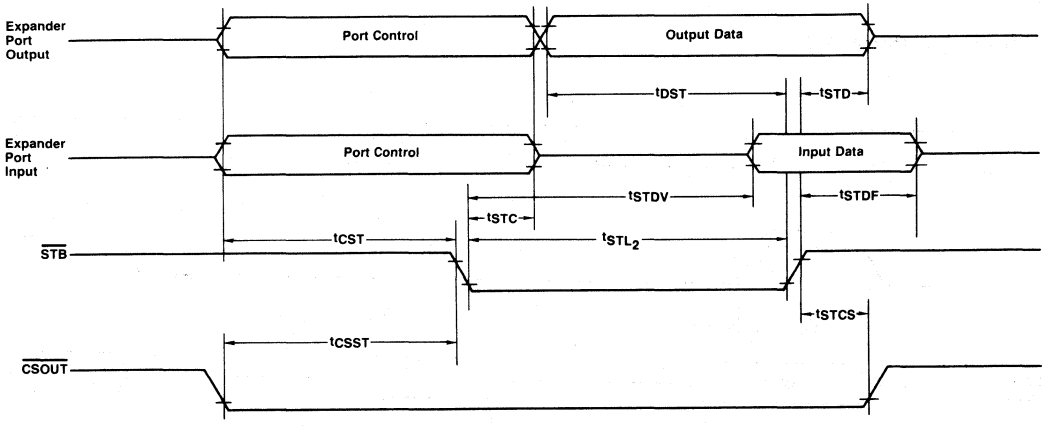
Bus I/O Timing Waveforms



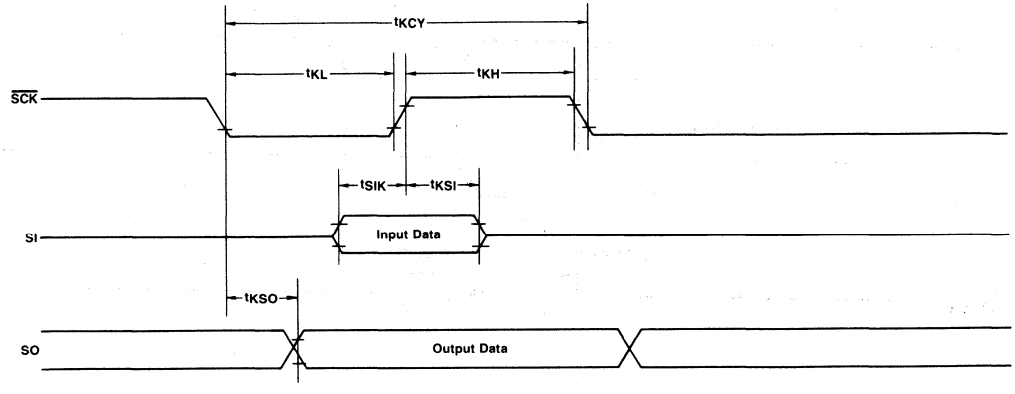
Strobe Output Timing Waveforms



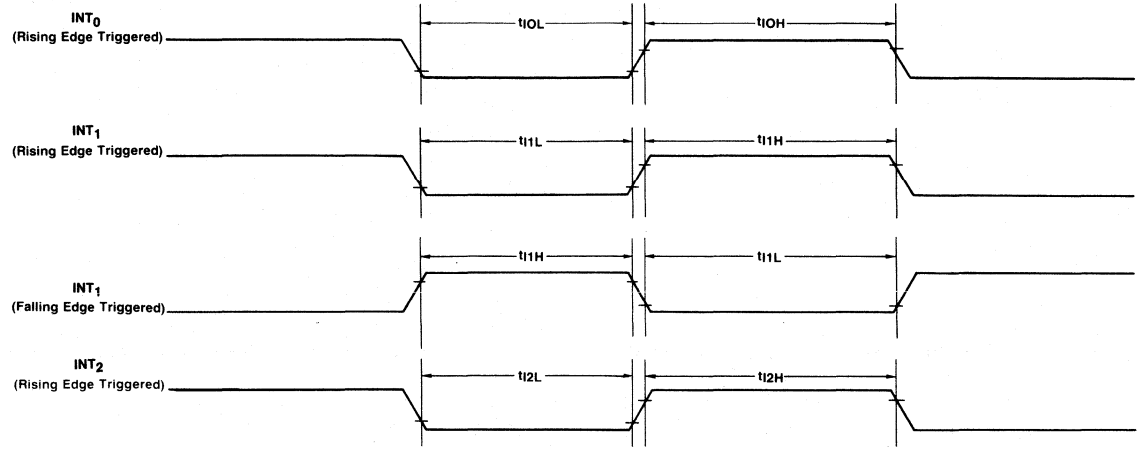
Port 1 I/O Expander Port Timing Waveforms



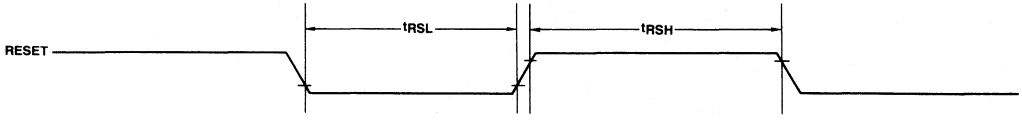
Serial Interface Timing Waveforms



Interrupt Input Timing Waveforms



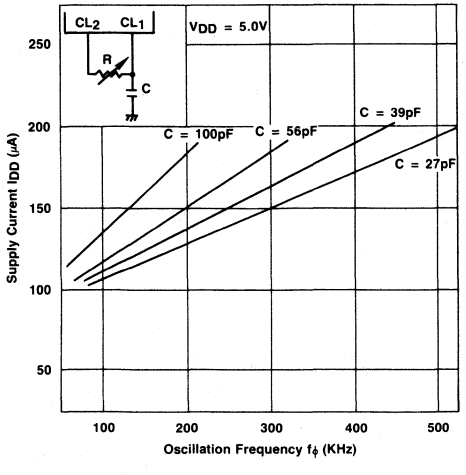
RESET Input Timing



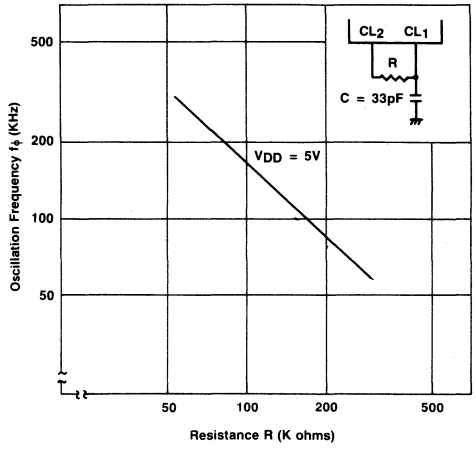
Operating Characteristics

Typical, T_a = 25°C

Supply Current vs System Clock Oscillation Frequency (Note ①)



System Clock Oscillation Frequency vs Resistance



Note:

① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.

HYBRID UV EPROM
4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

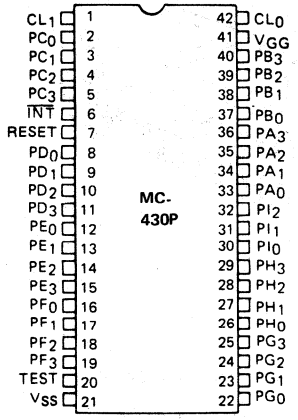
The MC-430P is a hybrid chip containing a μPD556B ROM-less Evaluation chip, a μPD2716 2K x 8-bit UV EPROM, a μPC7905 3-terminal voltage regulator, and pull-up resistors on the same ceramic substrate. The MC-430P is pin-compatible with the μPD546C/μPD547C, and can emulate the high-voltage drive or CMOS μCOM-4 microcomputers with the corresponding I/O line buffers.

The MC-430P contains a 2048 x 8-bit UV EPROM and a 96 x 4-bit RAM which includes six working registers and the flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit timer. The MC-430P executes all 80 instructions of the extended μCOM-4 family instruction set.

The MC-430P provides 35 I/O lines organized into the 4-bit input ports A and B, the 4-bit I/O ports C and D, the 4-bit output ports E, F, G, and H, and the 3-bit output port I. It typically executes its instructions with a 10 μs instruction cycle time. The MC-430P is manufactured with a standard PMOS process, allowing use of a single −10V power supply, and is available in a 42-pin dual-in-line ceramic hybrid package.

PIN CONFIGURATION

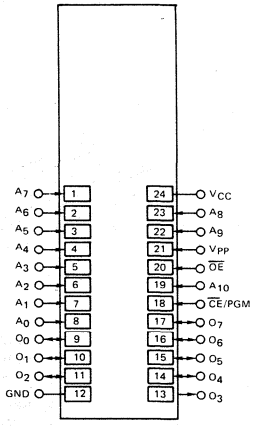
MC-430P (PIN COMPATIBLE WITH μPD546/μPD547)



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

EPROM WRITE PADS (μPD2716)

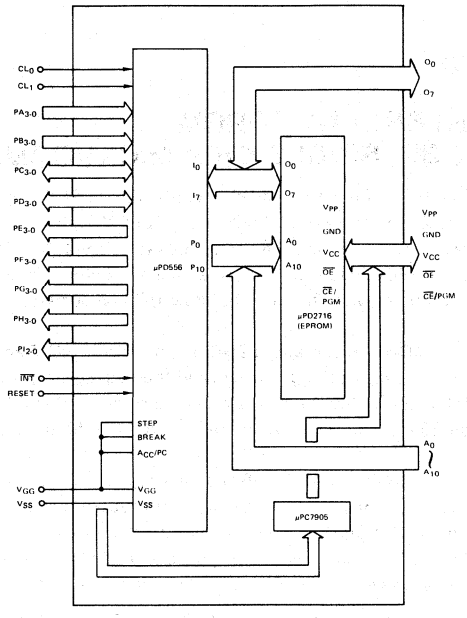


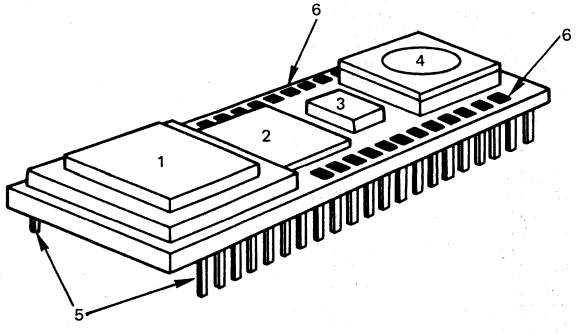
PIN NAMES

A_0-A_{10}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$/PGM	Chip Enable/Program

6

BLOCK DIAGRAM





1 : μPD556
2 : Pull-Up Resistors
3 : μPC7905 (3-Terminal 5 Volt Voltage Regulator)
4 : μPD2716 (EPROM)
5 : μPD546C/μPD547C Compatible Pins (42 Pins)
6 : EPROM Write Pads (24 Pads)

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−25°C to +85°C
Supply Voltage, V_{GG}	−15 to +0.3V
Input Voltages	−15 to +0.3V
Output Voltages	−15 to +0.3V
Output Current (Total, all ports)	−4 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MC-430P 42-PIN OPERATING SPECIFICATIONS

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.0	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL}	−4.3		V_{GG}	V	Ports A through D, $\overline{INT}$, RESET
Clock Voltage High	$V_{\phi H}$	0		−0.8	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, V_I = −1V
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A through D, $\overline{INT}$, RESET, V_I = −11V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H}$ = 0V
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = −11V
Output Voltage High	V_{OH_1}			−1.0	V	Ports C through I, I_{OH} = −1.0 mA
	V_{OH_2}			−2.3	V	Ports C through I, I_{OH} = −3.3 mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C through I, V_O = −11V
Supply Current	I_{GG}		−110	−165	mA	

AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%

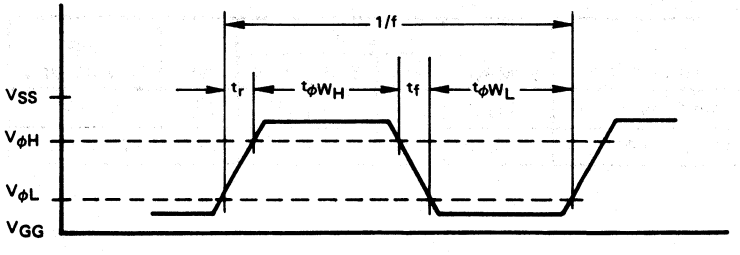
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			40	pF	
Input/Output Capacitance	C_{IO}			30	pF	

CLOCK WAVEFORM



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MC-430P 24-PAD
μPD2716 UV-EPROM
PROGRAMMING SPECIFICATIONS

DC CHARACTERISTICS

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} ① = +5V ± 5%; V_{PP} ①② = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2.0		V_{cc} +1	V	
Input Low Voltage	V_{IL}	-0.1		+0.8	V	
Input Leakage Current	I_{IL}			±10	μA	V_{IN} = 5.25V/0.45V
V_{PP} Current	I_{PP1}			+5	mA	$\overline{CE}/PGM = V_{IL}$ Program Verify / Program Inhibit
	I_{PP2}			+30	mA	$\overline{CE}/PGM = V_{IH}$ Program Mode
V_{CC} Current	I_{CC}			+100	mA	

AC CHARACTERISTICS

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C; V_{CC} ① = +5V ± 5%; V_{PP} ①② = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		120	ns	$\overline{CE}/PGM = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}/PGM = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	5			ns	
Program Pulse Fall Time	t_{PFT}	5			ns	

Test Conditions:

Input Pulse Levels . . . . . 0.8V to 2.2V Output Timing Reference Level . .0.8V and 2V
Input Timing Reference Level. . . . . 1V and 2V

Notes: ① V_{CC} must be applied simultaneously or before Vpp and removed after Vpp.

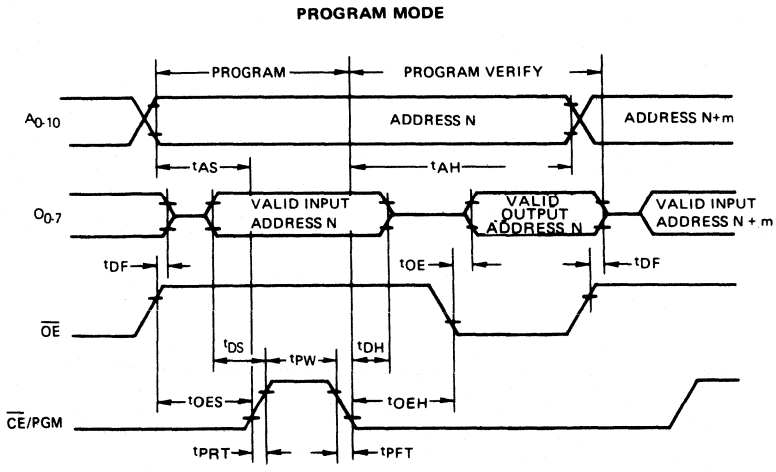
② During programming, program inhibit, and program verify, a maximum of +26V should be applied to the Vpp pin. Overshoot voltages to be generated by the Vpp power supply should be limited to less than +26V.

CAPACITANCE

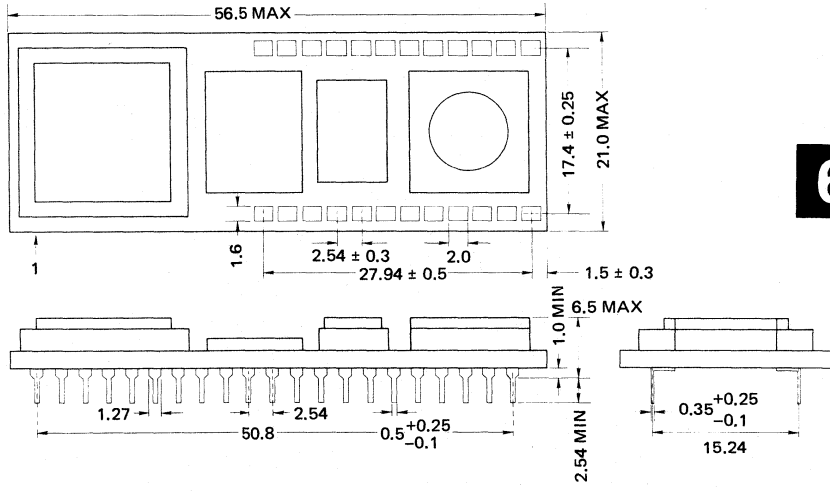
T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			60	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			45	pF	V_{OUT} = 0V

TIMING WAVEFORM



PACKAGE OUTLINE (Units: mm)



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MC-430Pds-12-81-CAT

NEC

NEC Electronics U.S.A. Inc.

Microcomputer Division

MICROCOMPUTERS

SINGLE CHIP 8-BIT MICROCOMPUTERS

7

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER ROM-LESS DEVELOPMENT DEVICE

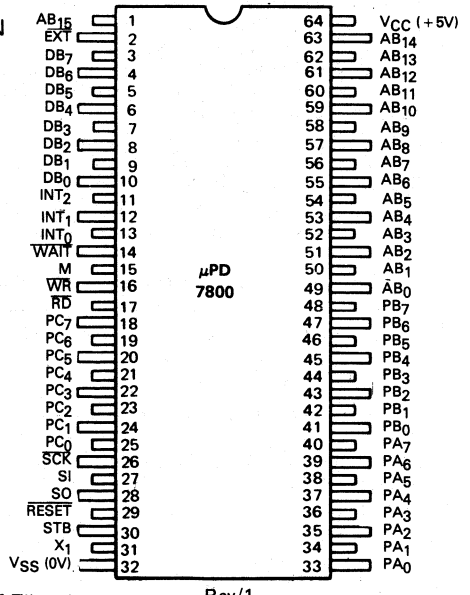
DESCRIPTION

The NEC μPD7800 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-channel Silicon Gate MOS Technology. Intended as a ROM-less development device for NEC μPD7801/7802 designs, the μPD7800 can also be used as a powerful microprocessor in volume production enabling program memory flexibility. Basic on-chip functional blocks include 128 bytes of RAM data memory, 8-bit ALU, 32 I/O lines, Serial I/O port, and 12-bit timer. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of 8080A/8085A peripheral and memory products. Total memory address space is 64K bytes.

FEATURES

- NMOS Silicon Gate Technology Requiring Single +5V Supply.
- Single-Chip Microcomputer with On-Chip ALU, RAM and I/O
  - 128 Bytes RAM
  - 32 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five-Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 64K Byte Memory Address Range
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instruction Set
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities

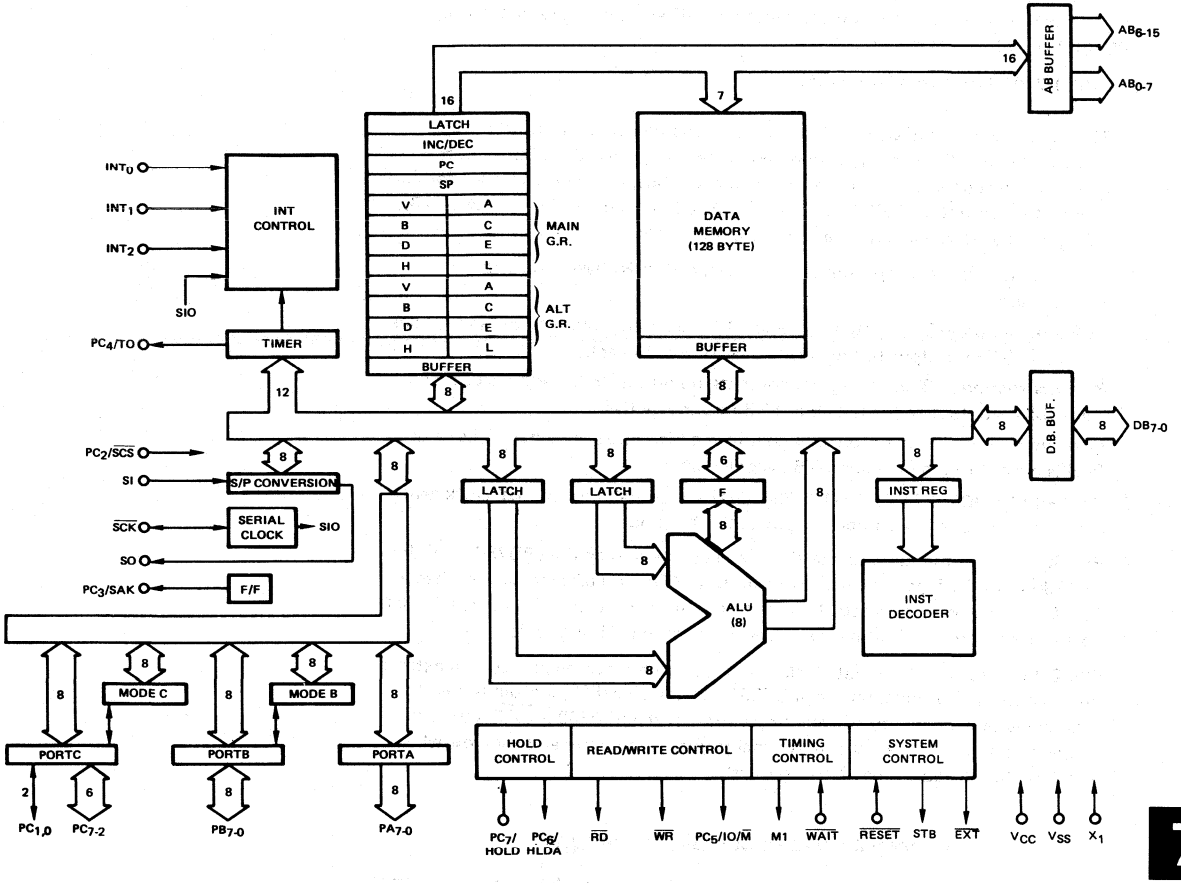
PIN CONFIGURATION



TM: Z80 is a registered trademark of Zilog, Inc.

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Tri-State, Output) 16-bit address bus.
2	$\overline{EXT}$	(Output) $\overline{EXT}$ is used to simulate μPD7801/7802 external memory reference operation. $\overline{EXT}$ distinguishes between internal and external memory references, and goes low when locations 4096 through 65407 are accessed.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices on the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of $\overline{SCK}$.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of $\overline{SCK}$, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7800.
30	STB	(Output) Used to simulate μPD7801/7802 Port E operation, indicating that a Port E operation is being performed when active.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Architecturally consistent with μPD7801/7802 devices, the μPD7800 uses a slightly different pin-out to accommodate for the address bus and lack of on-chip clock generator. For complete μPD7800 functional operation, please refer to μPD7801 product information. Listed below are functional differences that exist between μPD7800 and μPD7801 devices.

μPD7800/7801 Functional Differences

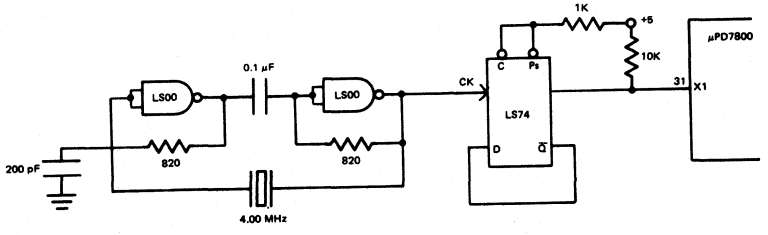
1. The functionality of μPD7801 Port E is somewhat different on the μPD7800. Because the μPD7800 contains no program memory, the address bus is made accessible to address external program memory. Thus, lines normally used for Port E operation with the μPD7801 are used as the address bus on the μPD7800. AB_0-AB_{15} is active during memory access 0 through 4095.
2. Consequently Port E instructions (PEX, PEN, and PER) have different functionality.

   PEX Instruction — The contents of B and C register are output to the address bus. The value 01H is output to the data bus. STB becomes active.

   PEN Instruction — B and C register contents are output to the address bus. The value 02H is output to the data bus. STB becomes active.

   PER Instruction — The address bus goes to the high impedance state. The value 04H is output to the data bus. STB becomes active.
3. ON-CHIP CLOCK GENERATOR. The μPD7800 contains no internal clock generator. An external clock source is input to the X_1 input.
4. PIN 30. This pin functions as the X_2 crystal connection on the μPD7801. On the μPD7800, pin 30 functions as a strobe output (STB) and becomes active when a Port E instruction is executed. This control signal is useful in simulating μPD7801 Port E operation — indicating that a port E operation is being performed.
5. PIN 2. Functions as the Φ out clock output used for synchronizing system external memory and I/O devices, on the μPD7801. On the μPD7800, this pin is used to simulate external memory reference operation of the μPD7801. $\overline{EXT}$ is used to distinguish between internal and external memory references and goes low when location 4096 through 65407 are accessed.

RECOMMENDED CLOCK DRIVE CIRCUIT



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10°C ~ +70°C, V_{CC} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5.0V ± 10%

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X_{OUT} Cycle Time	t_{CYX}	454	2000	ns	t_{CYX}
X_{OUT} Low Level Width	t_{XXL}	212		ns	t_{XXL}
X_{OUT} High Level Width	t_{XXH}	212		ns	t_{XXH}

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → X_{OUT} L.E.	t_{RX}	20		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → $\overline{WAIT}$ L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from X_{OUT} L.E.)	t_{WTS}	180		ns	
$\overline{WAIT}$ Hold Time (Referenced from X_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	t_{CYX} = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
X_{OUT} L.E. → $\overline{WR}$ L.E.	t_{XW}		270	ns	
Address (PE_{0-15}) → X_{OUT} T.E.	t_{AX}		300	ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

AC CHARACTERISTICS (CONT.)

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

PEN, PEX, PER OPERATION

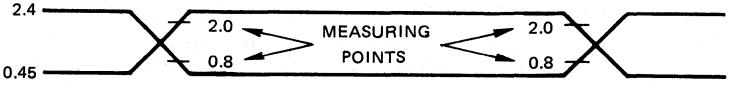
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
X_1 L.E. → $\overline{EXT}$	t_{XE}		250	ns	t_{CYX} = 500 ns
Address (AB_{0-15}) → STB L.E.	t_{AST}	200			
Data (DB_{0-7}) → STB L.E.	t_{DST}	200			
STB Hold Time	t_{STST}	300			
STB → Data	t_{STD}	400			

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from X_{OUT} L.E.)	t_{HDS_1}	100		ns	
	t_{HDS_2}	100		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	100		ns	
X_{OUT} L.E. → HLDA	t_{XHA}		100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

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AC CHARACTERISTICS (CONT.)

t_{CYX} DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
t_{RX}	(1/25) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
t_{XW}	(27/50) T	MAX	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns
t_{AST}	(2/5) T	MIN	ns
t_{DST}	(2/5) T	MIN	ns
t_{STST}	(3/5) T	MIN	ns
t_{STD}	(4/5) T	MIN	ns

Notes: ① N = Number of Wait States

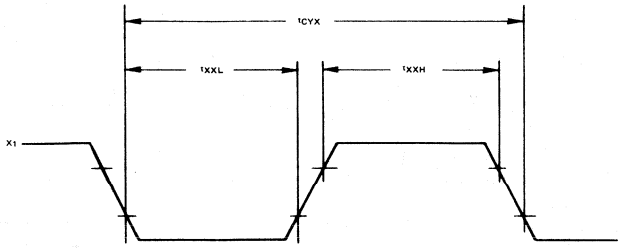
② T = t_{CYX}

③ Only above parameters are t_{CYX} dependent

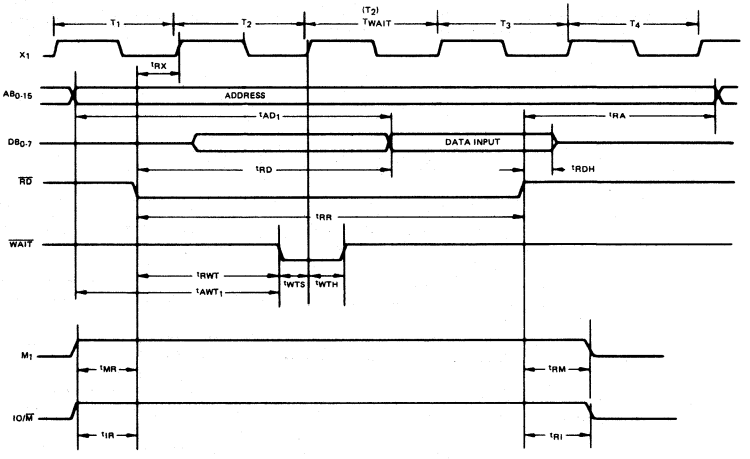
④ When a crystal frequency other than 4 MHz is used (t_{CYX} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

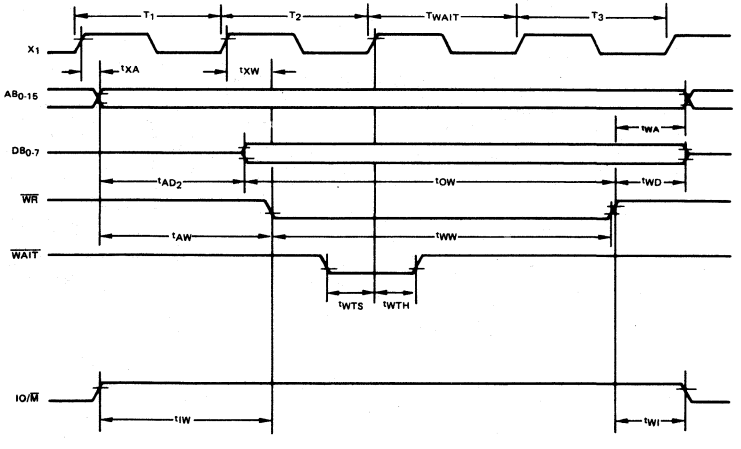
CLOCK TIMING



READ OPERATION



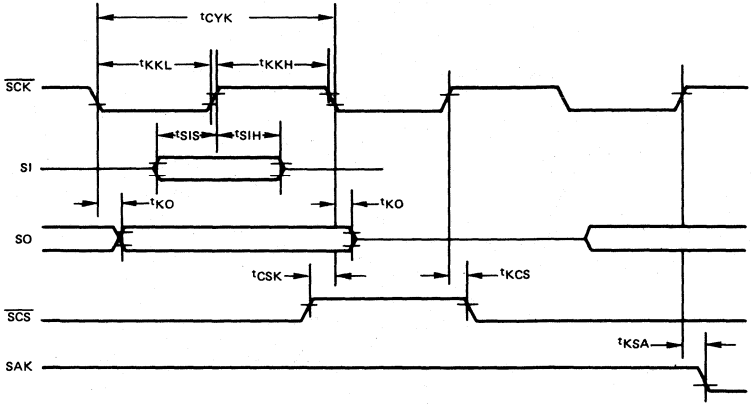
WRITE OPERATION



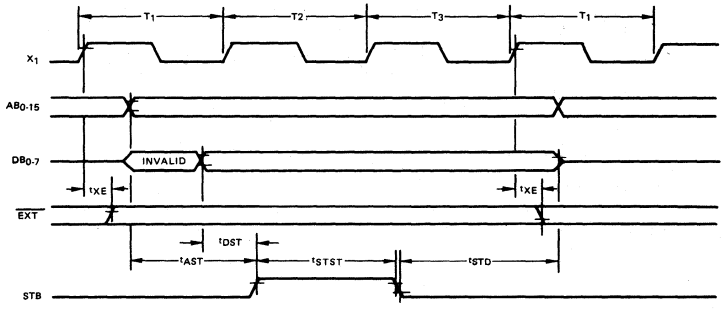
7

TIMING WAVEFORMS (CONT.)

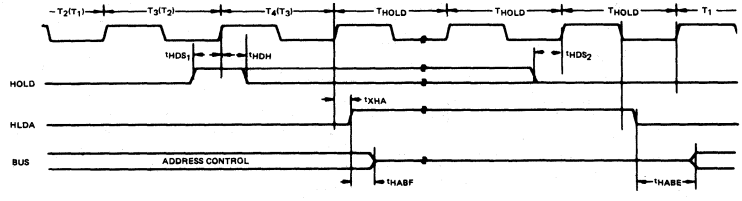
SERIAL I/O OPERATION



PEN, PEX, PER OPERATION

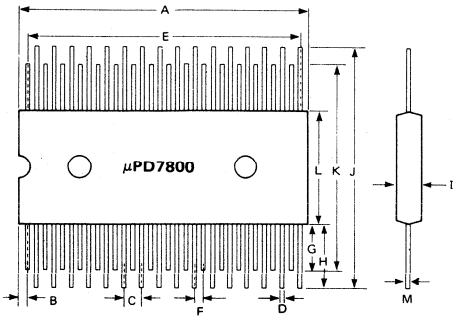


HOLD OPERATION



PACKAGE OUTLINE
μPD7800C

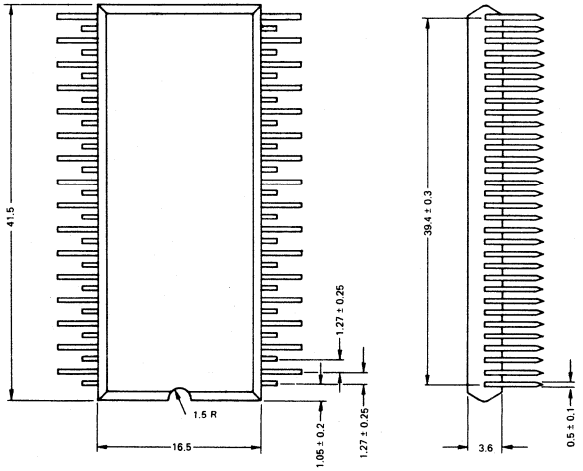
STRAIGHT LEADS



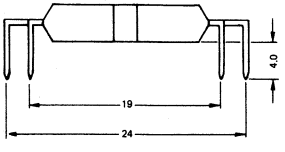
(Plastic)

ITEM	MILLIMETERS	INCHES
A	41.8 MAX.	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	39.37	1.55
F	1.27	0.05
G	6.75	0.27
H	9.3	0.37
I	3.6	0.14
J	35.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

BENT LEADS



(Unit:mm)



7800DS-REV1-12-81-CAT

NEC
NEC Electronics U.S.A. Inc.
Microcomputer Division

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 4K ROM

PRODUCT DESCRIPTION

The NEC μPD7801 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology.

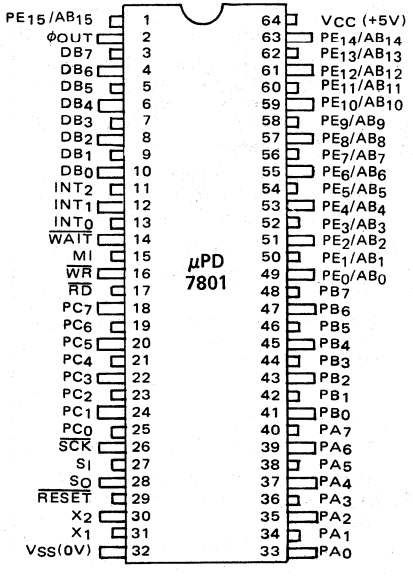
The NEC μPD7801 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks – 4096 x 8 of ROM program memory, 128 x 8 of RAM data memory, 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance stand-alone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instruction set coupled with 4K bytes of ROM program memory and 128 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7801 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
  - 4K Bytes ROM
  - 128 Bytes RAM
  - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 60K Bytes External Memory Address Range
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instruction Set
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities

PIN CONFIGURATION



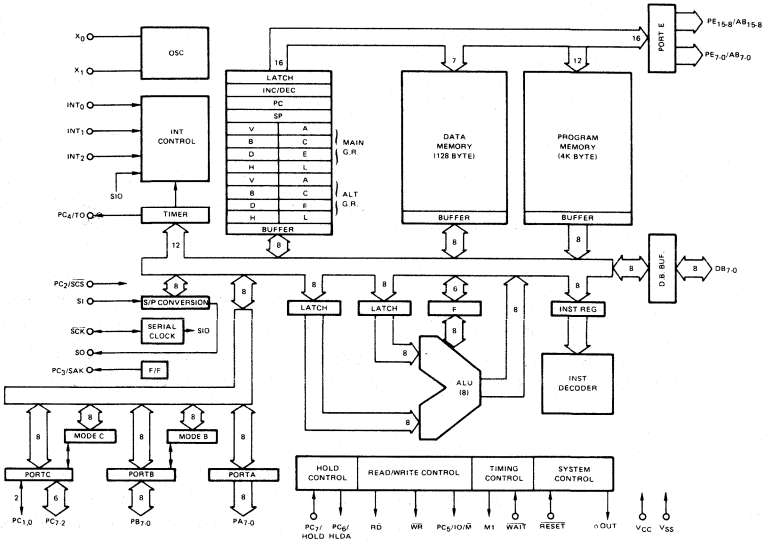
TM: Z80 is a registered trademark of Zilog, Inc.

Rev/1

PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	PE_0/AB_0-	(Tri-State, Output) 16-bit address bus.
2	PE_{15}/AB_{15}	
	ϕOUT	(Output) ϕOUT provides a prescaled output clock for use with external I/O devices or memories. ϕOUT frequency is $f_{XTAL}/2$.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7801.
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input.
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

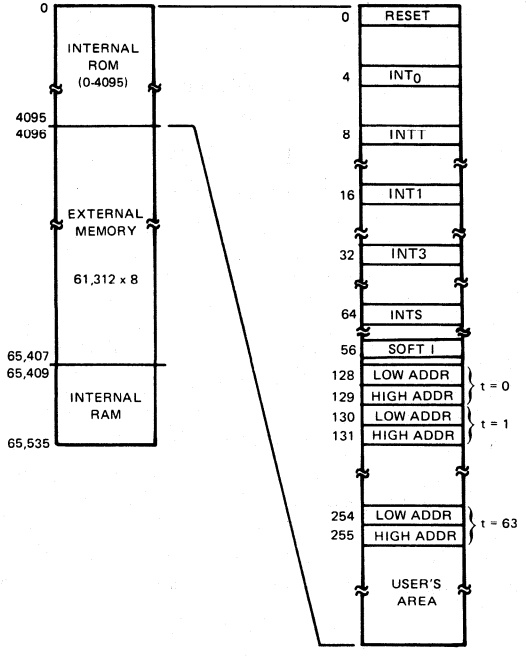
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD7801 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65,408-65,535), any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7801 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the internal ROM area.



I/O Ports

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	8-bit nibble I/O or Control port
Port E	16-bit Address/Output Port

Port A

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output modes. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_{n=1}$) or an Output (Mode $B_{n=0}$).

Port C

Port C is an 8-bit I/O port. The Mode C register is used to program the upper 6 bits of Port C to provide control functions or to set the I/O structure per the following table.

	MODE $C_n = 0$	MODE $C_n = 1$
PC_0	Output	Input
PC_1	Output	Input
PC_2	$\overline{SCS}$ Input	Input
PC_3	SAK Output	Output
PC_4	To Output	Output
PC_5	IO/$\overline{M}$ Output	Output
PC_6	HLDA Output	Output
PC_7	HOLD Input	Input

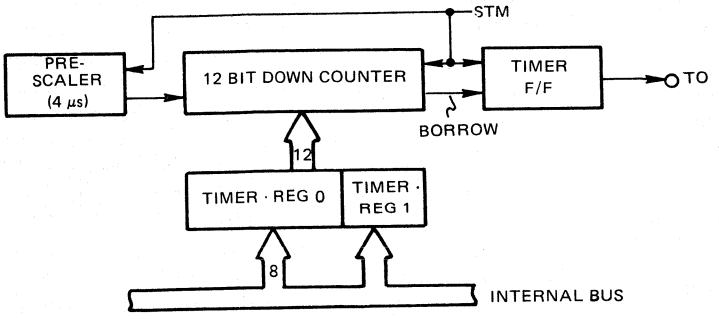
Port E

Port E is a 16-bit address bus/output port. It can be set to one of three operating modes using the PER, PEN, or PEX instructions.

- 16-Bit Address Bus — the Per instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 4-Bit Output Port/12 Bit Address Bus — the PEN instruction sets this mode which allows for memory expansion of up to 4K bytes, externally, plus the transfer of 4-bit nibbles.
- 16-Bit Output Port — the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

FUNCTIONAL DESCRIPTION (CONT.)

Timer Operation



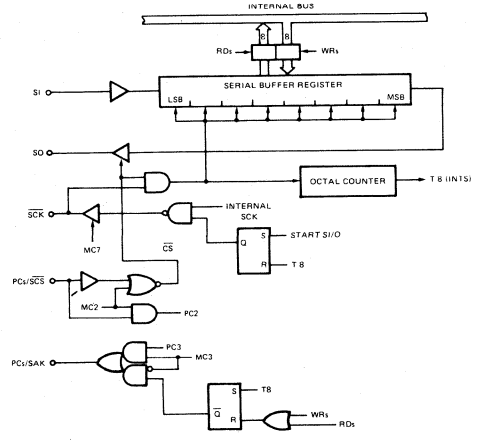
TIMER BLOCK DIAGRAM

A programmable 12-bit timer is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 4 μs to 16 μs in duration. The timer consists of a prescaler which decrements a 12-bit counter at a fixed 4 μs rate. Count pulses are loaded into the 12-bit down counter through timer register (TM0 and TM1). Count-down operation is initiated upon extension of the STM instruction when the contents of the down counter are fully decremented and a borrow operation occurs, an interval interrupt (INTT) is generated. At the same time, the contents of TM0 and TM1 are reloaded into the down-counter and countdown operation is resumed. Count operation may be restarted or initialized with the STM instruction. The duration of the timeout may be altered by loading new contents into the down counter.

The timer flip flop is set by the STM instruction and reset on a countdown operation. Its output (T0) is available externally and may be used in a single pulse mode or general external synchronization.

Timer interrupt (INTT) may be disabled through the interrupt.

Serial Port Operation



SERIAL PORT BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (CONT.)

The on-chip serial port provides basic synchronous serial communication functions allowing the NEC μPD7801 to serially interface with external devices.

Serial Transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at 1 Mbit/second if the internal clock is used or is variable between DC and 1 Mbit/second when an external clock is used. The Clock Source Select is determined by the Mode C register. The serial clock (internal or external $\overline{SCK}$) is enabled when the Serial Chip Select Signal ($\overline{SCS}$) goes low. At this time receive and transmit operations through the Serial Input port (SI)/Serial Output port (SO) are enabled. Receive and transmit operations are performed MSB first.

Serial Acknowledge (SAK) goes high when data transfers between the accumulator and Serial Register is completed. SAK goes low when the buffer becomes full after the completion of serial data receive or transmit operations. While SAK is low, no further data can be received.

Interrupt Structure

The μPD7801 provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from six different sources; three external interrupts, two internal interrupts, and non-maskable software interrupt. Each interrupt when activated branches to a designated memory vector location for that interrupt.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INTT	8	3	Internal, Timer Overflow
INTS	64	6	Internal, Serial Buffer Full/Empty
INT0	4	2	Ext., level sensitive
INT1	16	4	Ext., Rising edge sensitive
INT2	32	5	Ext., Rising/Falling edge sensitive
SOFTI	96	1	Software Interrupt

FUNCTIONAL DESCRIPTION (CONT.)

$\overline{\text{RESET}}$ (Reset)

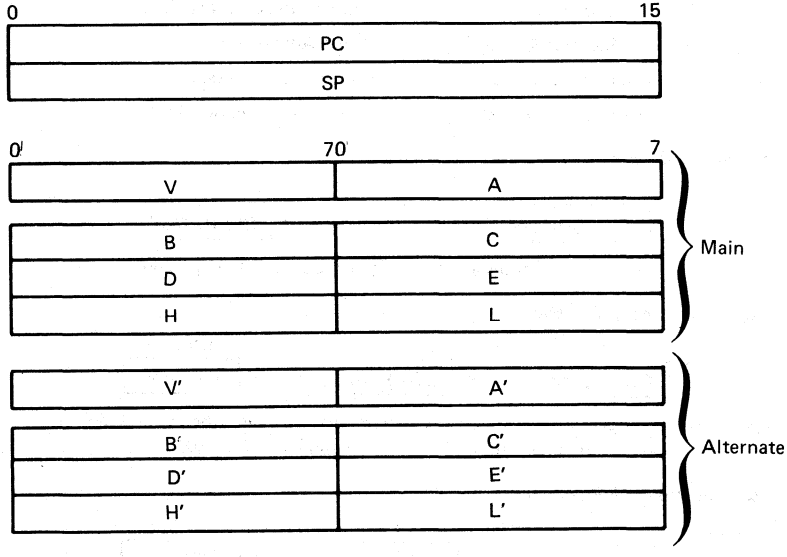
An active low-signal on this input for more than 4 μs forces the μPD7801 into a Reset condition. $\overline{\text{RESET}}$ affects the following internal functions:

- The Interrupt Enable Flags are reset, and Interrupts are inhibited.
- The Interrupt Request Flag is reset.
- The HALT flip flop is reset, and the Halt-state is released.
- The contents of the MODE B register are set to FF_H, and Port B becomes an input port.
- The contents of the MODE C register are set to FF_H. Port C becomes an I/O port and output lines go low.
- All Flags are reset to 0.
- The internal COUNT register for timer operation is set to FFF_H and the timer F/F is reset.
- The ACK F/F is set.
- The HLDA F/F is reset.
- The contents of the Program Counter are set to 0000_H.
- The Address Bus ($PE_{0\text{-}15}$), Data Bus ($DB_{0\text{-}7}$), $\overline{\text{RD}}$, and $\overline{\text{WR}}$ go to a high impedance state.

Once the $\overline{\text{RESET}}$ input goes high, the program is started at location 0000_H.

REGISTERS

The μPD7801 contains sixteen 8-bit registers and two 16-bit registers.



General Purpose Registers (B, C, D, E, H, L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement addressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

FUNCTIONAL DESCRIPTION (CONT.)

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters.

Accumulator (A)

All data transfers between the μPD7801 and external memory or I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

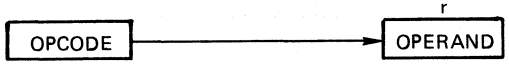
Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

ADDRESS MODES

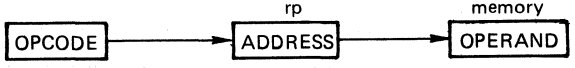
Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing

Register Addressing



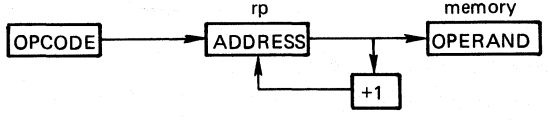
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

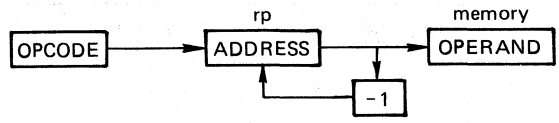
Auto-Increment Addressing



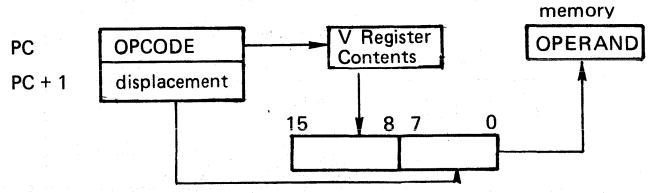
The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

ADDRESS MODES (CONT.)

Auto-Decrement Addressing

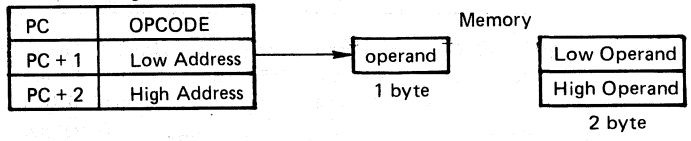


Working Register Addressing



The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

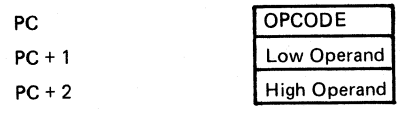
Direct Addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing

Immediate Extended Addressing



7

Operand Description

OPERAND	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA PB PC MK MB MC TM0 TM1 S
sr1	PA PB PC MK S
sr2	PA PB PC MK
rp	SP, B, D, H
rp1	V, B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	F0, F1, F2, FT, FS,

Notes:
1. When special register operands sr, sr1, sr2 are used; PA=Port A, PB=Port B, PC=Port C, MK=Mask Register, MB=Mode B Register, MC=Mode C Register, TM0=Timer Register 0, TM1=Timer Register 1, S=Serial Register.
2. When register pair operands rp, rp1 are used; SP=Stack Pointer, B=BC, D=DE, H=HL, V=VA.
3. Operands rPa, rPa1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes.
   B=(BC), D=(DE), H=(HL)
   $D+=(DE)^{+}$, $H+=(HL)^{+}$, $D-=(DE)^{-}$, $H-=(HL)^{-}$.
4. When the interrupt operand f is used; F0=INTF0, F1=INTF1, F2=INTF2, FT=INTFT, FS=INTFS.

INSTRUCTION GROUPS

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
8-BIT DATA TRANSFER							
MOV	r1, A	1	4	r1 ← A			
MOV	A, r1	1	4	A ← r1			
MOV	sr, A	2	10	sr ← A			
MOV	A, sr1	2	10	A ← sr1			
MOV	r, word	4	17	r ← (word)			
MOV	word, r	4	17	(word) ← r			
MVI	r, byte	2	7	r ← byte			
MVIW	wa, byte	3	13	(V, wa) ← byte			
MVIX	rpa1, byte	2	10	(rpa1) ← byte			
STAW	wa	2	10	(V, wa) ← A			
LDAW	wa	2	10	A ← (V, wa)			
STAX	rpa	1	7	(rpa) ← A			
LDAX	rpa	1	7	A ← (rpa)			
EXX		1	4	Exchange register sets			
EX		1	4	V, A ↔ V, A			
BLOCK		1	13 (C+1)	$(DE)^{+} \leftarrow (HL)^{+}$, C ← C − 1			
16-BIT DATA TRANSFER							
SBCD	word	4	20	(word) ← C, (word + 1) ← B			
SDED	word	4	20	(word) ← E, (word + 1) ← D			
SHLD	word	4	20	(word) ← L, (word + 1) ← H			
SSPD	word	4	20	(word) ← SP_L, (word + 1) ← SP_H			
LBCD	word	4	20	C ← (word), B ← (word + 1)			
LDED	word	4	20	E ← (word), D ← (word + 1)			
LHLD	word	4	20	L ← (word), H ← (word + 1)			
LSPD	word	4	20	SP_L ← (word), SP_H ← (word + 1)			
PUSH	rp1	2	17	(SP − 1) ← $rp1_H$, (SP − 2) ← $rp1_L$			
POP	rp1	2	15	$rp1_L$ ← (SP) $rp1_H$ ← (SP + 1), SP ← SP + 2			
LXI	rp, word	3	10	rp ← word			
TABLE		1	19	C ← (PC + 2 + A) B ← (PC + 2 + A + 1)			

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
ARITHMETIC							
ADD	A, r	2	8	A ← A + r		↕	↕
ADD	r, A	2	8	r ← r + A		↕	↕
ADDX	rpa	2	11	A ← A + (rpa)		↕	↕
ADC	A, r	2	8	A ← A + r + CY		↕	↕
ADC	r, A	2	8	r ← r + A + CY		↕	↕
ADCX	rpa	2	11	A ← A + (rpa) + CY		↕	↕
SUB	A, r	2	8	A ← A − r		↕	↕
SUB	r, A	2	8	r ← r − A		↕	↕
SUBX	rpa	2	11	A ← A − (rpa)		↕	↕
SBB	A, r	2	8	A ← A − r − CY		↕	↕
SBB	r, A	2	8	r ← r − A − CY		↕	↕
SBBX	rpa	2	11	A ← A − (rpa) − CY		↕	↕
ADDNC	A, r	2	8	A ← A + r	No Carry	↕	↕
ADDNC	r, A	2	8	r ← r + A	No Carry	↕	↕
ADDNCX	rpa	2	11	A ← A + (rpa)	No Carry	↕	↕
SUBNB	A, r	2	8	A ← A − r	No Borrow	↕	↕
SUBNB	r, A	2	8	r ← r − A	No Borrow	↕	↕
SUBNBX	rpa	2	11	A ← A − (rpa)	No Borrow	↕	↕
LOGICAL							
ANA	A, r	2	8	A ← A ∧ r			↕
ANA	r, A	2	8	r ← r ∧ A			↕
ANAX	rpa	2	11	A ← A ∧ (rpa)			↕
ORA	A, r	2	8	A ← A ∨ r			↕
ORA	r, A	2	8	r ← r ∨ A			↕
ORAX	rpa	2	11	A ← A ∨ (rpa)			↕
XRA	A, r	2	8	A ← A ∨̄ r			↕
XRA	r, A	2	8	A ← r ∨̄ A			↕
XRAX	rpa	2	11	A ← A ∨̄ (rpa)			↕
GTA	A, r	2	8	A − r − 1	No Borrow	↕	↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
LOGICAL (CONT.)							
GTAX	rpa	2	11	A – (rpa) – 1	No Borrow	↕	↕
LTA	A, r	2	8	A – r	Borrow	↕	↕
LTA	r, A	2	8	r – A	Borrow	↕	↕
LTAX	rpa	2	11	A – (rpa)	Borrow	↕	↕
ONA	A, r	2	8	A ∧ r	No Zero		↕
ONAX	rpa	2	11	A ∧ (rpa)	No Zero		↕
OFFA	A, r	2	8	A ∧ r	Zero		↕
OFFAX	rpa	2	11	A ∧ (rpa)	Zero		↕
NEA	A, r	2	8	A – r	No Zero	↕	↕
NEA	r, A	2	8	r – A	No Zero	↕	↕
NEAX	rpa	2	11	A – (rpa)	No Zero	↕	↕
EQA	A, r	2	8	A – r	Zero	↕	↕
EQA	r, A	2	8	r – A	Zero	↕	↕
EQAX	rpa	2	11	A – (rpa)	Zero	↕	↕
IMMEDIATE DATA TRANSFER (ACCUMULATOR)							
XRI	A, byte	2	7	A ← A ∨ byte			↕
ADINC	A, byte	2	7	A ← A + byte	No Carry	↕	↕
SUINB	A, byte	2	7	A ← A – byte	No Borrow	↕	↕
ADI	A, byte	2	7	A ← A + byte		↕	↕
ACI	A, byte	2	7	A ← A + byte + CY		↕	↕
SUI	A, byte	2	7	A ← A – byte		↕	↕
SBI	A, byte	2	7	A ← A – byte – CY		↕	↕
ANI	A, byte	2	7	A ← A ∧ byte			↕
ORI	A, byte	2	7	A ← A ∨ byte			↕
GTI	A, byte	2	7	A – byte – 1	No Borrow	↕	↕
LTI	A, byte	2	7	A – byte	Borrow	↕	↕
ONI	A, byte	2	7	A ∧ byte	No Zero		↕
OFFI	A, byte	2	7	A ∧ byte	Zero		↕
NEI	A, byte	2	7	A – byte	No Zero	↕	↕
EQI	A, byte	2	7	A – byte	Zero	↕	↕

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER							
XRI	r, byte	3	11	r ← r ∀ byte			↕
ADINC	r, byte	3	11	r ← r + byte	No Carry	↕	↕
SUINB	r, byte	3	11	r ← r − byte	No Borrow	↕	↕
ADI	r, byte	3	11	r ← r + byte		↕	↕
ACI	r, byte	3	11	r ← r + byte + CY		↕	↕
SUI	r, byte	3	11	r ← r − byte		↕	↕
SBI	r, byte	3	11	r ← r − byte − CY		↕	↕
ANI	r, byte	3	11	r ← r ∧ byte		↕	↕
ORJ	r, byte	3	11	r ← r ∨ byte			↕
GTI	r, byte	3	11	r − byte − 1	No Borrow	↕	↕
LTI	r, byte	3	11	r − byte	Borrow	↕	↕
ONI	r, byte	3	11	r ∧ byte	No Zero		↕
OFFI	r, byte	3	11	r ∧ byte	Zero		↕
NEI	r, byte	3	11	r − byte	No Zero	↕	↕
EQI	r, byte	3	11	r − byte	Zero	↕	↕
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER)							
XRI	sr2, byte	3	17	sr2 ← sr2 ∀ byte			↕
ADINC	sr2, byte	3	17	sr2 ← sr2 + byte	No Carry	↕	↕
SUINB	sr2, byte	3	17	sr2 ← sr2 − byte	No Borrow	↕	↕
ADI	sr2, byte	3	17	sr2 ← sr2 + byte		↕	↕
ACI	sr2, byte	3	17	sr2 ← sr2 + byte + CY		↕	↕
SUI	sr2, byte	3	17	sr2 ← sr2 − byte		↕	↕
SBI	sr2, byte	3	17	sr2 ← sr2 − byte − CY		↕	↕
ANI	sr2, byte	3	17	sr2 ← sr2 ∧ byte			↕
ORI	sr2, byte	3	17	sr2 ← sr2 ∨ byte			↕
GTI	sr2, byte	3	14	sr2 − byte − 1	No Borrow	↕	↕
LTI	sr2, byte	3	14	sr2 − byte	Borrow	↕	↕
ONI	sr2, byte	3	14	sr2 ∧ byte	No Zero		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER) (CONT.)							
OFFI	sr2, byte	3	14	sr2 ∧ byte	Zero		↕
NEI	sr2, byte	3	14	sr2 – byte	No Zero	↕	↕
EQI	sr2, byte	3	14	sr2 – byte	Zero	↕	↕
WORKING REGISTER							
XRAW	wa	3	14	A ← A ⊻ (V, wa)			↕
ADDNCW	wa	3	14	A ← A + (V, wa)	No Carry	↕	↕
SUBNBW	wa	3	14	A ← A – (V, wa)	No Borrow	↕	↕
ADDW	wa	3	14	A ← A + (V, wa)		↕	↕
ADCW	wa	3	14	A ← A + (V, wa) + CY		↕	↕
SUBW	wa	3	14	A ← A – (V, wa)		↕	↕
SBBW	wa	3	14	A ← A – (V, wa) – CW		↕	↕
ANAW	wa	3	14	A ← A ∧ (V, wa)			↕
ORAW	wa	3	14	A ← A ∨ (V, wa)			↕
GTAW	wa	3	14	A ← (V, wa) – 1	No Borrow	↕	↕
LTAW	wa	3	14	A – (V, wa)	Borrow	↕	↕
ONAW	wa	3	14	A ∧ (V, wa)	No Zero		↕
OFFAW	wa	3	14	A ∧ (V, wa)	Zero		↕
NEAW	wa	3	14	A – (V, wa)	No Zero	↕	↕
EQAW	wa	3	14	A – (V, wa)	Zero	↕	↕
ANIW	wa, byte	3	16	(V, wa) ← (V, wa) ∧ byte			↕
ORIW	wa, byte	3	16	(V, wa) ← (V, wa) ∨ byte			↕
GTIW	wa, byte	3	13	(V, wa) – byte – 1	No Borrow	↕	↕
LTIW	wa, byte	3	13	(V, wa) – byte	Borrow	↕	↕
ONIW	wa, byte	3	13	(V, wa) ∧ byte	No Zero		↕
OFFIW	wa, byte	3	13	(V, wa) ∧ byte	Zero		↕
NEIW	wa, byte	3	13	(V, wa) – byte	No Zero	↕	↕
EQIW	wa, byte	3	13	(V, wa) – byte	Zero	↕	↕
INCREMENT/DECREMENT							
INR	r2	1	4	r2 ← r2 + 1	Carry		↕
INRW	wa	2	13	(V, wa) ← (V, wa) + 1	Carry		↕

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
INCREMENT/DECREMENT (CONT.)							
DCR	r2	1	4	r2 ← r2 − 1	Borrow		↕
DCRW	wa	2	13	(V, wa) ← (V, wa) − 1	Borrow		↕
INX	rp	1	7	rp ← rp + 1			
DCX	rp	1	7	rp ← rp − 1			
DAA		1	4	Decimal Adjust Accumulator		↕	↕
STC		2	8	CY ← 1		1	
CLC		2	8	CY ← 0		0	
ROTATE AND SHIFT							
RLD		2	17	Rotate Left Digit			
RRD		2	17	Rotate Right Digit			
RAL		2	8	Am + 1 ← Am, A_0 ← CY, CY ← A_7		↕	
RCL		2	8	Cm + 1 ← Cm, C_0 ← CY, CY ← C_7		↕	
RAR		2	8	Am − 1 ← Am, A_7 ← CY, CY ← A_0		↕	
RCR		2	8	Cm − 1 ← Cm, C_7 ← CY, CY ← C_0		↕	
SHAL		2	8	Am + 1 ← Am, A_0 ← 0, CY ← A_7		↕	
SHCL		2	8	Cm + 1 ← CM, C_0 ← 0, CY ← C_7		↕	
SHAR		2	8	Am − 1 ← Am, A_7 ← 0, CY ← A_0		↕	
SHCR		2	8	Cm − 1 ← Cm, C_7 ← 0, CY ← C_0		↕	
JUMP							
JMP	word	3	10	PC ← word			
JB		1	4	PC_H ← B, PC_L ← C			
JR	word	1	13	PC ← PC + 1 + jdisp1			
JRE	word	2	13	PC ← PC + 2 + jdisp			
CALL							
CALL	word	3	16	(SP − 1) ← $(PC - 3)_H$, (SP − 2) ← $(PC - 3)_L$, PC ← word			
CALB		1	13	(SP − 1) ← $(PC - 1)_H$, (SP − 2) ← $(PC - 1)_L$, PC_H ← B, PC_L ← C			
CALF	word	2	16	$(SP-1) \leftarrow (PC-2)_H$, $(SP-2) \leftarrow (PC-2)_L$ PC15 ~ 11 ← 00001, PC10 ~ 0 ← fa			
CALT	word	1	19	$(SP-1) \leftarrow (PC-1)_H$, $(SP-2) \leftarrow (PC-1)_L$ $PC_L \leftarrow (128-2ta)$, $PC_H \leftarrow (129+2ta)$			
SOFTI		1	19	(SP − 1) ← PSW, SP − 2, (SP − 3) ← PC PC ← 0060_H, SIRQ ← 1			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
RETURN							
RET		1	11	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $SP \leftarrow SP - 2$			
RETS		1	11+a	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1),$ $SP \leftarrow SP + 2, PC \leftarrow PC + n$			
RETI		1	15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $PSW \leftarrow (SP+2), SP \leftarrow SP+3, SIRQ \leftarrow 0$			
SKIP							
BIT	bit, wa	2	10	Bit test	$(V, wa)_{bit} = 1)$		
SKC		2	8	Skip if Carry	CY = 1		
SKNC		2	8	Skip if No Carry	CY = 0		
SKZ		2	8	Skip if Zero	Z = 1		
SKNZ		2	8	Skip if No Zero	Z = 0		
SKIT	f	2	8	Skip if INT X = 1, then reset INT X	f = 1		
SKNIT	f	2	8	Skip if No INT X otherwise reset INT X	f = 0		
CPU CONTROL							
NOP		1	4	No Operation			
EI		2	8	Enable Interrupt			
DI		2	8	Disable Interrupt			
HLT		1	6	Halt			
SERIAL PORT CONTROL							
SIO		1	4	Start (Trigger) Serial I/O			
STM		1	4	Start Timer			
INPUT/OUTPUT							
IN	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $A \leftarrow DB_{7-0}$			
OUT	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $DB_{7-0} \leftarrow A$			
PEX		2	11	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$			
PEN		2	11	$PE_{15-12} \leftarrow B_{7-4}$			
PER		2	11	Port E AB Mode			

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Program Status Word (PSW) Operation

OPERATION						D6	D5	D4	D3	D2	D0
REG, MEMORY			IMMEDIATE		SKIP	Z	SK	HC	L1	L0	CY
ADD ADC SUB SBB	ADDW ADCW SUBW SBBW	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAW ORAW XRAW	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCW SUBNBW GTAW LTAW	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		↕	↕	↕	0	0	↕
ONA OFFA	ONAW OFFAW	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAW EQAW	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW					↕	↕	↕	0	0	•
DAA						↕	0	↕	0	0	↕
RAL, RAR, RCL, RCR SHAL, SHAR, SHCL, SHCR						•	0	•	0	0	↕
RLD, RRD						•	0	•	0	0	•
STC						•	0	•	0	0	1
CLC						•	0	•	0	0	0
			MVI A, byte			•	0	•	1	0	•
			MVI L, byte LXI H, word			•	0	•	0	1	•
					BIT SKC SKNC SKZ SKNZ SKIT SKNIT	•	↕	•	0	0	•
					RETS	•	1	•	0	0	•
All other instructions						•	0	•	0	0	•

↕ Flag affected according to result of operation
1 Flag set
0 Flag reset
• Flag not affected

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

−10°C to +70°C, V_{CC} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

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CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

AC CHARACTERISTICS

$-10°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X1 Input Cycle Time	t_{CYX}	227	1000	ns	
X1 Input Low Level Width	t_{XXL}	106		ns	
X1 Input High Level Width	t_{XXH}	106		ns	
ϕ_{OUT} Cycle Time	$t_{CY\phi}$	454	2000	ns	
ϕ_{OUT} Low Level Width	$t_{\phi\phi L}$	150		ns	
ϕ_{OUT} High Level Width	$t_{\phi\phi H}$	150		ns	
ϕ_{OUT} Rise/Fall Time	t_r, t_f		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → ϕ_{OUT} L.E.	$t_{R\phi}$	100		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	$200_{(T3)}$; $700_{(T4)}$		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → WAIT L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from ϕ_{OUT} L.E.)	t_{WTS}	290		ns	
$\overline{WAIT}$ Hold Time (Referenced from ϕ_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	$t_{CY\phi}$ = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
ϕ_{OUT} L.E. → $\overline{WR}$ L.E.	$t_{\phi W}$	40	125	ns	
Address (PE_{0-15}) → ϕ_{OUT} T.E.	$t_{A\phi}$	100	300	ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

AC CHARACTERISTICS
(CONT.)

SERIAL I/O OPERATION

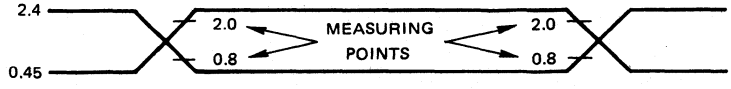
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from ϕ_{OUT} L.E.)	t_{HDS_1}	200		ns	$t_{CY\phi}$ = 500 ns
	t_{HDS_2}	200		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	0		ns	
ϕ_{OUT} L.E. → HLDA	t_{DHA}	110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

$t_{CY\phi}$ DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
$t_{R\phi}$	(1/5) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
$t_{\phi W}$	(1/4) T	MAX	ns
$t_{A\phi}$	(1/5) T	MIN	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns

Notes: ① N = Number of Wait States

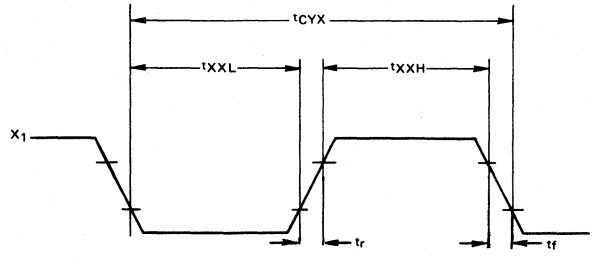
② $T = t_{CY\phi}$

③ Only above parameters are t_{CY_ϕ} dependent

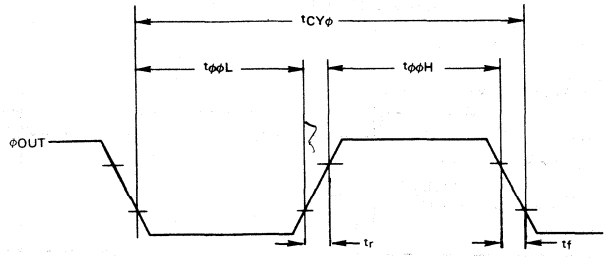
④ When a crystal frequency other than 4 MHz is used (t_{CY_ϕ} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

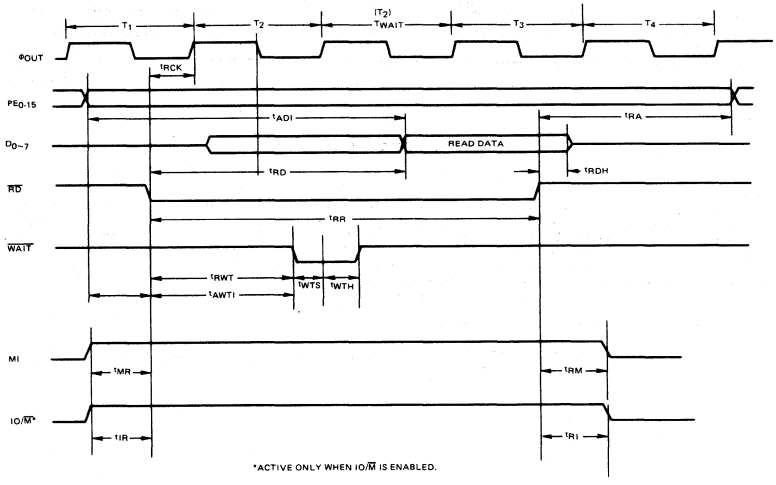
CLOCK TIMING



TIMING WAVEFORMS (CONT.)

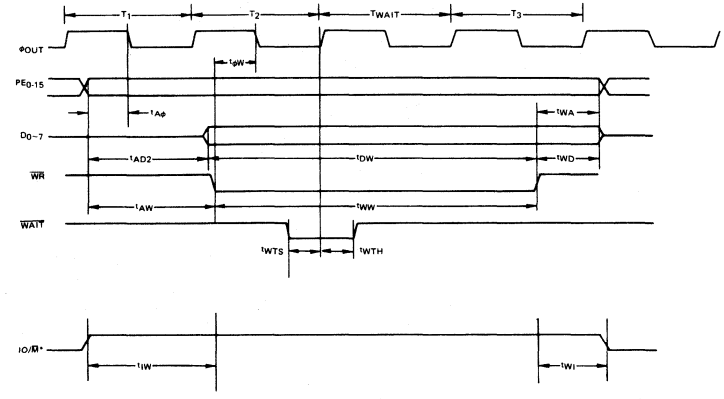


READ OPERATION



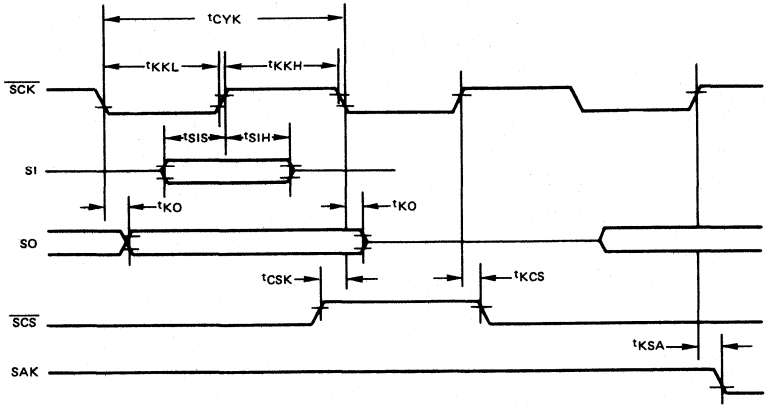
*ACTIVE ONLY WHEN IO/$\overline{M}$ IS ENABLED.

WRITE OPERATION

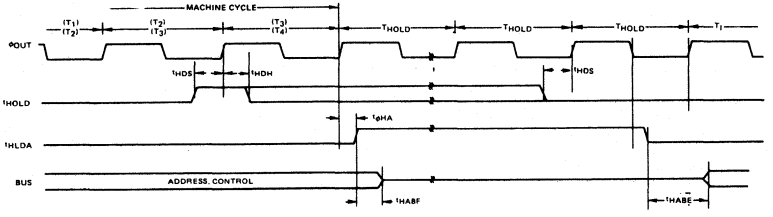


*ACTIVE ONLY WHEN IO/$\overline{M}$ IS ENABLED.

SERIAL I/O OPERATION

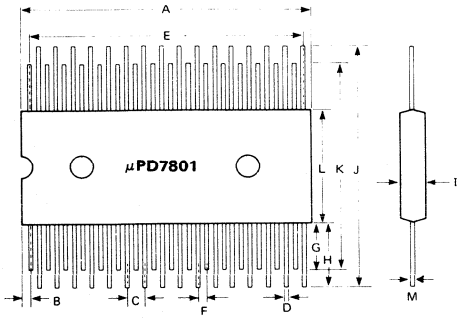


HOLD OPERATION



PACKAGE INFORMATION

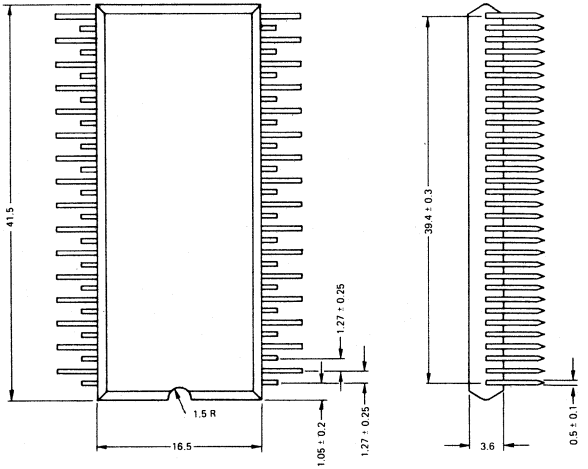
STRAIGHT LEADS



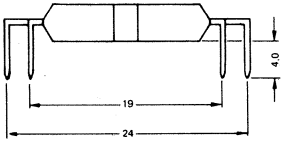
(Plastic)

ITEM	MILLIMETERS	INCHES
A	41.8 MAX.	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 + 0.004
E	39.37	1.55
F	1.27	0.05
G	6.75	0.27
H	9.3	0.37
I	3.6	0.14
J	35.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

BENT LEADS



(Unit:mm)



7801DS-Rev 1-12-81-CAT

NOTES

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 6K ROM

PRODUCT DESCRIPTION

The NEC μPD7802 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology.

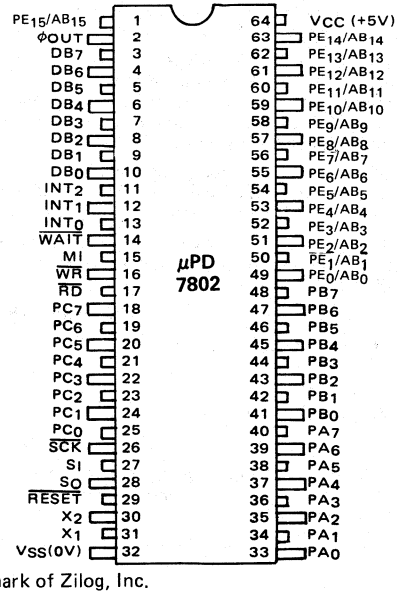
The NEC μPD7802 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks – 6144 x 8 of ROM program memory, 64 x 8 of RAM data memory, 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance stand-alone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instruction set coupled with 6K bytes of ROM program memory and 64 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7802 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
  - 6K Bytes ROM
  - 64 Bytes RAM
  - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 58K Bytes External Memory Address Range
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instruction Set
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities

PIN CONFIGURATION



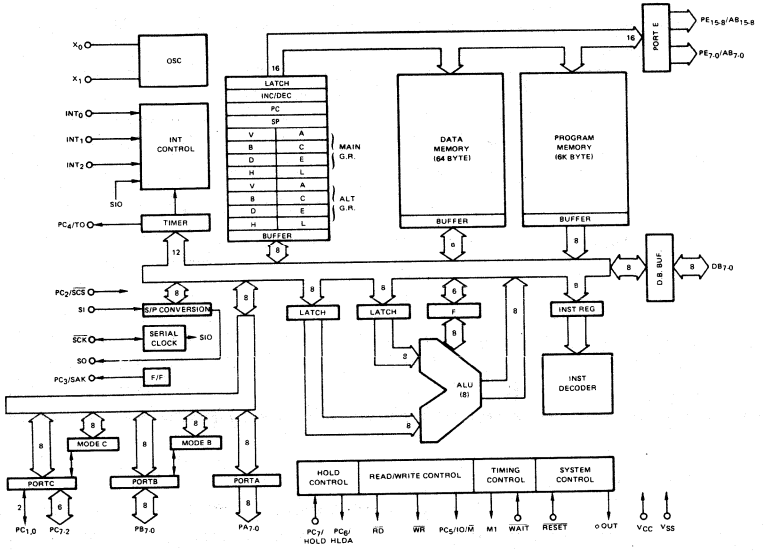
TM: Z80 is a registered trademark of Zilog, Inc.

Rev/1

PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
1, 49-63	PE_0/AB_0-	(Tri-State, Output) 16-bit address bus.
2	PE_{15}/AB_{15}	
	ϕOUT	(Output) ϕOUT provides a prescaled output clock for use with external I/O devices or memories. ϕOUT frequency is $f_{XTAL}/2$.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state T_W and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7802.
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

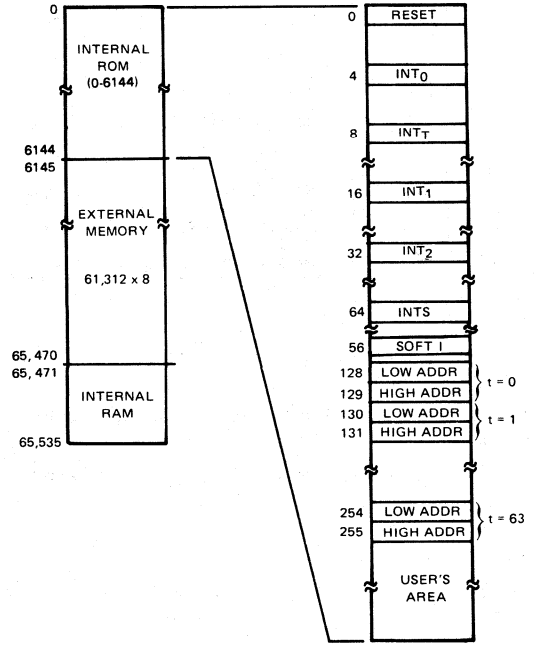
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD7802 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-6144) and RAM (65, 471-65, 535), any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7802 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the Internal ROM area.



I/O PORTS

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	8-bit nibble I/O or Control port
Port E	16-bit Address/Output Port

Port A

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and Logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output modes. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_{n=1}$) or an Output (Mode $B_{n=0}$).

Port C

Port C is an 8-bit I/O port. The Mode C register is used to program the upper 6 bits of Port C to provide control functions or to set the I/O structure per the following table.

	MODE $C_n = 0$	MODE $C_n = 1$
PC_0	Output	Input
PC_1	Output	Input
PC_2	$\overline{SCS}$ Input	Input
PC_3	SAK Output	Output
PC_4	To Output	Output
PC_5	IO/$\overline{M}$ Output	Output
PC_6	HLDA Output	Output
PC_7	HOLD Input	Input

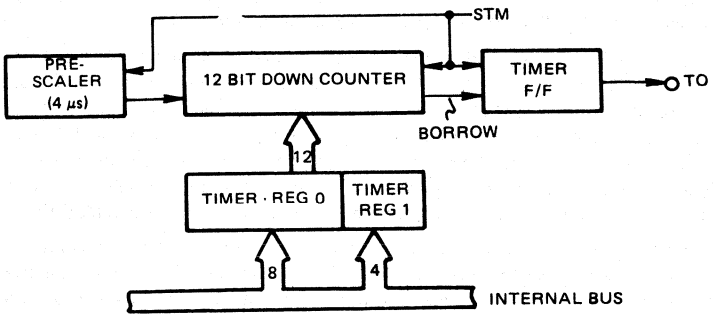
Port E

Port E is a 16-bit address bus/output port. It can be set to one of three operating modes using the PER, PEN, or PEX instructions.

- 16-Bit Address Bus — the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 4-Bit Output Port/12 Bit Address Bus — the PEN instruction sets this mode which allows for memory expansion of an additional 4K bytes, externally, plus the transfer of 4-bit nibbles.
- 16-Bit Output Port — the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

FUNCTIONAL DESCRIPTION (CONT.)

TIMER OPERATION



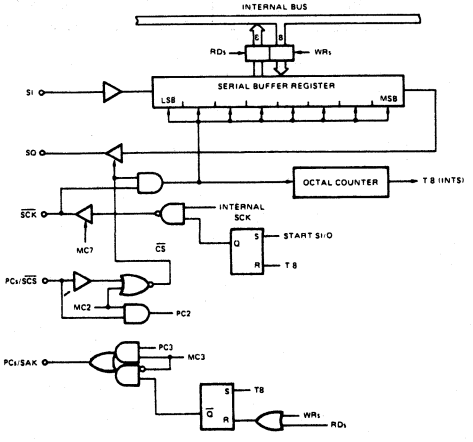
TIMER BLOCK DIAGRAM

A programmable 12-bit timer is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 4 μs to 16 ms in duration. The timer consists of a prescaler which decrements a 12-bit counter at a fixed 4 μs rate. Count pulses are loaded into the 12-bit down counter through timer register (TM0 and TM1). Count-down operation is initiated upon extension of the STM instruction when the contents of the down counter are fully decremented and a borrow operation occurs, an interval interrupt (INTT) is generated. At the same time, the contents of TM0 and TM1 are reloaded into the down-counter and countdown operation is resumed. Count operation may be restarted or initialized with the STM instruction. The duration of the timeout may be altered by loading new contents into the down counter.

The timer flip flop is set by the STM instruction and reset on a countdown operation. Its output (TO) is available externally and may be used in a single pulse mode or general external synchronization.

Timer interrupt (INTT) may be disabled through the interrupt.

SERIAL PORT OPERATION



SERIAL PORT BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (CONT.)

The on-chip serial port provides basic synchronous serial communication functions allowing the NEC μPD7802 to serially interface with external devices.

Serial Transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at 1 Mbit/second if the internal clock is used or is variable between DC and 1 Mbit/second when an external clock is used. The Clock Source Select is determined by the Mode C register. The serial clock (internal or external $\overline{SCK}$) is enabled when the Serial Chip Select Signal ($\overline{SCS}$) goes low. At this time receive and transmit operations through the Serial Input port (SI)/Serial Output port (SO) are enabled. Receive and transmit operations are performed MSB first.

Serial Acknowledge (SAK) goes high when data transfers between the accumulator and Serial Register is completed. SAK goes low when the buffer becomes full after the completion of serial data receive or transmit operations. While SAK is low, no further data can be received.

INTERRUPT STRUCTURE

The μPD7802 provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from six different sources; three external interrupts, two internal interrupts, and a non-maskable software interrupt. Each interrupt when activated branches to a designated memory vector location for that interrupt.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INTT	8	3	Internal, Timer Overflow
INTS	64	6	Internal, Serial Buffer Full/Empty
INT0	4	2	Ext., level sensitive
INT1	16	4	Ext., Rising edge sensitive
INT2	32	5	Ext., Rising/Falling edge sensitive
SOFTI	96	1	Software Interrupt

FUNCTIONAL DESCRIPTION (CONT.)

$\overline{\text{RESET}}$ (Reset)

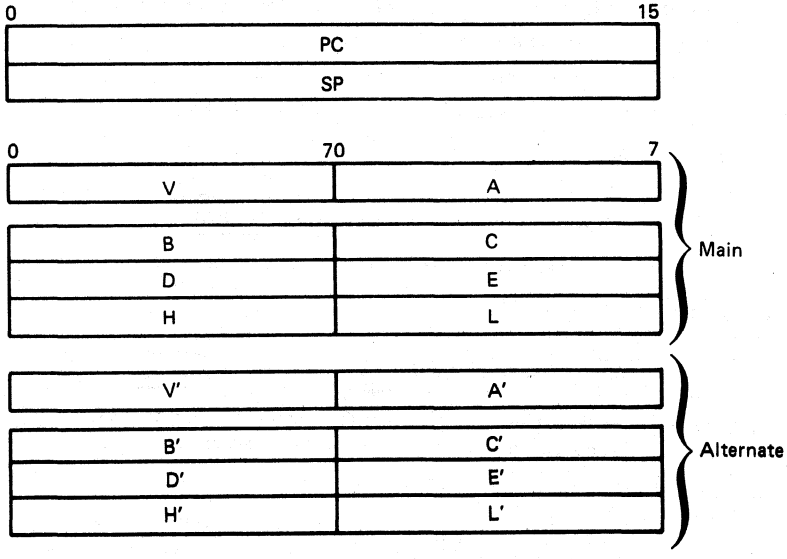
An active low-signal on this input for more than 4 μs forces the μPD7802 into a Reset condition. $\overline{\text{RESET}}$ affects the following internal functions:

- The Interrupt Enable Flags are reset, and Interrupts are inhibited.
- The Interrupt Request Flag is reset.
- The HALT flip flop is reset, and the Halt-state is released.
- The contents of the MODE B register are set to FF_H, and Port B becomes an input port.
- The contents of the MODE C register are set to FF_H. Port C becomes an I/O port and output lines go low.
- All Flags are reset to 0.
- The internal COUNT register for timer operation is set to FFF_H and the timer F/F is reset.
- The ACK F/F is set.
- The HLDA F/F is reset.
- The contents of the Program Counter are set to 0000_H.
- The Address Bus ($PE_{0\text{-}15}$), Data Bus ($DB_{0\text{-}7}$), $\overline{\text{RD}}$, and $\overline{\text{WR}}$ go to a high impedance state.

Once the $\overline{\text{RESET}}$ input goes high, the program is started at location 0000_H.

REGISTERS

The μPD7802 contains sixteen 8-bit registers and two 16-bit registers.



General Purpose Registers (B, C, D, E, H, L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement addressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

FUNCTIONAL DESCRIPTION (CONT.)

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters.

Accumulator (A)

All data transfers between the μPD7802 and external memory or I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

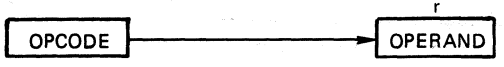
Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

ADDRESS MODES

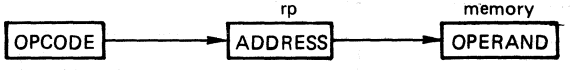
Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing

Register Addressing



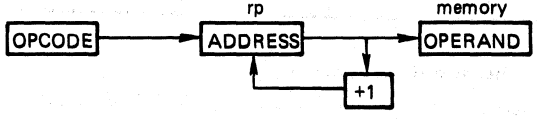
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

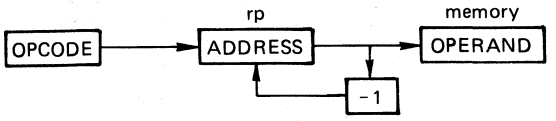
Auto-Increment Addressing



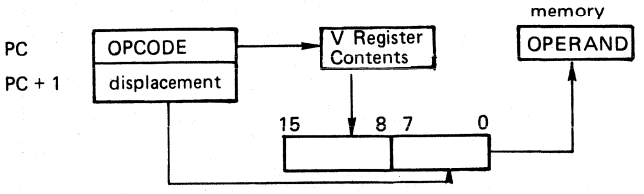
The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

ADDRESS MODES (CONT.)

Auto-Decrement Addressing

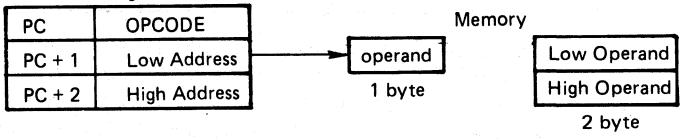


Working Register Addressing



The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

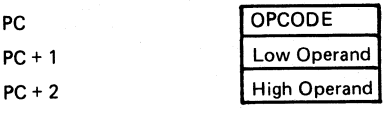
Direct Addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing

Immediate Extended Addressing



7

Operand Description

OPERAND	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA PB PC MK MB MC TM0 TM1 S
sr1	PA PB PC MK S
sr2	PA PB PC MK
rp	SP, B, D, H
rp1	V, B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	F0, F1, F2, FT, FS,

Notes:
1. When special register operands sr, sr1, sr2 are used; PA=Port A, PB=Port B, PC=Port C, MK=Mask Register, MB=Mode B Register, MC=Mode C Register, TM0=Timer Register 0, TM1=Timer Register 1, S=Serial Register.
2. When register pair operands rp, rp1 are used; SP=Stack Pointer, B=BC, D=DE, H=HL, V=VA.
3. Operands rPa, rPa1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes.
   B=(BC), D=(DE), H=(HL)
   $D+=(DE)^+$, $H+=(HL)^+$, $D-=(DE)^-$, $H-=(HL)^-$.
4. When the interrupt operand f is used; F0=INTF0, F1=INTF1, F2=INTF2, FT=INTFT, FS=INTFS.

INSTRUCTION GROUPS

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
8-BIT DATA TRANSFER							
MOV	r1, A	1	4	r1 ← A			
MOV	A, r1	1	4	A ← r1			
MOV	sr, A	2	10	sr ← A			
MOV	A, sr1	2	10	A ← sr1			
MOV	r, word	4	17	r ← (word)			
MOV	word, r	4	17	(word) ← r			
MVI	r, byte	2	7	r ← byte			
MVIW	wa, byte	3	13	(V, wa) ← byte			
MVIX	rpa1, byte	2	10	(rpa1) ← byte			
STAW	wa	2	10	(V, wa) ← A			
LDAW	wa	2	10	A ← (V, wa)			
STAX	rpa	1	7	(rpa) ← A			
LDAX	rpa	1	7	A ← (rpa)			
EXX		1	4	Exchange register sets			
EX		1	4	V, A ↔ V, A			
BLOCK		1	13 (C+1)	$(DE)^+ \leftarrow (HL)^+$, C ← C − 1			
16-BIT DATA TRANSFER							
SBCD	word	4	20	(word) ← C, (word + 1) ← B			
SDED	word	4	20	(word) ← E, (word + 1) ← D			
SHLD	word	4	20	(word) ← L, (word + 1) ← H			
SSPD	word	4	20	(word) ← SP_L, (word + 1) ← SP_H			
LBCD	word	4	20	C ← (word), B ← (word + 1)			
LDED	word	4	20	E ← (word), D ← (word + 1)			
LHLD	word	4	20	L ← (word), H ← (word + 1)			
LSPD	word	4	20	SP_L ← (word), SP_H ← (word + 1)			
PUSH	rp1	2	17	(SP − 1) ← $rp1_H$, (SP − 2) ← $rp1_L$			
POP	rp1	2	15	$rp1_L$ ← (SP) $rp1_H$ ← (SP + 1), SP ← SP + 2			
LXI	rp, word	3	10	rp ← word			
TABLE		1	19	C ← (PC + 2 + A) B ← (PC + 2 + A + 1)			

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
ARITHMETIC							
ADD	A, r	2	8	A ← A + r		↕	↕
ADD	r, A	2	8	r ← r + A		↕	↕
ADDX	rpa	2	11	A ← A + (rpa)		↕	↕
ADC	A, r	2	8	A ← A + r + CY		↕	↕
ADC	r, A	2	8	r ← r + A + CY		↕	↕
ADCX	rpa	2	11	A ← A + (rpa) + CY		↕	↕
SUB	A, r	2	8	A ← A − r		↕	↕
SUB	r, A	2	8	r ← r − A		↕	↕
SUBX	rpa	2	11	A ← A − (rpa)		↕	↕
SBB	A, r	2	8	A ← A − r − CY		↕	↕
SBB	r, A	2	8	r ← r − A − CY		↕	↕
SBBX	rpa	2	11	A ← A − (rpa) − CY		↕	↕
ADDNC	A, r	2	8	A ← A + r	No Carry	↕	↕
ADDNC	r, A	2	8	r ← r + A	No Carry	↕	↕
ADDNCX	rpa	2	11	A ← A + (rpa)	No Carry	↕	↕
SUBNB	A, r	2	8	A ← A − r	No Borrow	↕	↕
SUBNB	r, A	2	8	r ← r − A	No Borrow	↕	↕
SUBNBX	rpa	2	11	A ← A − (rpa)	No Borrow	↕	↕
LOGICAL							
ANA	A, r	2	8	A ← A ∧ r			↕
ANA	r, A	2	8	r ← r ∧ A			↕
ANAX	rpa	2	11	A ← A ∧ (rpa)			↕
ORA	A, r	2	8	A ← A ∨ r			↕
ORA	r, A	2	8	r ← r ∨ A			↕
ORAX	rpa	2	11	A ← A ∨ (rpa)			↕
XRA	A, r	2	8	A ← A ∨̄ r			↕
XRA	r, A	2	8	A ← r ∨̄ A			↕
XRAX	rpa	2	11	A ← A ∨̄ (rpa)			↕
GTA	A, r	2	8	A − r − 1	No Borrow	↕	↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
LOGICAL (CONT.)							
GTAX	rpa	2	11	A – (rpa) – 1	No Borrow	↕	↕
LTA	A, r	2	8	A – r	Borrow	↕	↕
LTA	r, A	2	8	r – A	Borrow	↕	↕
LTAX	rpa	2	11	A – (rpa)	Borrow	↕	↕
ONA	A, r	2	8	A ∧ r	No Zero		↕
ONAX	rpa	2	11	A ∧ (rpa)	No Zero		↕
OFFA	A, r	2	8	A ∧ r	Zero		↕
OFFAX	rpa	2	11	A ∧ (rpa)	Zero		↕
NEA	A, r	2	8	A – r	No Zero	↕	↕
NEA	r, A	2	8	r – A	No Zero	↕	↕
NEAX	rpa	2	11	A – (rpa)	No Zero	↕	↕
EQA	A, r	2	8	A – r	Zero	↕	↕
EQA	r, A	2	8	r – A	Zero	↕	↕
EQAX	rpa	2	11	A – (rpa)	Zero	↕	↕
IMMEDIATE DATA TRANSFER (ACCUMULATOR)							
XRI	A, byte	2	7	A ← A ∨ byte			↕
ADINC	A, byte	2	7	A ← A + byte	No Carry	↕	↕
SUINB	A, byte	2	7	A ← A – byte	No Borrow	↕	↕
ADI	A, byte	2	7	A ← A + byte		↕	↕
ACI	A, byte	2	7	A ← A + byte + CY		↕	↕
SUI	A, byte	2	7	A ← A – byte		↕	↕
SBI	A, byte	2	7	A ← A – byte – CY		↕	↕
ANI	A, byte	2	7	A ← A ∧ byte			↕
ORI	A, byte	2	7	A ← A ∨ byte			↕
GTI	A, byte	2	7	A – byte – 1	No Borrow	↕	↕
LTI	A, byte	2	7	A – byte	Borrow	↕	↕
ONI	A, byte	2	7	A ∧ byte	No Zero		↕
OFFI	A, byte	2	7	A ∧ byte	Zero		↕
NEI	A, byte	2	7	A – byte	No Zero	↕	↕
EQI	A, byte	2	7	A – byte	Zero	↕	↕

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER							
XRI	r, byte	3	11	r ← r ⊻ byte			↕
ADINC	r, byte	3	11	r ← r + byte	No Carry	↕	↕
SUINB	r, byte	3	11	r ← r − byte	No Borrow	↕	↕
ADI	r, byte	3	11	r ← r + byte		↕	↕
ACI	r, byte	3	11	r ← r + byte + CY		↕	↕
SUI	r, byte	3	11	r ← r − byte		↕	↕
SBI	r, byte	3	11	r ← r − byte − CY		↕	↕
ANI	r, byte	3	11	r ← r ∧ byte		↕	↕
ORJ	r, byte	3	11	r ← r ∨ byte			↕
GTI	r, byte	3	11	r − byte − 1	No Borrow	↕	↕
LTI	r, byte	3	11	r − byte	Borrow	↕	↕
ONI	r, byte	3	11	r ∧ byte	No Zero		↕
OFFI	r, byte	3	11	r ∧ byte	Zero		↕
NEI	r, byte	3	11	r − byte	No Zero	↕	↕
EQI	r, byte	3	11	r − byte	Zero	↕	↕
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER)							
XRI	sr2, byte	3	17	sr2 ← sr2 ⊻ byte			↕
ADINC	sr2, byte	3	17	sr2 ← sr2 + byte	No Carry	↕	↕
SUINB	sr2, byte.	3	17	sr2 ← sr2 − byte	No Borrow	↕	↕
ADI	sr2, byte	3	17	sr2 ← sr2 + byte		↕	↕
ACI	sr2, byte	3	17	sr2 ← sr2 + byte + CY		↕	↕
SUI	sr2, byte	3	17	sr2 ← sr2 − byte		↕	↕
SBI	sr2, byte	3	17	sr2 ← sr2 − byte − CY		↕	↕
ANI	sr2, byte	3	17	sr2 ← sr2 ∧ byte			↕
ORI	sr2, byte	3	17	sr2 ← sr2 ∨ byte			↕
GTI	sr2, byte	3	14	sr2 − byte − 1	No Borrow	↕	↕
LTI	sr2, byte	3	14	sr2 − byte	Borrow	↕	↕
ONI	sr2, byte	3	14	sr2 ∧ byte	No Zero		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER) (CONT.)							
OFFI	sr2, byte	3	14	sr2 ∧ byte	Zero		↕
NEI	sr2, byte	3	14	sr2 – byte	No Zero	↕	↕
EQI	sr2, byte	3	14	sr2 – byte	Zero	↕	↕
WORKING REGISTER							
XRAW	wa	3	14	A ← A ⊻ (V, wa)			↕
ADDNCW	wa	3	14	A ← A + (V, wa)	No Carry	↕	↕
SUBNBW	wa	3	14	A ← A – (V, wa)	No Borrow	↕	↕
ADDW	wa	3	14	A ← A + (V, wa)		↕	↕
ADCW	wa	3	14	A ← A + (V, wa) + CY		↕	↕
SUBW	wa	3	14	A ← A – (V, wa)		↕	↕
SBBW	wa	3	14	A ← A – (V, wa) – CW		↕	↕
ANAW	wa	3	14	A ← A ∧ (V, wa)			↕
ORAW	wa	3	14	A ← A ∨ (V, wa)			↕
GTAW	wa	3	14	A ← (V, wa) – 1	No Borrow	↕	↕
LTAW	wa	3	14	A – (V, wa)	Borrow	↕	↕
ONAW	wa	3	14	A ∧ (V, wa)	No Zero		↕
OFFAW	wa	3	14	A ∧ (V, wa)	Zero		↕
NEAW	wa	3	14	A – (V, wa)	No Zero	↕	↕
EQAW	wa	3	14	A – (V, wa)	Zero	↕	↕
ANIW	wa, byte	3	16	(V, wa) ← (V, wa) ∧ byte			↕
ORIW	wa, byte	3	16	(V, wa) ← (V, wa) ∨ byte			↕
GTIW	wa, byte	3	13	(V, wa) – byte – 1	No Borrow	↕	↕
LTIW	wa, byte	3	13	(V, wa) – byte	Borrow	↕	↕
ONIW	wa, byte	3	13	(V, wa) ∧ byte	No Zero		↕
OFFIW	wa, byte	3	13	(V, wa) ∧ byte	Zero		↕
NEIW	wa, byte	3	13	(V, wa) – byte	No Zero	↕	↕
EQIW	wa, byte	3	13	(V, wa) – byte	Zero	↕	↕
INCREMENT/DECREMENT							
INR	r2	1	4	r2 ← r2 + 1	Carry		↕
INRW	wa	2	13	(V, wa) ← (V, wa) + 1	Carry		↕

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
INCREMENT/DECREMENT (CONT.)							
DCR	r2	1	4	r2 ← r2 − 1	Borrow		↕
DCRW	wa	2	13	(V, wa) ← (V, wa) − 1	Borrow		↕
INX	rp	1	7	rp ← rp + 1			
DCX	rp	1	7	rp ← rp − 1			
DAA		1	4	Decimal Adjust Accumulator		↕	↕
STC		2	8	CY ← 1		1	
CLC		2	8	CY ← 0		0	
ROTATE AND SHIFT							
RLD		2	17	Rotate Left Digit			
RRD		2	17	Rotate Right Digit			
RAL		2	8	Am + 1 ← Am, A_0 ← CY, CY ← A_7		↕	
RCL		2	8	Cm + 1 ← Cm, C_0 ← CY, CY ← C_7		↕	
RAR		2	8	Am − 1 ← Am, A_7 ← CY, CY ← A_0		↕	
RCR		2	8	Cm − 1 ← Cm, C_7 ← CY, CY ← C_0		↕	
SHAL		2	8	Am + 1 ← Am, A_0 ← 0, CY ← A_7		↕	
SHCL		2	8	Cm + 1 ← CM, C_0 ← 0, CY ← C_7		↕	
SHAR		2	8	Am − 1 ← Am, A_7 ← 0, CY ← A_0		↕	
SHCR		2	8	Cm − 1 ← Cm, C_7 ← 0, CY ← C_0		↕	
JUMP							
JMP	word	3	10	PC ← word			
JB		1	4	PC_H ← B, PC_L ← C			
JR	word	1	13	PC ← PC + 1 + jdisp1			
JRE	word	2	13	PC ← PC + 2 + jdisp			
CALL							
CALL	word	3	16	(SP − 1) ← $(PC - 3)_H$, (SP − 2) ← $(PC - 3)_L$, PC ← word			
CALB		1	13	(SP − 1) ← $(PC - 1)_H$, (SP − 2) ← $(PC - 1)_L$, PC_H ← B, PC_L ← C			
CALF	word	2	16	$(SP-1) \leftarrow (PC-2)_H$, $(SP-2) \leftarrow (PC-2)_L$ PC15 ~ 11 ← 00001, PC10 ~ 0 ← fa			
CALT	word	1	19	$(SP-1) \leftarrow (PC-1)_H$, $(SP-2) \leftarrow (PC-1)_L$ $PC_L \leftarrow (128-2ta)$, $PC_H \leftarrow (129+2ta)$			
SOFTI		1	19	(SP − 1) ← PSW, SP − 2, (SP − 3) ← PC PC ← 0060_H, SIRQ ← 1			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
RETURN							
RET		1	11	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $SP \leftarrow SP - 2$			
RETS		1	11+a	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1),$ $SP \leftarrow SP + 2, PC \leftarrow PC + n$			
RETI		1	15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $PSW \leftarrow (SP+2), SP \leftarrow SP+3, SIRQ \leftarrow 0$			
SKIP							
BIT	bit, wa	2	10	Bit test	$(V, wa)_{bit} = 1)$		
SKC		2	8	Skip if Carry	CY = 1		
SKNC		2	8	Skip if No Carry	CY = 0		
SKZ		2	8	Skip if Zero	Z = 1		
SKNZ		2	8	Skip if No Zero	Z = 0		
SKIT	f	2	8	Skip if INT X = 1, then reset INT X	f = 1		
SKNIT	f	2	8	Skip if No INT X otherwise reset INT X	f = 0		
CPU CONTROL							
NOP		1	4	No Operation			
EI		2	8	Enable Interrupt			
DI		2	8	Disable Interrupt			
HLT		1	6	Halt			
SERIAL PORT CONTROL							
SIO		1	4	Start (Trigger) Serial I/O			
STM		1	4	Start Timer			
INPUT/OUTPUT							
IN	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $A \leftarrow DB_{7-0}$			
OUT	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow$ byte $DB_{7-0} \leftarrow A$			
PEX		2	11	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$			
PEN		2	11	$PE_{15-12} \leftarrow B_{7-4}$			
PER		2	11	Port E AB Mode			

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Program Status Word (PSW) Operation

OPERATION						D6	D5	D4	D3	D2	D0
REG, MEMORY			IMMEDIATE		SKIP	Z	SK	HC	L1	L0	CY
ADD ADC SUB SBB	ADDW ADCW SUBW SBBW	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			‡	0	‡	0	0	‡
ANA ORA XRA	ANAW ORAW XRAW	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		‡	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCW SUBNBW GTAW LTAW	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		‡	‡	‡	0	0	‡
ONA OFFA	ONAW OFFAW	ONAX OFFAX	ONI OFFI	ONIW OFFIW		‡	‡	•	0	0	•
NEA EQA	NEAW EQAW	NEAX EQAX	NEI EQI	NEIW EQIW		‡	‡	‡	0	0	‡
INR DCR	INRW DCRW					‡	‡	‡	0	0	•
DAA						‡	0	‡	0	0	‡
RAL, RAR, RCL, RCR SHAL, SHAR, SHCL, SHCR						•	0	•	0	0	‡
RLD, RRD						•	0	•	0	0	•
STC						•	0	•	0	0	1
CLC						•	0	•	0	0	0
			MVI A, byte			•	0	•	1	0	•
			MVI L, byte LXI H, word			•	0	•	0	1	•
					BIT SKC SKNC SKZ SKNZ SKIT SKNIT	•	‡	•	0	0	•
					RETS	•	1	•	0	0	•
All other instructions						•	0	•	0	0	•

‡ Flag affected according to result of operation
1 Flag set
0 Flag reset
• Flag not affected

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

−10 to +70°C, V_{CC} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

AC CHARACTERISTICS

-10 to $+70°C$, $V_{CC} = +5.0V \pm 10\%$

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X1 Input Cycle Time	t_{CYX}	227	1000	ns	
X1 Input Low Level Width	t_{XXL}	106		ns	
X1 Input High Level Width	t_{XXH}	106		ns	
ϕ_{OUT} Cycle Time	$t_{CY\phi}$	454	2000	ns	
ϕ_{OUT} Low Level Width	$t_{\phi\phi L}$	150		ns	
ϕ_{OUT} High Level Width	$t_{\phi\phi H}$	150		ns	
ϕ_{OUT} Rise/Fall Time	t_r, t_f		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → ϕ_{OUT} L.E.	$t_{R\phi}$	100		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	$200_{(T3)}$; $700_{(T4)}$		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → $\overline{WAIT}$ L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from ϕ_{OUT} L.E.)	t_{WTS}	290		ns	
$\overline{WAIT}$ Hold Time (Referenced from ϕ_{OUT} L.E.)	t_{WTH}	0		ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	$t_{CY\phi}$ = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
ϕ_{OUT} L.E. → $\overline{WR}$ L.E.	$t_{\phi W}$	40	125	ns	
Address (PE_{0-15}) → ϕ_{OUT} T.E.	$t_{A\phi}$	100	300	ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	140		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from ϕ_{OUT} L.E.)	t_{HDS1}	200		ns	$t_{CY\phi}$ = 500 ns
	t_{HDS2}	200		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	0		ns	
ϕ_{OUT} L.E. → HLDA	t_{DHA}	110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)

② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

7

AC CHARACTERISTICS (CONT.)

$t_{CY\phi}$ DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
$t_{R\phi}$	(1/5) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
$t_{\phi W}$	(1/4) T	MAX	ns
$t_{A\phi}$	(1/5) T	MIN	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns

Notes: ① N = Number of Wait States

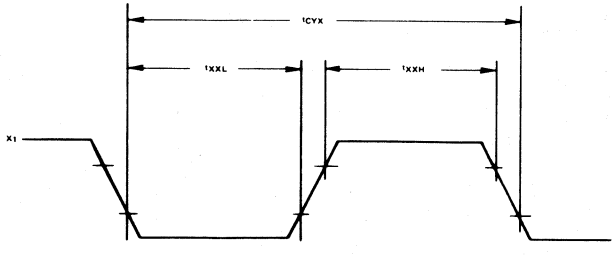
② $T = t_{CY\phi}$

③ Only above parameters are t_{CY_ϕ} dependent

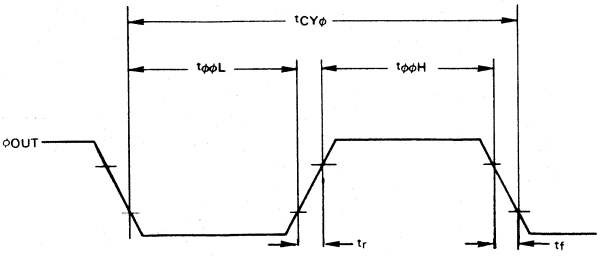
④ When a crystal frequency other than 4 MHz is used (t_{CY_ϕ} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

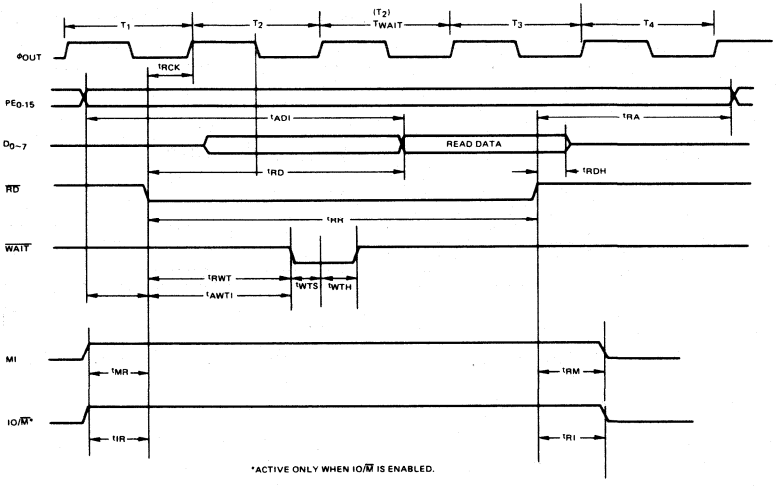
CLOCK TIMING



TIMING WAVEFORMS
(CONT.)

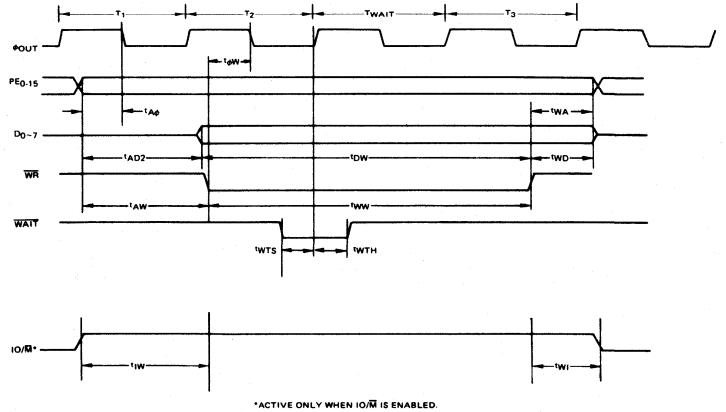


READ OPERATION



*ACTIVE ONLY WHEN IO/$\overline{M}$ IS ENABLED.

WRITE OPERATION



*ACTIVE ONLY WHEN IO/$\overline{M}$ IS ENABLED.

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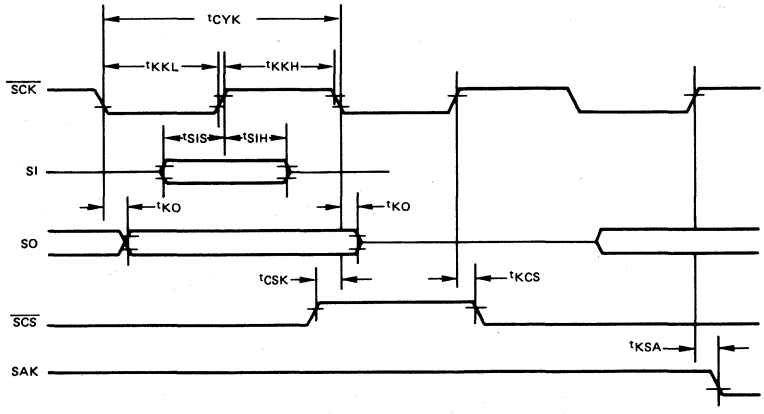
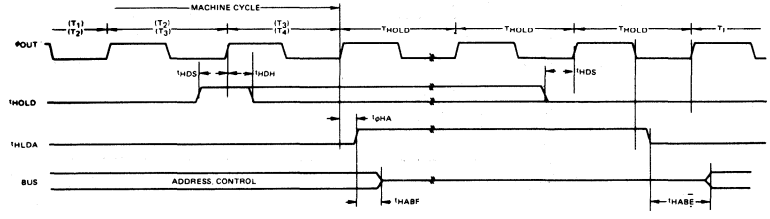
SERIAL I/O OPERATION

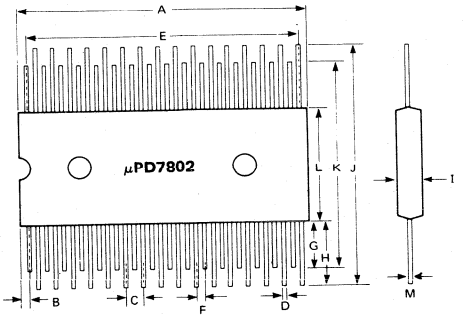


HOLD OPERATION



PACKAGE INFORMATION

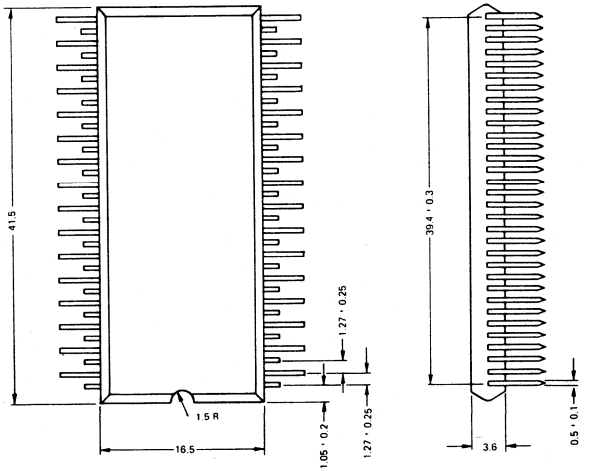
STRAIGHT LEADS



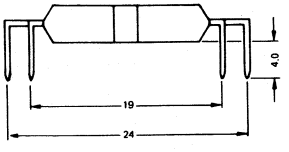
(Plastic)

ITEM	MILLIMETERS	INCHES
A	41.8 MAX	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	39.37	1.55
F	1.27	0.05
G	6.75	0.27
H	9.3	0.37
I	3.6	0.14
J	35.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

BENT LEADS



(Unit: mm)



7802DS-Rev 1-12-81-CAT

μPD78C06
CMOS HIGH END 8-BIT SINGLE CHIP MICROCOMPUTER

Description

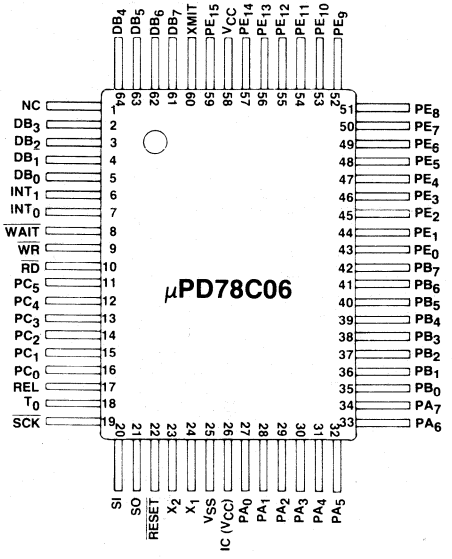
The NEC μPD78C06 is an advanced CMOS 8-bit general purpose single chip microcomputer intended for applications requiring 8-bit microprocessor control and extremely low power consumption; ideally suited for portable, battery-powered/backed-up products. A subset of the μPD7801, the μPD78C06 integrates an 8-bit ALU, 4K ROM, 128 bytes RAM, 46 I/O lines, an 8-bit timer, and a serial I/O port on a single die. Fully compatible with the 8080A bus structure, expanded system operation can easily be implemented using industry standard peripheral and memory components. Total memory space can be increased to 64K bytes.

The μPD78C06 lends itself well to low power, portable applications by featuring two power down modes to further conserve power when the processor is not active. The μPD78C06 is packaged in a 64-pin flat pack. The μPD78C05 is a ROM-less version packaged in a 64-pin QUIL, designed for prototype development and small volume production.

Features

- ☐ CMOS Silicon Gate Technology + 5V supply
- ☐ Complete Single Chip Microcomputer
  - — 8-bit ALU
  - — 4K ROM
  - — 256 Bytes RAM
- ☐ Low Power Consumption
- ☐ 46 I/O Lines
- ☐ Expansion Capabilities
  - — 8080A Bus Compatible
  - — 60K Bytes External Memory Address Range
- ☐ Serial I/O Port
- ☐ 101 Instruction Set
  - — Multiple Address Modes
- ☐ Power Down Modes
  - — Halt Mode
  - — Stop Mode
- ☐ 8-Bit Timer
- ☐ Prioritized Interrupt Structure
  - — 2 External
  - — 1 Internal
- ☐ On Chip Clock Generator
- ☐ 64-Pin Flat Pack

Pin Configuration



Pin Identification

PA_{7-0}, PB_{7-0}, PC_{5-0}, PE_{15-0}	I/O Ports
DB_{7-0}	Data Bus
$\overline{WAIT}$	Wait Request
INT_0, INT_1	Interrupt Request
X_2, X_1	Xtal
$\overline{SCK}$	Serial Clock Input/Output
SI	Serial Input
SO	Serial Output
$\overline{RESET}$	Reset
$\overline{RD}$	Read Strobe
$\overline{WR}$	Write Strobe
ϕout	Clock Output

7

Block Diagram

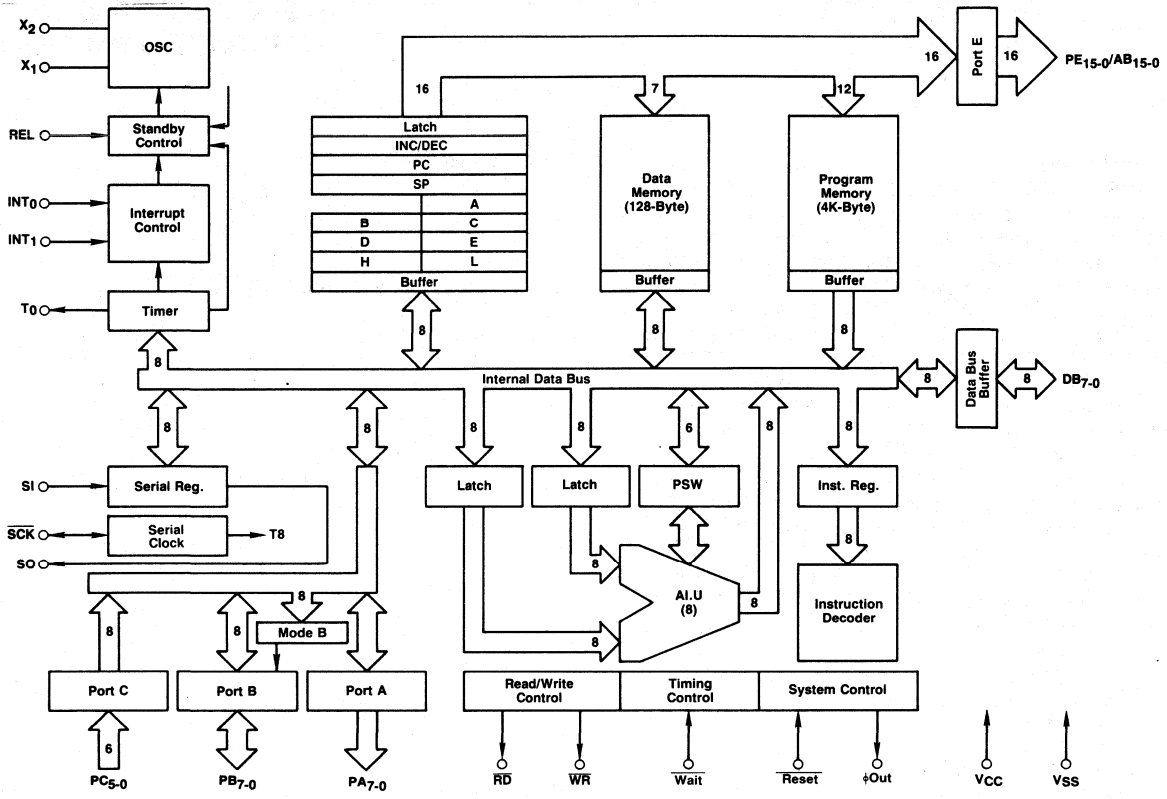


Table 4-1 HALT Mode and STOP Mode

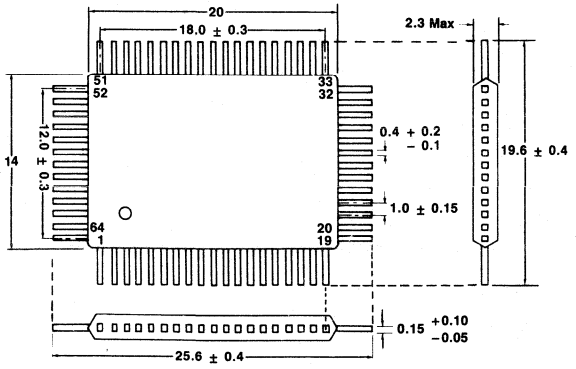
Function	Halt Mode	Stop Mode
Oscillator	Run	Stop
Internal System Clock	Stop	
Timer	Run	
TIMER REG	Hold	Set
UPCOUNTER, PRESCALER 0, 1	Run	Cleared
Serial Interface		Run ①
Serial Clock	Hold	Hold
Interrupt Control Circuit	Run	Stop
Interrupt Enable Flag	Hold	Reset
INT_0, INT_1 Input	Active	Inactive
INTT		—
T_8 (INTFS)		—
MASK Register	Hold	Set
Pending Interrupts (INTFX)		Reset
REL Input	Inactive	Active
$\overline{RESET}$ Input	Active	

Function	Halt Mode	Stop Mode
On-Chip RAM	Hold	Hold
Output Latch in Port A, B, E		
Program Counter (PC)		Cleared
Stack Pointer (SP)	Unknown	
General Registers (A, B, C, D, E, F, L)		
Program Status Word (PSW)	Hold	Reset
Mode B-Register	Hold	
Standby Control Register (SC_0–SC_3)		
Standby Control Register (SC_4)		Set
Timer Mode Register (TMM_{0-1})		Hold
Timer Mode Register (TMM_1)		Set
Serial Mode Register (SM)		Hold
Data Bus (DB_{0-7})	High-Z	High-Z
$\overline{RD}$, $\overline{WR}$ Output	High	High

Note:

① Serial clock counter is running and T_8 is generated; however, there are no effects by it.

Package Dimension
64-Pin Flat
(Unit: mm)



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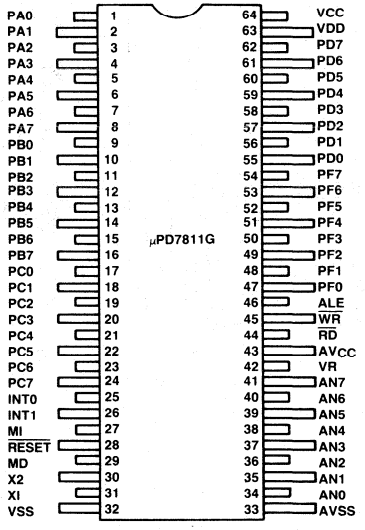
μPD7811G
HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH A/D CONVERTER

Description

The NEC μPD7811G is a high performance single chip microcomputer integrating sophisticated on-chip peripheral functionality normally provided by external components. The device's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make the μPD7811G appropriate in data processing as well as control applications. The device integrates a 16-bit ALU, 4K ROM, 256 Bytes RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART and two zero-cross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.

The μPD7811G is the mask-ROM high volume production device embedded with custom customer program. The μPD7810G is a ROM-less version for prototyping and small volume production. The μPD78PG11E is a piggy-back EPROM version for design development.

Pin Configuration



Features

- ☐ NMOS Silicon Gate Technology Requiring + 5V Supply
- ☐ Complete Single Chip Microcomputer
  - — 16-Bit ALU
  - — 4K ROM
  - — 256 Bytes RAM
- ☐ 44 I/O lines
- ☐ Two Zero-Cross Detect Inputs
- ☐ Expansion Capabilities
  - — 8085A Bus Compatible
  - — 60K Bytes External Memory Address Range
- ☐ 8-Channel, 8-Bit A/D Converter
  - — Auto Scan
  - — Channel Select
- ☐ Full Duplex USART
  - — Synchronous and Asynchronous
- ☐ 153 Instruction Set
  - — 16-Bit Arithmetic, Multiply and Divide
- ☐ 1 μs Instruction Cycle Time
- ☐ Prioritized Interrupt Structure
  - — 2 External
  - — 4 Internal
- ☐ Standby Function
- ☐ On-Chip Clock Generator
- ☐ 64-Quil Package

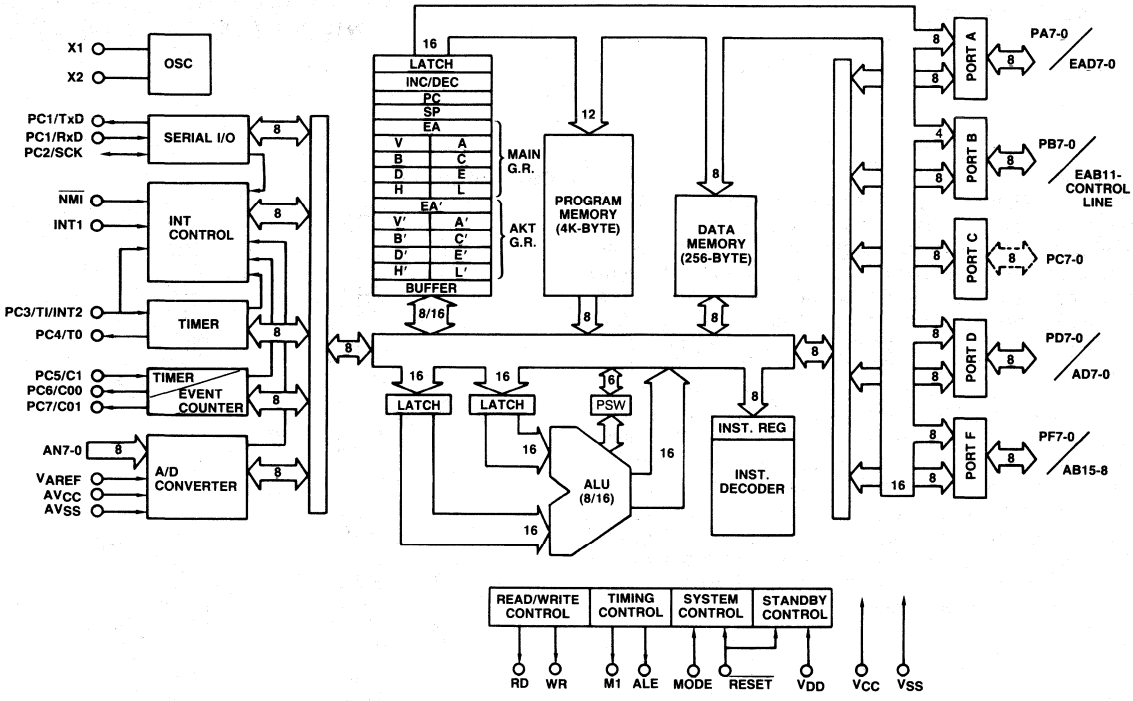
Instruction Set

In addition to the existing instruction set for μPD7801, the following new instructions are incorporated in the μPD7811.

- — 16-Bit Data Transfer
  - 16-Bit Data Transfer Memory and Extended Accumulator
- — 16-Bit Data Arithmetic and Logical Operation
  - 16-Bit Addition and Subtraction
  - 16-Bit Comparison
  - 16-Bit And, Or, Ex-or Operation
- — 16-Bit Data Shift and Rotation
- — Multiply
  - 8-Bit by 8-Bit
  - Less than 8 μs Execution
- — Divide
  - 16-Bit Divided by 8-Bit
  - Less than 14 μs Execution
- — Index Operation
  - Register Pair HL and DE are used as Index Register

7

Block Diagram



Input/Output

8 Analog Input Lines

44 Digital I/O Lines — Five 8-Bit ports (Port A, Port B, Port C, Port D, Port F) and 4 Input Lines (AN_{4-7})

1. Analog Input Lines
   AN_{0-7} are configured as analog input lines for on chip A/D converter.
2. Port Operation
   — Port A, Port B, Port C, Port F
   Each line of these ports can be individually programmed as an input or as an output.
   — Port D
   Port D can be programmed as a byte input or a byte output.
   — AN_{4-7}
   In addition to the analog input lines, AN_{4-7} can be used as digital input lines for falling edge detection.
3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, Timer and Timer/Counter.
4. Memory Expansion
   In addition to the single-chip operation mode μPD7811 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

Memory Expansion	Port Configuration
Non	Port D — I/O Port Port F — I/O Port
256 Bytes	Port D — Multiplexed Address/Data Bus Port F — I/O Port
4K Bytes	Port D — Multiplexed Address/Data Bus Port F0-3 — Address Bus Port F4-7 — I/O Port
16K Bytes	Port D — Multiplexed Address/Data Bus Port F0-5 — Address Bus Port F6, 7 — I/O Port
60K Bytes	Port D — Multiplexed Address/Data Bus Port F — Address Bus

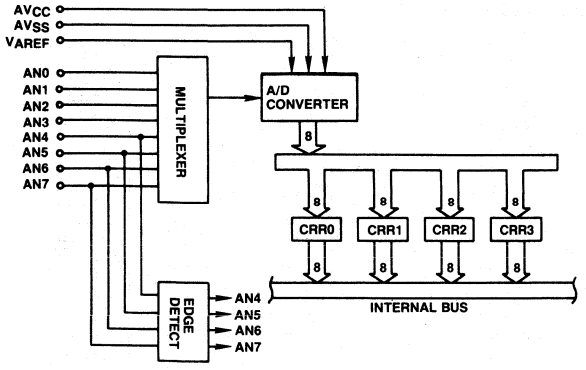
8-Bit A/D Converter

8 Input Channels
4 Conversion Result Registers
2 Powerful Operation Modes
  Auto Scan Mode
  Channel Select Mode
Successive Approximation Technique

Absolute Accuracy	±1.5 LSB (±0.6%)
Conversion Range	0 ∼ 5V
Conversion Time	50 μs

Interrupt Generation

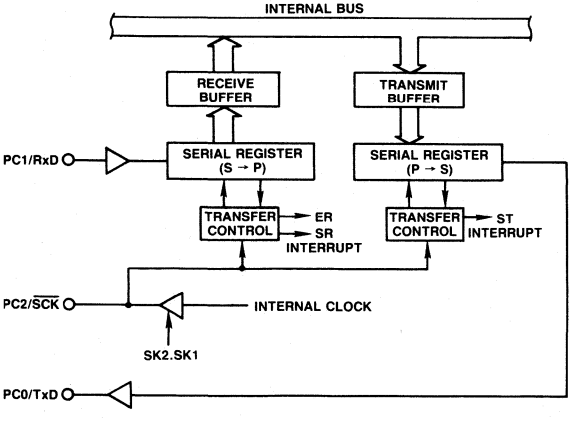
A/D Converter Block Diagram



Universal Serial Interface

- — Full-Duplex, Double Buffering
- — Synchronous Operation Mode
  - Search Mode
  - Receive Mode
- — Asynchronous Operation Mode
  - 7, 8-Bits/Character
  - Start/Stop Bit
  - Even/Odd Parity
  - Programmable Clock Rate x1, x16, x64
- — I/O Expansion Mode (μPD7801 Serial Mode)
- — Programmable Communication Rate
  - 2 μs, 32 μs, Timer 1 and External
- — Interrupt Generation

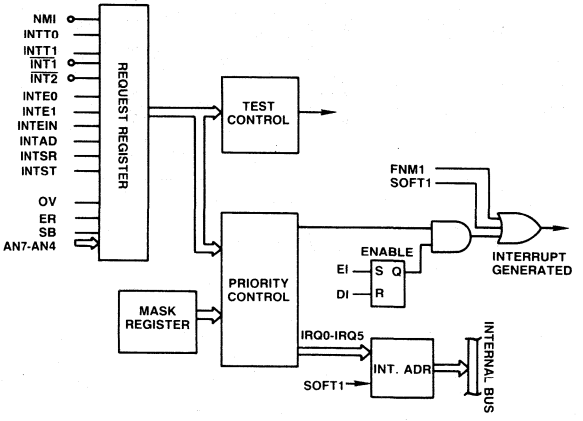
Universal Serial Interface Block Diagram



Interrupt Structure

- — 11 Interrupt Sources
- — 6 Priority Levels
- — Non-maskable Interrupt Capability — NMI
- — Individual Request Mask Capability — Except NMI

Interrupt Request	Interrupt	Type of Interrupt	In/Ext
IRQ0	4	NMI (Non-maskable interrupt)	External
IRQ1	8	INTT0 (Coincidence signal from timer 0) INTT1 (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 (Maskable interrupt) INT2 (Maskable interrupt)	External
IRQ3	24	INTE0 (Coincidence signal from timer/event counter) INTE1 (Coincidence signal from timer/event counter)	Internal
IRQ4	32	INTEIN (Falling signal of C1 and T0 counter) INTAD (A/D converter interrupt)	In/External
IRQ5	40	INTSR (Serial receive interrupt) INST (Serial send interrupt)	Internal



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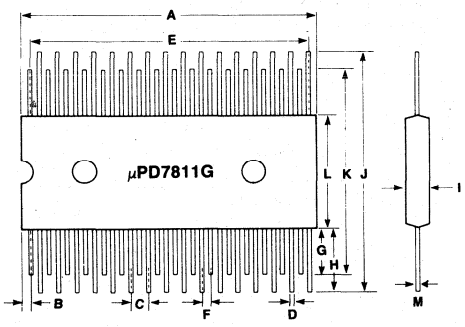
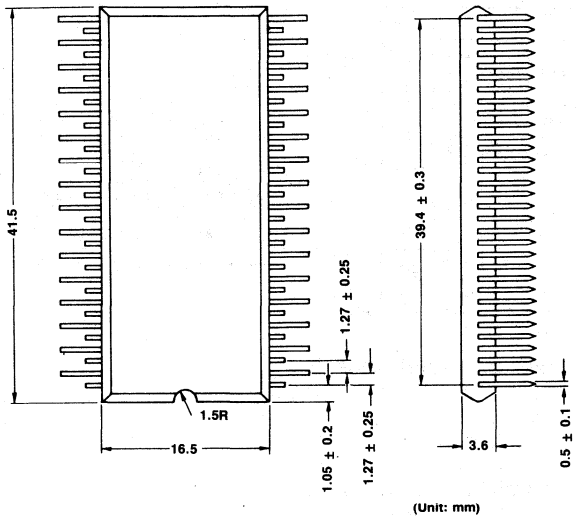
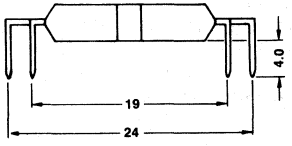
Package Information

Straight Leads



Bent Leads





Plastic

Item	Millimeters	Inches
A	41.8 Max	1.65
B	1.22	0.05
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	39.37	1.55
F	1.27	0.05
G	6.75	0.27
H	9.3	0.37
I	3.6	0.14
J	35.1	1.38
K	30.0	1.18
L	16.5	0.65
M	0.25 ± 0.05	0.01 ± 0.002

SINGLE CHIP 8-BIT MICROCOMPUTER

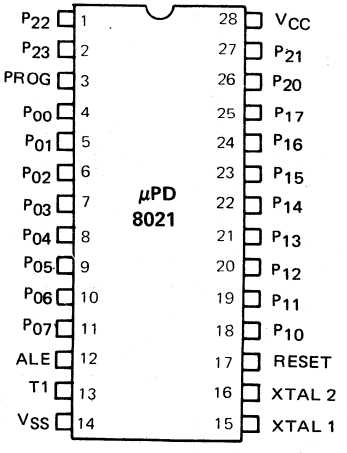
DESCRIPTION

The NEC μPD8021 is a stand alone 8-bit parallel microcomputer incorporating the following features usually found in external peripherals. The μPD8021 contains: 1K x 8 bits of mask ROM program memory, 64 x 8 bits of RAM data memory, 21 I/O lines, an 8-bit interval timer/event counter, and internal clock circuitry.

FEATURES

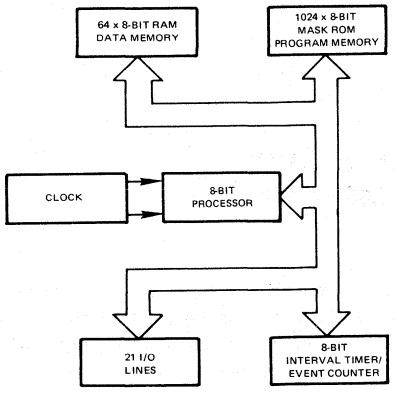
- 8-Bit Processor, ROM, RAM, I/O, Timer/Counter
- Single +5V Supply (+4.5V to +6.5V)
- NMOS Silicon Gate Technology
- 8.38 μs Instruction Cycle Time
- All Instructions 1 or 2 Cycles
- Instructions are Subset of μPD8048/8748/8035
- High Current Drive Capability — 2 I/O Pins
- Clock Generation Using Crystal or Single Inductor
- Zero-Cross Detection Capability
- Expandable I/O Using μ8243's
- Available in 28-Pin Plastic Package

PIN CONFIGURATION



7

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . -65°C to +150°C
(Plastic Package) . . . . . -65°C to +150°C
Voltage on Any Pin . . . . . -0.5 to +7 Volts ①
Power Dissipation. . . . . 1 Watt

Note: ① With Respect to Ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5.5V \pm 1V$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		+ 0.8	V	
Input High Voltage, RESET, T1 (All Except XTAL 1, XTAL 2)	V_{IH}	2.0		V_{CC}	V	$V_{CC} = 5.0V \pm 10\%$
Input High Voltage (XTAL 1, XTAL 2)	V_{IH1}	3.0		V_{CC}	V	$V_{CC} = 5.5V \pm 1V$
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 1.7$ mA
Output Low Voltage (P_{10}, P_{11})	V_{OL1}			2.5	V	$I_{OL} = 7$ mA
Output High Voltage (All Unless Open Drain)	V_{OH}	2.4			V	$I_{OH} = 40\ \mu A$
Output Leakage Current (Open Drain Option – Port 0)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V
V_{CC} Supply Current	I_{CC}		40	75	mA	

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5.5V \pm 1V$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Cycle Time	T_{CY}	8.38		50.0	μs	3.58 MHz XTAL for T_{CY} Min.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1-2, 26-27	P_{20}-P_{23} (Port 2)	P_{20}-P_{23} comprise the 4-bit bi-directional I/O port which is also used as the expander bus for the μPD8243.
3	PROG	PROG is the output strobe pin for the μPD8243.
4-11	P_{00}-P_{07} (Port 0)	One of the two 8-bit quasi bi-directional I/O ports.
12	ALE	Address Latch Enable output (active-high). Occurring once every 30 input clock periods, ALE can be used as an output clock.
13	T1	Testable input using transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction. T1 also provides zero-cross sensing for low-frequency AC input signals.
14	V_{SS}	Processor's ground potential.
15	XTAL 1	One side of frequency source input using resistor, inductor, crystal or external source. (non-TTL compatible V_{IH}).
16	XTAL 2	The other side of frequency source input.
17	RESET	Active high input that initializes the processor and starts the program at location zero.
18-25	P_{10}-P_{17} (Port 1)	The second of two 8-bit quasi bi-directional I/O ports.
28	V_{CC}	+5V power supply input.

FUNCTIONAL DESCRIPTION

The NEC μPD8021 is a single component, 8-bit, parallel microprocessor using N-channel silicon gate MOS technology. The self-contained 1K x 8-bit ROM, 64 x 8-bit RAM, 8-bit timer/counter, and clock circuitry allow the μPD8021 to operate as a single-chip microcomputer in applications ranging from controllers to arithmetic processors.

The instruction set, a subset of the μPD8048/8748/8035, is optimum for high-volume, low cost applications where I/O flexibility and instruction set power are required. The μPD8021 instruction set is comprised mostly of single-byte instructions with no instructions over two bytes.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAG C
DATA MOVES													
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
MOV A, Rr	(A) ← (Rr); r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1	
MOV A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1	
MOV Rr, = data	(Rr) ← data; r = 0 - 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2	
MOV Rr, A	(Rr) ← (A); r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1	
MOV @ Rr, A	((Rr)) ← (A); r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1	
MOV @ Rr, = data	((Rr)) ← data; r = 0 - 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2	
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1	
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1	
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1	
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1	
FLAGS													
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•
INPUT/OUTPUT													
ANLD Pp, A	(P_p) ← (P_p) AND (A 0 - 3) p = 4 - 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1	
IN A, P_p	(A) ← (P_p); p = 1 - 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1	
MOVD A, P_p	(A 0 - 3) ← (P_p); p = 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1	
MOVD P_p, A	(P_p) ← A 0 - 3; p = 4 - 7	Move contents of Accumulator to designated port (4 - 7).	0	0	1	1	1	1	p	p	1	1	
ORLD P_p, A	(P_p) ← (P_p) OR (A 0 - 3) p = 4 - 7	Logical or contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1	
OUTL P_p, A	(P_p) ← (A); p = 1 - 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1	
REGISTERS													
INC Rr	(Rr) ← (Rr) + 1; r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1	
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1	
SUBROUTINE													
CALL addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
RET	(SP) ← (SP) - 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1	
TIMER/COUNTER													
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1	
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1	
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1	
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1	
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1	
MISCELLANEOUS													
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1	

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

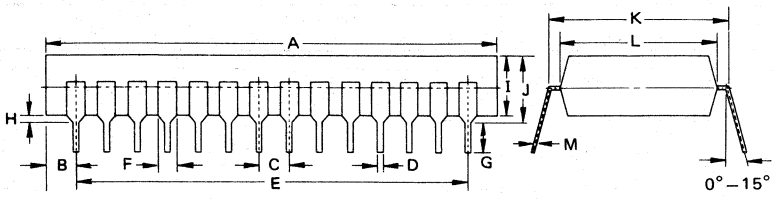
Symbol Definitions

SYMBOL	DESCRIPTION
A	The Accumulator
addr	Program Memory Address (12 bits)
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
P	"In-Page" Operation Designator
P_p	Port Designator (p = 1, 2 or 4 - 7)
Rr	Register Designator (r = 0, 1 or 0 - 7)

SYMBOL	DESCRIPTION
T	Timer
• T_1	Testable Flag 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAG C
ACCUMULATOR													
ADD A, = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•
Add A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•
ADDC A, = data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1	
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1	
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1	
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1	
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•
DEC A	(A) ← (A) – 1	DECREMENT by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1	
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1	
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1	
ORL A @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1	
RL A	(AN + 1)← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1	
RLC A	(AN + 1) ← (AN); N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1	
RRC A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•
SWAP A	(A_{4-7}) $\rightleftarrows$ (A_0 – 3)	Swap the 24-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1	
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1	
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1	
BRANCH													
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0 (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2	
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1	
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JNZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	

PACKAGE OUTLINE
μPD8021C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX	1.496 MAX
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

SINGLE CHIP 8-BIT MICROCOMPUTER WITH ON-CHIP A/D CONVERTER

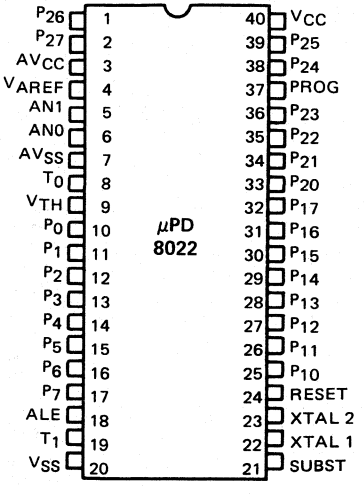
DESCRIPTION

The NEC μPD8022 is designed for low cost, high volume applications requiring large ROM space, analog to digital conversion capability, a capacitive touchpanel keyboard interface and/or a power line time base. The μPD8022 satisfies these requirements by integrating on one chip, an 8-bit μPD8021 type processor with 2K of ROM, a 2 channel 8-bit A/D converter, a high impedance comparator input port, and a zero crossing detector.

FEATURES

- 8-Bit Processor, ROM, RAM, I/O and Clock Generator
- Single +5V Supply (4.5V to 6.5V)
- NMOS Silicon Gate Technology
- 2K x 8 ROM, 64 x 8 RAM, 26 I/O Lines
- On Chip 8-Bit A/D Converter with 2 Input Channels
- 8.3 μs Instruction Cycle Timer
- Instructions are a Subset of μPD8048; Superset of μPD8021
- Internal Timer/Event Counter
- External and Timer/Counter Interrupts
- On-Chip Zero-Cross Detector
- High Impedance Comparator Port with Variable Threshold
- Clock Generator Using a Crystal or Single Inductor
- High Current Drive Capability on 2 I/O Pins
- Expandable I/O Utilizing the μPD8243
- Available in 40-Pin Plastic Dual-In-Line Package

PIN CONFIGURATION



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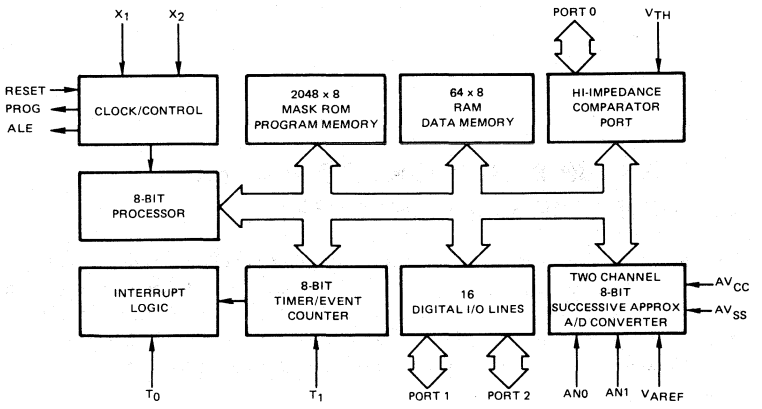
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Plastic Package)	-65°C to +150°C
Voltage on Any Pin	-0.5 to +7 Volts①
Power Dissipation	1 Watt

Note: ① With Respect to Ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage	V_{IL}	-0.5		0.8	V	V_{TH} Floating
Input Low Voltage (Port 0)	V_{IL1}	-0.5		V_{TH}-0.1	V	
Input High Voltage (All except XTAL 1, RESET)	V_{IH}	2.0		V_{CC}	V	V_{CC} = 5.0V ± 10% V_{TH} Floating
Input High Voltage (All except XTAL 1, RESET)	V_{IH1}	3.0		V_{CC}	V	V_{CC} = 5.5V ± 1V V_{TH} Floating
Input High Voltage (Port 0)	V_{IH2}	V_{TH}+0.1		V_{CC}	V	
Input High Voltage (RESET, XTAL 1)	V_{IH3}	3.0		V_{CC}	V	V_{CC} = 5.0V ± 10%
Port 0 Threshold Voltage	V_{TH}	0		0.4 V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.7 mA
Output Low Voltage (P_{10}, P_{11})	V_{OL1}			2.5	V	I_{OL} = 7 mA
Output High Voltage (All unless open drain option for Port 0)	V_{OH}	2.4			V	I_{OH} = 50 μA
Input Current (T1)	I_{L1}			±200	μA	$V_{CC} \geqslant V_{IN} \geqslant V_{SS}$ + 0.45V
Output Leakage Current (Open drain option for Port 0)	I_{LO}			±10	μA	$V_{CC} \geqslant V_{IN} \geqslant V_{SS}$ + 0.45V
V_{CC} Supply Current	I_{CC}		50	100	mA	

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
8	T_0	Active low interrupt input if enabled. Also testable using the conditional jump instructions JTO and JNTO.
19	T_1	Zero-cross detector input. After executing a STRT CNT instruction this becomes the event counter input. Also testable using the conditional jump instructions JT1 and JNT1. Optional ROM mask pull-up resistor available.
6	AN0	Analog input to the A/D converter after execution of the SEL AN0 instruction.
5	AN1	Analog input to the A/D converter after execution of the SEL AN1 instruction.
22	XTAL 1	Input for internal oscillator connected to one side of a crystal or inductor. Serves as an external frequency input also (Non-TTL compatible V_{IH}).
23	XTAL 2	Input for internal oscillator connected to the other side of a crystal or inductor. This pin is not used when employing an external frequency source.
37	PROG	Strobe output for the μPD8243 I/O expander.
18	ALE	Active high address latch enable output occurring once every instruction cycle. Can be used as an output clock.
24	RESET	Active high input that initializes the processor to a defined state and starts the program at memory location zero.
40	V_{CC}	+5V power supply.
3	AV_{CC}	+5V A/D converter power supply.
20	V_{SS}	Power supply ground potential.
7	AV_{SS}	A/D converter power supply ground potential. Sets conversion range lower limit.
4	VA_{REF}	Reference voltage for A/D converter. Sets conversion range upper limit.
9	V_{TH}	Port 0 comparator threshold reference input.
21	SUBST (NC)	Substrate connection used with bypass capacitor to V_{SS} for substrate voltage stabilization and improvement of A/D accuracy.
10-17	P_{00}-P_{07}	Port 0. 8-bit open drain I/O port with comparator inputs. The reference threshold is set via V_{TH}. Optional ROM mask pull-up resistors available.
25-32	P_{10}-P_{17}	Port 1. 8-bit quasi-bidirectional port. TTL compatible.
1-2 33-36 38-39	P_{20}-P_{27}	Port 2. 8-bit quasi-bidirectional port. TTL compatible. P_{20}-P_{23} also function as an I/O expander port for the μPD8243.

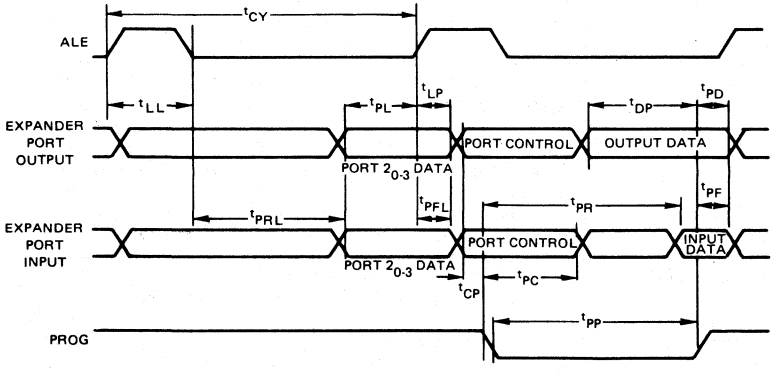
T_a = 0°C to 70°C, V_{CC} = 5.5V ± 1V, V_{SS} = 0V

AC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Cycle Time	t_{CY}	8.38		50.0	μs	3.58 MHz XTAL for t_{CY} min.
Zero-Cross Detection Input (T1)	V_{T1}	1		3	VAC_{pp}	AC coupled
Zero-Cross Accuracy	A_{ZX}			±135	mV	60 Hz Sine Wave
Zero-Cross Detection Input Frequency (T1)	F_{ZX}	0.05		1	kHz	
Port Control Setup Before Falling Edge of PROG	t_{CP}	0.5			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Port Control Hold After Falling Edge of PROG	t_{PC}	0.8			μs	t_{CY} = 8.38 μs, C_L = 80 pF
PROG to Time P2 Input Must be Valid	t_{PR}			1.0	μs	t_{CY} = 8.38 μs, C_L = 80 pF
Output Data Setup Time	t_{PP}	7.0			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Output Data Hold Time	t_{PD}	8.3			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Input Data Hold Time	t_{PF}	0		150	ns	t_{CY} = 8.38 μs, C_L = 80 pF
PROG Pulse Width	t_{PP}	8.3			μs	t_{CY} = 8.38 μs, C_L = 80 pF
ALE to Time P2 Input Must be Valid	t_{PRL}			3.6	μs	t_{CY} = 8.38 μs, C_L = 80 pF
Output Data Setup Time	t_{PL}	0.8			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Output Data Hold Time	t_{LP}	1.6			μs	t_{CY} = 8.38 μs, C_L = 80 pF
Input Data Hold Time	t_{PFL}	0			μs	t_{CY} = 8.38 μs, C_L = 80 pF
ALE Pulse Width	t_{LL}	3.9		23.0	μs	t_{CY} = 8.38 μs for min.

PORT 2 TIMING

TIMING WAVEFORM



A/D CONVERTER CHARACTERISTICS

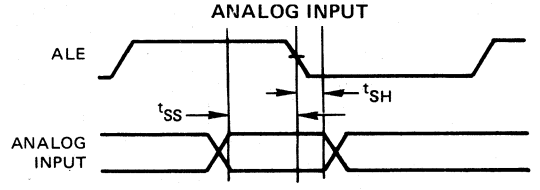
$T_a = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$, $AV_{CC} = 5.5V \pm 1V$, $AV_{SS} = 0V$
$AV_{CC}/2 \leq V_{AREF} \leq AV_{CC}$

PARAMETER	SYMBOL	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
Resolution		8			BITS	
Absolute Accuracy				②	LSB	
Sample Setup Before Falling Edge of ALE	t_{SS}		0.20		t_{CY}	①
Sample Hold After Falling Edge of ALE	t_{SH}		0.10		t_{CY}	①
Input Capacitance (AN0, AN1)	C_{AD}		1		pF	
Conversion Time	t_{CNV}	4		4	t_{CY}	
Conversion Range		AV_{SS}		V_{AREF}	V	
Reference Voltage	V_{AREF}	$AV_{CC}/2$		AV_{CC}	V	

Note: ① The analog signal on AN0 and AN1 must remain constant during the sample time $t_{SS} + t_{SH}$.

② .8% FSR ± 1/2 LSB

TIMING WAVEFORM



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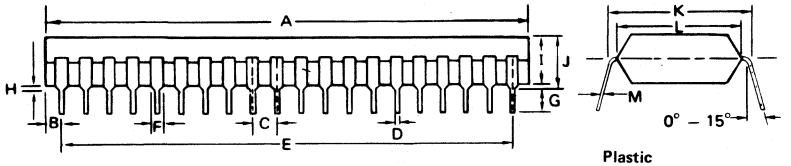
INSTRUCTION SET

The instruction set of the μPD8022 is a subset of the μPD8048 instruction set except for three instructions, SEL AN0, SEL AN1, and RAD, which are unique to the μPD8022. The μPD8022 instruction set is also a superset of the μPD8021, meaning that the μPD8022 will execute ALL of the μPD8021 instructions PLUS some additional instructions which are listed below. For a summary of the μPD8021 instruction set, please refer to that section. Symbols used below are defined in the same manner as in that section. Also note that the instructions listed below do not affect any status flags.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								CYCLES	BYTES
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
JTO addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if T0 is high	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNTO addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if T0 is low	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
RAD	(A) ← (CRR)	Move to A the contents of the A/D conversion result register (CRR)	1	0	0	0	0	0	0	0	2	1
SEL AN0		Select AN0 as the input for the A/D converter	1	0	0	0	0	1	0	1	1	1
SEL AN1		Select AN1 as the input for the A/D converter	1	0	0	1	0	1	0	1	1	1
EN I		Enable the external interrupt input T0	0	0	0	0	0	1	0	1	1	1
DIS I		Disable the external interrupt input T0	0	0	0	1	0	1	0	1	1	1
EN TCNTI		Enable internal timer/ counter interrupt	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disable internal timer/ counter interrupt	0	0	1	1	0	1	0	1	1	1
RETI	(SP) ← (SP) − 1 (PC) ← ((SP))	Return from interrupt and re-enable interrupt input logic	1	0	0	1	0	0	1	1	2	1

PACKAGE OUTLINE μPD8022C



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

UNIVERSAL PROGRAMMABLE PERIPHERAL INTERFACE — 8-BIT MICROCOMPUTER

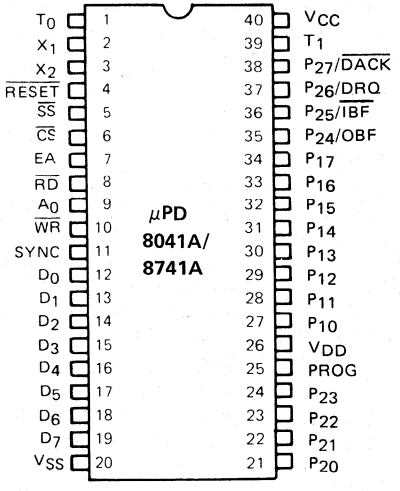
DESCRIPTION

The μPD8041A/8741A is a programmable peripheral interface intended for use in a wide range of microprocessor systems. Functioning as a totally self-sufficient controller, the μPD8041A/8741A contains an 8-bit CPU, 1K x 8 program memory, 64 x 8 data memory, I/O lines, counter/timer, and clock generator in a 40-pin DIP. The bus structure, data registers, and status register enable easy interface to 8048, 8080A or 8085A based systems. The μPD8041A's program memory is factory mask programmed, while the μPD8741A's program memory is UV EPROM to enable user flexibility.

FEATURES

- Fully Compatible with 8048, 8080A, 8085A and 8086 Bus Structure
- 8-Bit CPU with 1K x 8 ROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 I/O Lines
- 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface
- Interchangeable EPROM and ROM Versions
- Interrupt, DMA or Polled Operation
- Expandable I/O
- 40-Pin Plastic or Ceramic Dip
- Single +5V Supply

PIN CONFIGURATION



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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1,39	T_0, T_1	Testable input pins using conditional transfer functions JT0, JNT0, JT1, JNT1. T_1 can be made the counter/timer input using the STRT CNT instruction. The PROM programming and verification on the μPD8741A uses T_0.
2	X_1	One side of the crystal input for external oscillator or frequency source.
3	X_2	The other side of the crystal input.
4	$\overline{RESET}$	Active-low input for processor initialization. $\overline{RESET}$ is also used for PROM programming, verification, and power down.
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with SYNC output allows the μPD8741A to "single-step" through each instruction in program memory.
6	$\overline{CS}$	Chip Select input (active-low). $\overline{CS}$ is used to select the appropriate μPD8041A/8741A on a common data bus.
7	EA	External Access input (active-high). A logic "1" at this input commands the μPD8041A/8741A to perform all program memory fetches from external memory.
8	$\overline{RD}$	Read strobe input (active-low). $\overline{RD}$ will pulse low when the master processor reads data and status words from the DATA BUS BUFFER or Status Register.
9	A_0	Address input which the master processor uses to indicate if a byte transfer is a command or data.
10	$\overline{WR}$	Write strobe input (active-low). $\overline{WR}$ will pulse low when the master processor writes data or status words to the DATA BUS BUFFER or Status Register.
11	SYNC	The SYNC output pulses once for each μPD8041A/8741A instruction cycle. It can function as a strobe for external circuitry. SYNC can also be used together with $\overline{SS}$ to "single-step" through each instruction in program memory.
12-19	D_0-D_7 BUS	The 8-bit, bi-directional, tri-state DATA BUS BUFFER lines by which the μPD8041A/8741A interfaces to the 8-bit master system data bus.
20	V_{SS}	Processor's ground potential.
21-24, 35-38	P_{20}-P_{27}	PORT 2 is the second of two 8-bit, quasi-bi-directional I/O ports. P_{20}-P_{23} contain the four most significant bits of the program counter during external memory fetches. P_{20}-P_{23} also serve as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER. P_{24}-P_{27} can be used as port lines or can provide Interrupt Request (IBF and OBF) and DMA handshake lines (DRG and DACK).
25	PROG	Program Pulse. PROG is used in programming the μPD8741A. It is also used as an output strobe for the μPD8243.
26	V_{DD}	V_{DD} is the programming supply voltage for programming the μPD8741A. It is +5V for normal operation of the μPD8041A/8741A. V_{DD} is also the Low Power Standby input for the ROM version.
27-34	P_{10}-P_{17}	PORT 1 is the first of two 8-bit quasi-bi-directional I/O ports.
40	V_{CC}	Primary power supply. V_{CC} must be +5V for programming and operation of the μPD8741A and for the operation of the μPD8041A.

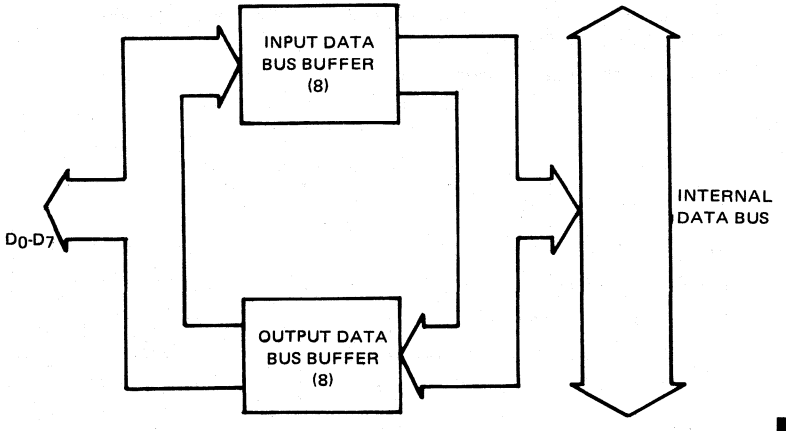
FUNCTIONAL DESCRIPTION

The μPD8041A/8741A is a programmable peripheral controller intended for use in master/slave configurations with 8048, 8080A, 8085A, 8086 – as well as most other 8-bit and 16-bit microprocessors. The μPD8041A/8741A functions as a totally self-sufficient controller with its own program and data memory to effectively unburden the master CPU from I/O handling and peripheral control functions. The μPD8041A/8741A is an intelligent peripheral device which connects directly to the master processor bus to perform control tasks which off load main system processing and more efficiently distribute processing functions.

μPD8041A/8741A FUNCTIONAL ENHANCEMENTS

The μPD8041A/8741A features several functional enhancements to the earlier μPD8041 part. These enhancements enable easier master/slave interface and increased functionality.

1. Two Data Bus Buffers. Separate Input and Output data bus buffers have been provided to enable smoother data flow to and from master processors.

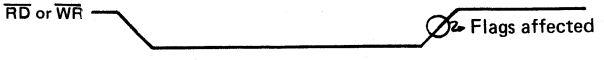


2. 8-Bit Status Register. Four user-definable status bits, ST_4-ST_7, have been added to the status register. ST_4-ST_7 bits are defined with the MOV STS, A instruction which moves accumulator bits 4-7 to bits 4-7 of the status register. ST_0-ST_3 bits are not affected.

ST_7	ST_6	ST_5	ST_4	F_1	F_0	IBF	OBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MOV STS, A Instruction OP Code 90H

3. $\overline{RD}$ and $\overline{WR}$ inputs are edge-sensitive. Status bits IBF, OBF, F1 and INT are affected on the trailing edge at $\overline{RD}$ or $\overline{WR}$.



μPD8041A/8741A
FUNCTIONAL
ENHANCEMENTS (CONT.)

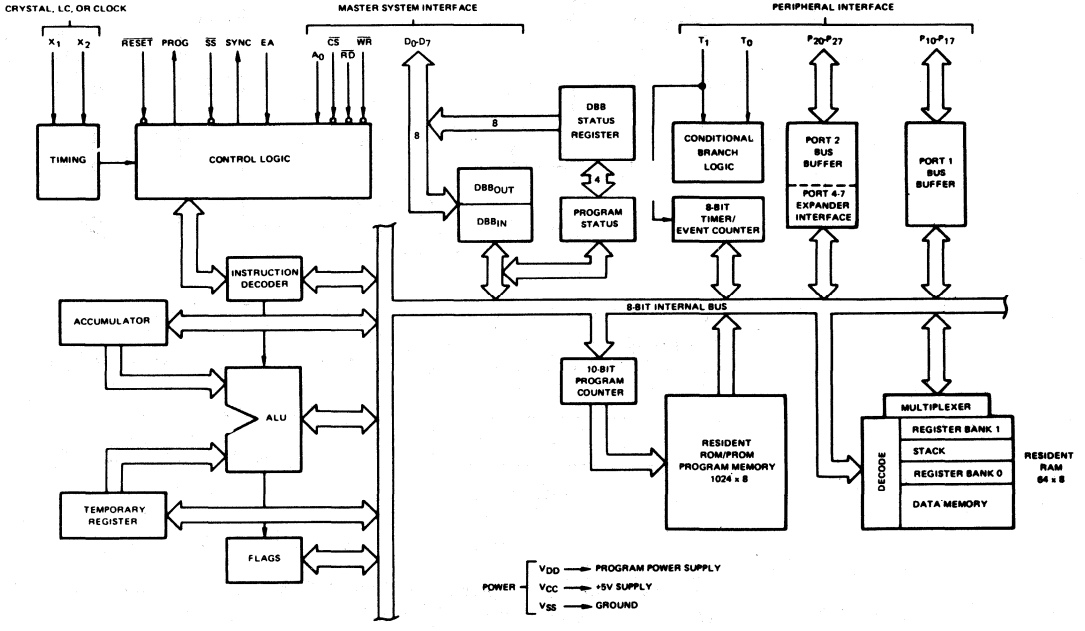
4. P_{24} and P_{25} can be used as either port lines or Buffer Status Flag pins. This feature allows the user to make OBF and IBF status available externally to interrupt the master processor. Upon execution of the EN Flags instruction, P_{24} becomes the OBF pin. When a "1" is written to P_{24}, the OBF pin is enabled and the status of OFB is output. A "0" written to P_{24} disables the OBF pin and the pin remains low. This pin indicates valid data is available from the μPD8041A/8741A. EN Flags instruction execution also enables P_{25} indicate that the μPD8041A/8741A is ready to accept data. A "1" written to P_{25} enables the IBF pin and the status of IBF is available on P25. A "0" written to P_{25} disables the IBF pin.

   EN Flags Instruction Op code – F5H.

5. P_{26} and P_{27} can be used as either port lines or DMA handshake lines to allow DMA interface. The EN DMA instruction enables P_{26} and P_{27} to be used as DRQ (DMA Request) and $\overline{DACK}$ (DMA acknowledge) respectively. When a "1" is written to P_{26}, DRQ is activated and a DMA request is issued. Deactivation of DRQ is accomplished by the execution of the EN DMA instruction, $\overline{DACK}$ anded with $\overline{RD}$, or $\overline{DACK}$ anded with $\overline{WR}$. When EM DMA has been executed, P_{27} ($\overline{DACK}$) functions as a chip select input for the Data Bus Buffer registers during DMA transfers.

   EN DMA Instruction Op Code – E5H.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . −65°C to +150°C
Storage Temperature (Plastic Package) . . . . . −65°C to +150°C
Voltage on Any Pin . . . . . −0.5 to +7 Volts ①
Power Dissipation . . . . . 1.5 Watt

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: ① With respect to ground.

DC CHARACTERISTICS

T_a = 0°C to +70°C; $V_{DD} = V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All except X_1 and X_2)	V_{IL}	−0.5		+0.8	V	
Input Low Voltage (X_1 and X_2, $\overline{RESET}$)	V_{IL1}	−0.5		0.6	V	
Input High Voltage (All except X_1, X_2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (X_1, X_2, $\overline{RESET}$)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (D_0-D_7, SYNC)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All other outputs except PROG)	V_{OL1}			0.45	V	I_{OL} = 1.0 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 1.0 mA
Output High Voltage (D_0-D_7)	V_{OH}	2.4			V	I_{OH} = −400 μA
Output High Voltage (All other outputs)	V_{OH1}	2.4			V	I_{OH} = −50 μA
Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, EA, A_0)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (D_0-D_7; High Z State)	I_{OL}			±10	μA	$V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$
V_{DD} Supply Current	I_{DD}			15	mA	
Total Supply Current	$I_{CC} + I_{DD}$			125	mA	
Low Input Source Current (P_{10}-P_{17}; P_{20}-P_{27})	I_{LI}			0.5	mA	V_{IL} = 0.8V
Low Input Source Current (SS; $\overline{RESET}$)	I_{LI1}			0.2	mA	V_{IL} = 0.8V

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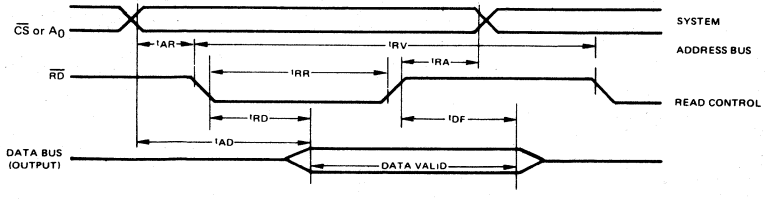
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{DD} = V_{CC} = +5V ± 10%; V_{SS} = 0V

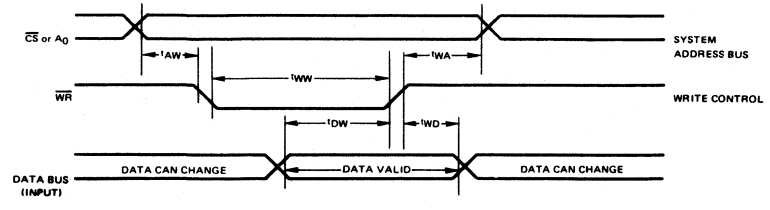
PARAMETER	SYMBOL	LIMITS μPD8041A MIN	LIMITS μPD8041A MAX	LIMITS μPD8741A MIN	LIMITS μPD8741A MAX	UNITS	TEST CONDITIONS
DBB READ							
$\overline{CS}$, A_0 Setup to $\overline{RD}$ ↓	t_{AR}	0		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{RD}$ ↑	t_{RA}	0		30		ns	
$\overline{RD}$ Pulse Width	t_{RR}	250		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		225		370	ns	C_L = 150 pF
$\overline{RD}$ ↓ to Data Out Delay	t_{RD}		225		200	ns	C_L = 150 pF
$\overline{RD}$ ↑ to Data Float Delay	t_{DF}		100		140	ns	
Cycle Time	t_{CY}	2.5	15	2.5	15	μs	6 MHz Crystal
DBB WRITE							
$\overline{CS}$, A_0 Setup to $\overline{WR}$ ↓	t_{AW}	0		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{WR}$ ↑	t_{WA}	0		30		ns	
$\overline{WR}$ Pulse Width	t_{WW}	250		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
Data Setup to $\overline{WR}$ ↑	t_{DW}	150		250		ns	
Data Hold after $\overline{WR}$ ↑	t_{WD}	0		30		ns	

TIMING WAVEFORMS

READ OPERATION – DATA BUS BUFFER REGISTER



WRITE OPERATION – DATA BUS BUFFER REGISTER



INSTRUCTION SET

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	ΦBF	ST_{4-7}
ACCUMULATOR																			
ADD A, # data	ADD A = data	Add Immediate the specified Data to the Accumulator.	0	0	0	0	0	0	1	1	2	2	•						
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•						
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•						
ADDC A, # data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0	0	0	1	0	0	1	1	2	2	•						
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator	0	1	1	1	1	r	r	r	1	1	•						
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•						
ANL A, # data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0	1	0	1	0	0	1	1	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1							
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1							
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1							
CLR A	(A) ← 0	CLEAR the contents of the Accumulator	0	0	1	0	0	1	1	1	1	1							
DA A		DECIMAL ADJUST the contents of the Accumulator	0	1	0	1	0	1	1	1	1	1	•						
DEC A	(A) ← (A) - 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1							
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1							
ORL A, # data	(A) ← (A) OR data	Logical OR or specified immediate data with Accumulator.	0	1	0	0	0	0	1	1	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1							
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1							
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 - 6	Rotate Accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1							
RLC A	(AN + 1) ← (AN), N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•						
RR A	(AN) ← (AN + 1), N = 0 - 6 (A_7) ← (A_0)	Rotate Accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1							
RRC A	(AN) ← (AN + 1), N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•						
SWAP A	(A_{4-7}) ← $(A_0 - 3)$	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1							
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1	1	0	1	0	0	1	1	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1							
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1							
BRANCH																			
DJNZ Rr, addr	(Rr) ← (Rr) - 1, r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents	1	1	1	0	1	r	r	r	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JBb addr	(PC 0 - 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2	b_1	b_0	1	0	0	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1	1	1	1	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JF0 addr	(PC 0 - 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1	0	1	1	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JF1 addr	(PC 0 - 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0	1	1	1	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JMP addr	(PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10}	a_9	a_8	0	0	1	0	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JMPP @ A	(PC 0 - 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1							
JNC addr	(PC 0 - 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1	1	1	0	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JNIBF addr	(PC 0 - 7) ← addr if IBF = (PC) ← (PC) + 2 if IBF = 1	Jump to specified address if input buffer full flag is low.	1	1	0	1	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JOBF	(PC 0 - 7) ← addr if OBF = 1 (PC) ← (PC) + 2 if OBF = 0	Jump to specified address if output buffer full flag is set.	1	0	0	0	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									

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INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION		INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF	ST_{4-7}
BRANCH (CONT.)																			
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T 1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
CONTROL																			
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1							
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1							
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1							
SEL RB1	(BS) ← 1	Select Bank 0 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1							
EN DMA		Enable DMA Handshake.	1	1	1	1	0	1	0	1	1	1							
EN FLAGS		Enable Interrupt to Master Device.	1	1	1	0	0	1	0	1	1	1							
DATA MOVES																			
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
MOV A, Rr	(A) ← (Rr); r = 0 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1							
MOV A, @ Rr	(A) ← ((Rr)), r = 0 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1							
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1							
MOV Rr, = data	(Rr) ← data, r = 0 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2							
MOV Rr, A	(Rr) ← (A), r = 0 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1							
MOV @ Rr, A	((Rr)) ← (A), r = 0 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1							
MOV @ Rr, = data	((Rr)) ← data; r = 0 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2							
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1							
MOVP A, @ A	(PC 0 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1							
MOVP3 A, @ A	(PC 0 - 7) ← (A) (PC 8 - 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1							
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1							
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1							
XCHD A, @ Rr	(A 0 - 3) ⇆ ((Rr)) 0 - 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1							
FLAGS																			
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•						
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•				
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1.	1	0	1	1	0	1	0	1	1	1				•			
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•						
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•				
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•			
MOV STS, A	ST_4-ST_7 ← A_4-A_7	Move high order 4 bits of Accumulator into status register bits 4-7.	1	0	0	1	0	0	0	0	1	1							•

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF	ST_{4-7}
INPUT/OUTPUT																			
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 2	Logical and Immediate specified data with designated port (1 or 2).	1	0	0	1	1	0	p	p	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 3) p = 4 7	**Logical and contents of Accumulator with designated port (4 – 7).**	1	0	0	1	1	1	p	p	2	1							
IN A, Pp	(A) ← (Pp); p = 1 2	Input data from designated port (1 or 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1							
IN A, DBB	(A) ← (DBB)	Input strobed DBB data into Accumulator and clear IBF.	0	0	1	0	0	0	1	0	1	1					•		
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 - 7 (A 4 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1							
MOVD Pp, A	(Pp) ← A 0 3; p = 4 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1							
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 3) p = 4 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1							
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 2	Logical or Immediate specified data with designated port (1 or 2).	1	0	0	0	1	0	p	p	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
OUT DBB, A	(DBB) (A)	**Output contents of Accumulator onto DBB and set OBF.**	0	0	0	0	0	0	1	0	1	1						•	
OUTL Pp, A	(Pp) - (A); p - 1 2	Output contents of Accumulator to designated port (1 or 2).	0	0	1	1	1	0	p	p	1	1							
REGISTERS																			
DEC Rr (Rr)	(Rr) ← (Rr) 1; r = 0 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1							
INC Rr	(Rr) ← (Rr) +1; r = 0 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1							
INC @ Rr	((Rr)) - ((Rr)) + 1, r = 0 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1							
SUBROUTINE																			
CALL addr	((SP)) - (PC), (PSW 4 7) (SP) - (SP) + 1 (PC 8 10) - addr 8 10 (PC 0 - 7) ← addr 0 7 (PC 11) - DBF	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
RET	(SP) - (SP) - 1 (PC) - ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1							
RETR	(SP) - (SP) 1 (PC) ← ((SP)) (PSW 4 7) - ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1							
TIMER/COUNTER																			
EN TCNTI		Enable Internal Interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1							
DIS TCNTI		Disable Internal Interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1							
MOV A, T	(A) - (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1							
MOV T, A	(T) - (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1							
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1							
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1							
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1							
MISCELLANEOUS																			
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1							

Notes
① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
IBF	Input Buffer Full Flag

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By
OBF	Output Buffer Full
DBB	Data Bus Buffer

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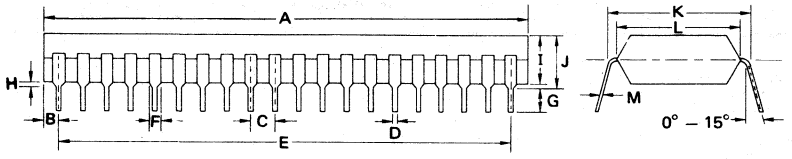
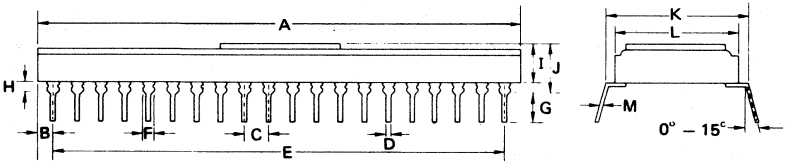


PACKAGE OUTLINE
μPD8041AC

Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8041AD
μPD8741AD

Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

μPD8048 FAMILY OF SINGLE CHIP 8-BIT MICROCOMPUTERS

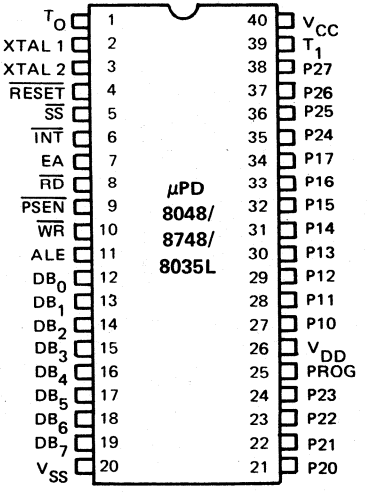
DESCRIPTION

The μPD8048 family of single chip 8-bit microcomputers is comprised of the μPD8048, μPD8748 and μPD8035L. The processors in this family differ only in their internal program memory options: The μPD8048 with 1K x 8 bytes of mask ROM, the μPD8748 with 1K x 8 bytes of UV erasable EPROM and the μPD8035L with external memory.

FEATURES

- Fully Compatible With Industry Standard 8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 2.5 μs Cycle Time. All Instruction 1 or 2 Bytes
- Interval Timer/Event Counter
- 64 x 8 Byte RAM Data Memory
- Single Level Interrupt
- 96 Instructions: 70% Single Byte
- 27 I/O Lines
- Internal Clock Generator
- 8 Level Stack
- Compatible With 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40 Pin Packages

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The NEC μPD8048, μPD8748 and μPD8035L are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8048/8748/8035L efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8048/8748/8035L instruction set is comprised of 1 and 2 byte instructions with over 70% single-byte and requiring only 1 or 2 cycles per instruction with over 50% single-cycle.

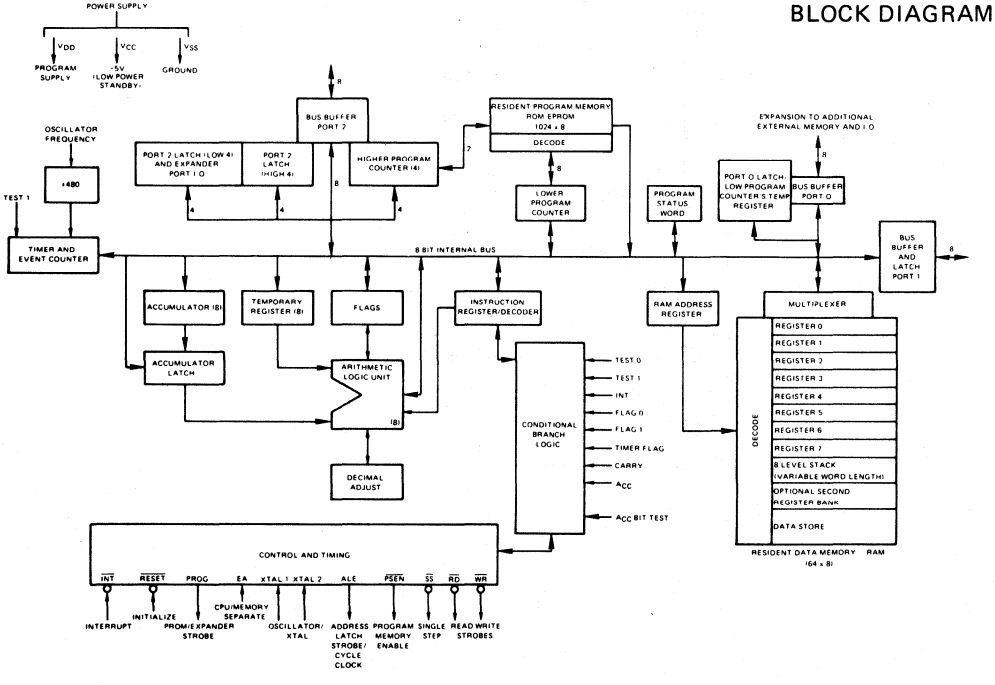
The μPD8048 series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8048 contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The μPD8748 differs from the μPD8048 only in its 1024 x 8-bit UV erasable EPROM program memory instead of the 1024 x 8-bit ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

The μPD8035L is intended for applications using external program memory only. It contains all the features of the μPD8048 except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{\text{RESET}}$	Active low input for processor initialization. $\overline{\text{RESET}}$ is also used for PROM programming verification and power-down (non TTL compatible V_{IH}).
5	$\overline{\text{SS}}$	Single Step input (active-low). $\overline{\text{SS}}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{\text{INT}}$	Interrupt input (active-low). $\overline{\text{INT}}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{\text{INT}}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{\text{RD}}$	READ strobe output (active-low). $\overline{\text{RD}}$ will pulse low when the processor performs a BUS READ. $\overline{\text{RD}}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{\text{PSEN}}$	Program Store Enable output (active-low). $\overline{\text{PSEN}}$ becomes active only during an external memory fetch.
10	$\overline{\text{WR}}$	WRITE strobe output (active-low). $\overline{\text{WR}}$ will pulse low when the processor performs a BUS WRITE. $\overline{\text{WR}}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12 – 19	$D_0 - D_7$ BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. The contents of the $D_0 - D_7$ BUS can be latched in a static mode. During an external memory fetch, the $D_0 - D_7$ BUS holds the least significant bits of the program counter. $\overline{\text{PSEN}}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the $D_0 - D_7$ BUS, controlled by ALE, $\overline{\text{RD}}$ and $\overline{\text{WR}}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21 – 24, 35 – 38	$P_{20} - P_{27}$: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in $P_{20} - P_{23}$. Bits $P_{20} - P_{23}$ are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. A +25V pulse applied to this input is used for programming the μPD8748. PROG is also used as an output strobe for the μPD8243.
26	V_{DD}	Programming Power Supply. V_{DD} must be set to +25V for programming the μPD8748, and to +5V for the ROM and PROM versions for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048.
27 – 34	$P_{10} - P_{17}$: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power Supply. V_{CC} must be +5V for programming and operation of the μPD8748, and for operation of the μPD8035L and μPD8048.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . -65°C to +150°C
Storage Temperature (Plastic Package) . . . . . -65°C to +150°C
Voltage on Any Pin . . . . . - 0.5 to +7 Volts ①
Power Dissipation . . . . . 1.5 W

Note: ① With respect to ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -0°C$ to $+70°C$; $V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (BUS)	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, PSEN, ALE)	V_{OL1}			0.45	V	$I_{OL} = 1.8$ mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	$I_{OL} = 1.0$ mA
Output Low Voltage (All Other Outputs)	V_{OL3}			0.45	V	$I_{OL} = 1.6$ mA
Output High Voltage (BUS)	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	2.4			V	$I_{OH} = -100\ \mu A$
Output High Voltage (All Other Outputs)	V_{OH2}	2.4			V	$I_{OH} = -40\ \mu A$
Input Leakage Current (T_1, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input Leakage Current (P_{10}-P_{17}, P_{20}-P_{27}, EA, $\overline{SS}$)	I_{IL1}			-500	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$
Output Leakage Current (BUS, T_0 – High Impedance State)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$
Power Down Supply Current	I_{DD}		7	15	mA	$T_a = 25°C$
Total Supply Current	$I_{DD} + I_{CC}$		60	135	mA	$T_a = 25°C$

DC CHARACTERISTICS PROGRAMMING THE μPD8748

$T_a = 25°C \pm 5°C$; $V_{CC} = +5V \pm 10\%$; $V_{DD} = +25V \pm 1V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
V_{DD} Program Voltage High-Level	V_{DOH}	24.0		26.0	V	
V_{DD} Voltage Low-Level	V_{DDL}	4.75		5.25	V	
PROG Voltage High-Level	V_{PH}	21.5		24.5	V	
PROG Voltage Low-Level	V_{PL}			0.2	V	
EA Program or Verify Voltage High-Level	V_{EAH}	21.5		24.5	V	
EA Voltage Low-Level	V_{EAL}			5.25	V	
V_{DD} High Voltage Supply Current	I_{DD}			30.0	mA	
PROG High Voltage Supply Current	I_{PROG}			16.0	mA	
EA High Voltage Supply Current	I_{EA}			1.0	mA	

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST ① CONDITIONS
ALE Pulse Width	t_{LL}	400			ns	
Address Setup before ALE	t_{AL}	120			ns	
Address Hold from ALE	t_{LA}	80			ns	
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	700			ns	
Data Setup before $\overline{WR}$	t_{DW}	500			ns	
Data Hold after $\overline{WR}$	t_{WD}	120			ns	C_L = 20 pF
Cycle Time	t_{CY}	2.5		15.0	μs	6 MHz XTAL
Data Hold	t_{DR}	0		200	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			500	ns	
Address Setup before $\overline{WR}$	t_{AW}	230			ns	
Address Setup before Data In	t_{AD}			950	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0			ns	
Control Pulse to ALE	**t_{CA}**	**10**			**ns**	

Notes: ① For Control Outputs: C_L = 80 pF
For Bus Outputs: C_L = 150 pF
$t_{CY} = 2.5\ \mu s$

PORT 2 TIMING

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

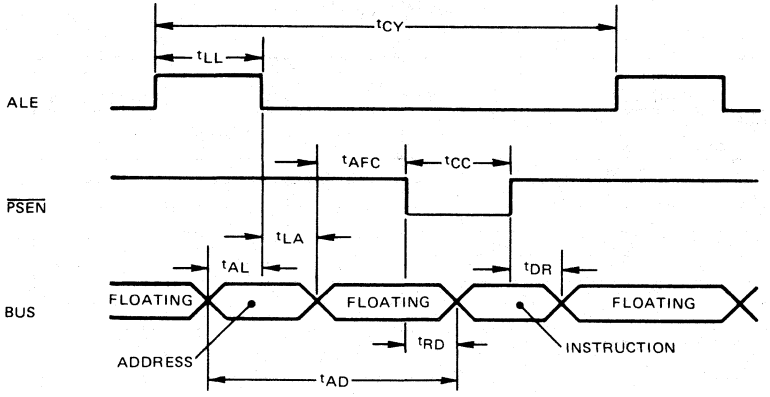
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Port Control Setup before Falling Edge of $\overline{PROG}$	t_{CP}	110			ns	
Port Control Hold after Falling Edge of $\overline{PROG}$	t_{PC}	100			ns	
$\overline{PROG}$ to Time P2 Input must be Valid	t_{PR}			810	ns	
Output Data Setup Time	t_{DP}	250			ns	
Output Data Hold Time	t_{PD}	65			ns	
Input Data Hold Time	t_{PF}	0		150	ns	
$\overline{PROG}$ Pulse Width	t_{PP}	1200			ns	
Port 2 I/O Data Setup	t_{PL}	350			ns	
Port 2 I/O Data Hold	t_{LP}	150			ns	

PROGRAMMING SPECIFICATIONS – μPD8748

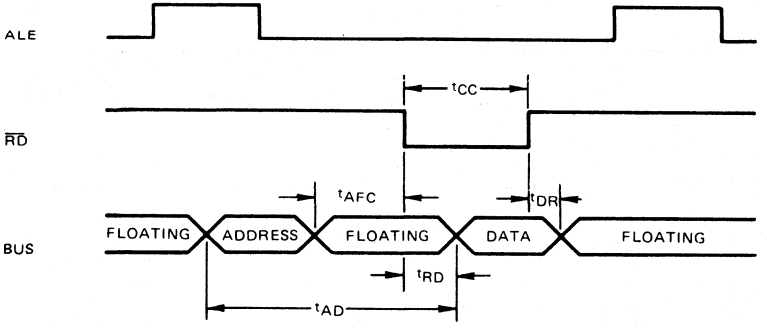
$T_a = 25°C \pm 5°C$; $V_{CC} = +5V \pm 10\%$; $V_{DD} = +25V \pm 1V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Setup Time before $\overline{RESET}$ ↑	t_{AW}	4 t_{CY}				
Address Hold Time after $\overline{RESET}$ ↑	t_{WA}	4 t_{CY}				
Data In Setup Time before $\overline{PROG}$ ↑	t_{DW}	4 t_{CY}				
Data In Hold Time after $\overline{PROG}$ ↓	t_{WD}	4 t_{CY}				
RESET Hold Time to VERIFY	t_{PH}	4 t_{CY}				
V_{DD}	t_{VDDW}	4 t_{CY}				
V_{DD} Hold Time after $\overline{PROG}$ ↓	t_{VDDH}	0				
Program Pulse Width	t_{PW}	50		60	ms	
Test 0 Setup Time before Program Mode	t_{TW}	4 t_{CY}				
Test 0 Hold Time after Program Mode	t_{WT}	4 t_{CY}				
Test 0 to Data Out Delay	t_{DO}			4 t_{CY}		
$\overline{RESET}$ Pulse Width to Latch Address	t_{WW}	4 t_{CY}				
V_{DD} and $\overline{PROG}$ Rise and Fall Times	t_r,t_f	0.5		2.0	μs	
Processor Operation Cycle Time	t_{CY}	5.0			μs	
$\overline{RESET}$ Setup Time before EA ↑	t_{RE}	4 t_{CY}				

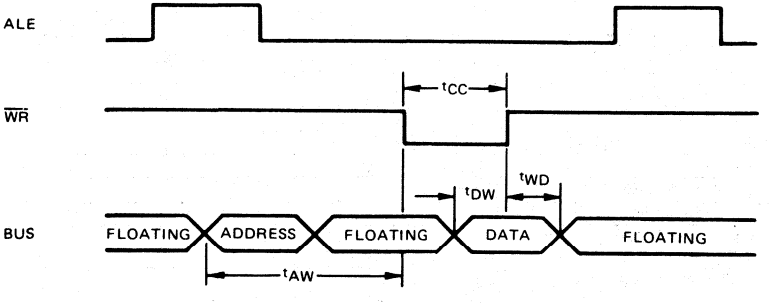
TIMING WAVEFORMS



INSTRUCTION FETCH FROM EXTERNAL MEMORY

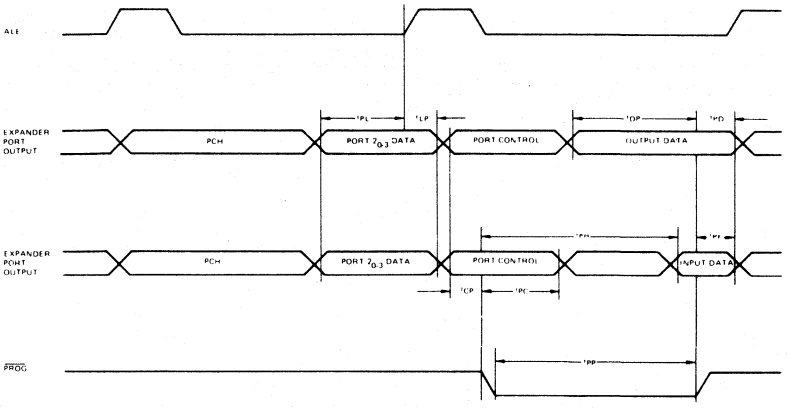


READ FROM EXTERNAL DATA MEMORY

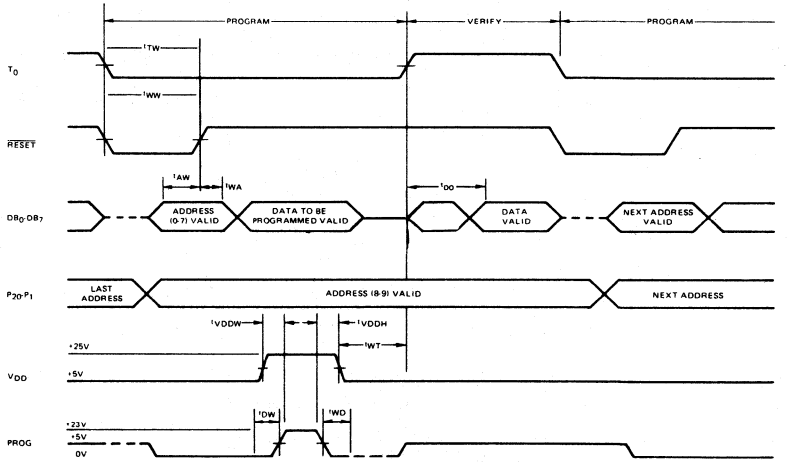


WRITE TO EXTERNAL MEMORY

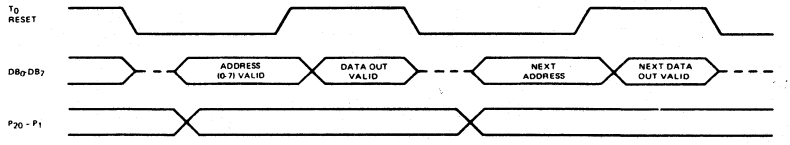
TIMING WAVEFORMS (CONT.)



PORT 2 TIMING



PROGRAM/VERIFY TIMING (μPD8748 ONLY)



VERIFY MODE TIMING (μPD8048/8748 ONLY)

Notes:

① Conditions: $\overline{CS}$ TTL Logic "1"; Ao TTL Logic "0" must be met. (Use 10K resistor to V_{CC} for $\overline{CS}$, and 10K resistor to V_{SS} for Ao)

② t_{CY} 5μs can be achieved using a 3 MHz frequency source (LC, XTAL or external) at the XTAL 1 and XTAL 2 inputs.

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
ACCUMULATOR																
ADD A, # data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) – 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) $(A_0) \leftarrow (A_7)$ for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 – 6 $(A_0) \leftarrow$ (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 – 6 $(A_7) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 – 6 $(A_7) \leftarrow$ (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	$(A_{4-7}) \rightleftarrows (A_0 - 3)$	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ←(PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2*	1				
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 – 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a :	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
DATA MOVES																
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1
INPUT/OUTPUT																
ANL BUS, #data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1	0	0	1	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL Pp, #data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 = 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	2	1				
ORL BUS, #data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1	0	0	0	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	2	1				
ORL Pp, #data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2).	1	0	0	0	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	2	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	2	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) + 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @Ri	((Ri)) ← ((Ri)) + 1; r = 0 – 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
RET	(SP) ← (SP) = 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) = 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

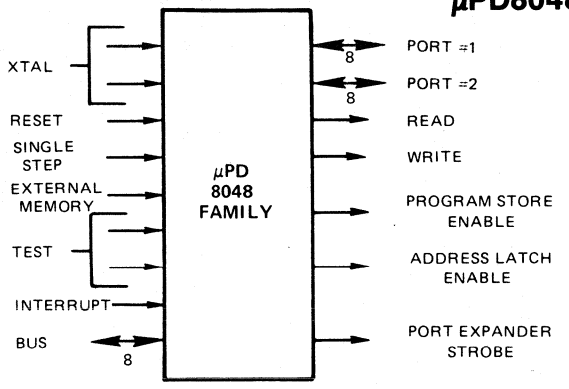
Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

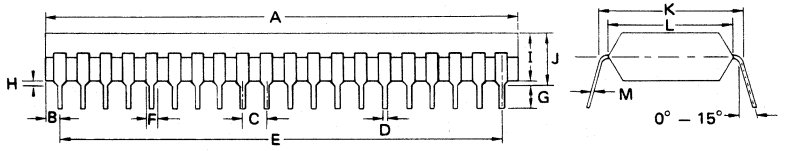
SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By

LOGIC SYMBOL



PACKAGE OUTLINES

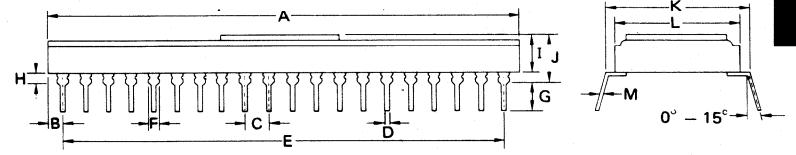
μPD8048C
μPD8035LC



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$

μPD8048D
μPD8748D
μPD8035LD



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5	2.03
B	1.62	0.06
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26	1.9
F	1.02	0.04
G	3.2	0.13
H	1.0	0.04
I	3.5	0.14
J	4.5	0.18
K	15.24	0.6
L	14.93	0.59
M	0.25 ± 0.05	0.01 ± 0.0019

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μPD80C48/μPD80C35
CMOS 8-BIT SINGLE-CHIP MICROCOMPUTER

Description

The NEC μPD80C48 is a true stand-alone 8-bit microcomputer fabricated with CMOS technology. The μPD80C48 contains all the functional blocks — 1K bytes ROM, 64 bytes RAM, 28 I/O lines, on-chip 8-bit Timer/Event counter, on-chip clock generator — to enable its use in stand-alone applications. For designs requiring extra capability the μPD80C48 can be expanded using industry standard μPD8080A/μPD8085A peripherals and memory products. The μPD80C35 differs from the μPD80C48 only in that the μPD80C35 contains no internal program memory (ROM).

Compatible with the industry-standard 8048, 8748, and 8035, the CMOS-fabricated μPD80C48 provides significant power consumption savings in applications requiring low power and portability. In addition to the power savings gained through CMOS technology, the NEC μPD80C48 features Halt and Stop modes to further minimize power drain.

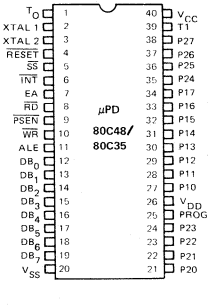
Features

- ☐ 8-bit CPU, ROM, RAM, I/O in a single package
- ☐ Hardware/Software-compatible with industry standard 8048, 8748, 8035 products
- ☐ 1K x 8 ROM
- ☐ 64 x 8 RAM
- ☐ 27 I/O lines
- ☐ 2.5 μs cycle time (6 MHz crystal)
- ☐ All instructions 1 or 2 cycles
- ☐ 97 instructions: 70% single-byte
- ☐ Internal Timer/Event Counter
- ☐ Two Interrupts (External and Timer)
- ☐ Easily expandable memory and I/O
- ☐ Bus-compatible with 8080A/8085A peripherals
- ☐ CMOS technology
- ☐ Operational over a 2.7 to 5.5 V_{CC} range
- ☐ Available in 40-pin DIP
- ☐ Low-power Standby modes
- ☐ Halt Mode
  - 1 mA typical supply current
  - Maintains internal logic values and control status
  - Initiated by HALT instruction
  - Released by External Interrupt or Reset
- ☐ Stop Mode
  - 1 μA typical supply current
  - Disables internal clock generation and internal logic
  - Maintains RAM
  - Initiated via Hardware (V_{DD})
  - Released via Reset

Pin Identification

Pin No.	Pin Symbol	Function
1	T0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non-TTL-compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for Halt/Stop Mode release (non-TTL-compatible V_{IH}).
5	$\overline{SS}$	Single step input (active-low). $\overline{SS}$ with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ starts an interrupt if an enable instruction has been executed. A reset disables the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	Read strobe output (active-low). $\overline{RD}$ pulses low when the processor performs a Bus Read. $\overline{RD}$ also enables data onto the processor Bus from a peripheral device and functions as a Read Strobe for external Data Memory.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	Write strobe output (active-low). $\overline{WR}$ pulses low when the processor performs a Bus Write. $\overline{WR}$ can also function as a Write Strobe for external Data Memory.
11	ALE	Address Latch Enable output (active high). Occuring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12 — 19	D_0 — D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the D_0 — D_7 Bus can be latched in a static mode. During an external memory fetch, the D_0 — D_7 Bus holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0 — D_7 Bus, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's Ground potential.
21 — 24, 35 — 38	P_{20} — P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20} — P_{23}. Bits P_{20} — P_{23} are also used as a 4-bit I/O bus for the μPD8243, Input/Output Expander.
25	PROG	PROG is used as an output strobe for the μPD8243.
26	V_{DD}	+5V during normal operation. V_{DD} is used in Stop Mode. By forcing V_{DD} low during a reset, the processor enters Stop Mode.
27 — 34	P_{10} — P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power Supply.

Pin Configuration



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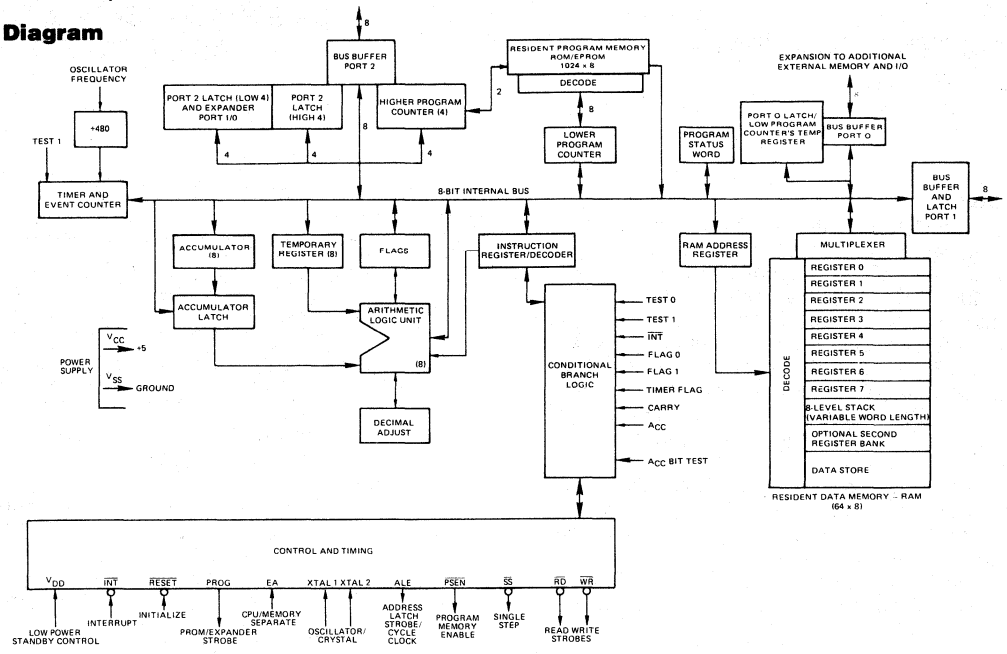
Block Diagram



Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−40°C to +85°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	V_{SS} −0.3V to V_{CC} +0.3V
Supply Voltage	V_{SS} −0.3 to +10V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditons outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −40°C to +85°C; V_{CC} = 2.7 to 5.5V, V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	−0.3		0.18 V_{CC}	V	
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}	0.7 V_{CC}		V_{CC}	V	
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}	0.8 V_{CC}		V_{CC}	V	
Output Low Voltage (BUS, RD, WR, PSEN, ALE)	V_{OL}			0.45	V	I_{OL} = 1.0 mA
Output High Voltage (BUS, RD, WR, PSEN, ALE)	V_{OH}	0.75 V_{CC}			V	I_{OH} = −100μA
Output High Voltage (All Other Outputs)	V_{OH1}	0.75 V_{CC}			V	I_{OH} = −1μA
Input Current (Port 1, Port 2)	I_{ILP}			−30	μA	$V_{IN} \leq V_{IL}$
Input Current (SS, RESET)	I_{ILC}			−40	μA	$V_{IN} \leq V_{IL}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Leakage Current: (T1, INT)	I_{IL}			±1	μA	$V_{SS} < V_{IN} < V_{CC}$
Input Leakage Current (EA)	I_{IL1}			±3	μA	$V_{SS} < V_{IN} < V_{CC}$
Output Leakage Current (BUS, T_0 — High Impedance State)	I_{OL}			±1	μA	$V_{SS} < V_{IN} < V_{CC}$
Total Supply Current	$I_{DD} + I_{CC}$		5	10	mA	T_a = 25°C 6 MHz
Halt Power Supply Current	I_{CC}		1	3	mA	6 MHz
Stop Mode Supply Current	I_{CC}		1	20	μA	6 MHz
RAM Data Retention Voltage	$V_{CC}DR$	2.0			V	Stop Mode (V_{DD}, RESET ≤ .4V) or RESET ≤ 0.4V

AC Characteristics

Read, Write and Instruction Fetch—External Data and Program Memory

T_a = −40°C to +85°C

Parameter	Symbol	Limits ② Min	Max	Unit	Limits ③ Min	Max	Unit	Test Conditions ①
ALE Pulse Width	t_{LL}	400		ns	1.6		μs	
Address Setup before ALE	t_{AL}	120		ns	500		ns	
Address Hold from ALE	t_{LA}	80		ns	100		ns	
Control Pulse Width (PSEN, RD, WR)	t_{CC}	700		ns	2.5		μs	
Data Setup before WR	t_{DW}	500		ns	2.0		μs	
Data Hold after WR	t_{WD}	120		ns	200		ns	C_L = 20 pF, t_{CY} = 2.5 μs
Cycle Time	t_{CY}	2.5	100	s	See Characterization Chart 1			
Data Hold	t_{DR}	0	200	ns	0	800	ns	

AC Characteristics (Cont.)

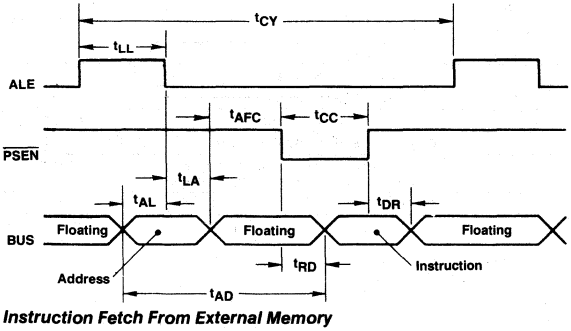
Parameter	Symbol	Limits ② Min	Limits ② Max	Unit	Limits ③ Min	Limits ③ Max	Unit	Test Conditions ①
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}		500	ns		1.5	μs	
Address Setup before $\overline{WR}$	t_{AW}	230		ns	1.0		μs	
Address Setup before Data In	t_{AD}		950	ns		4.0	μs	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0		ns	0		ns	
Control Pulse to ALE	t_{CA}	10		ns	10		ns	

Port 2 Timing
T_a = −40°C to +85°C

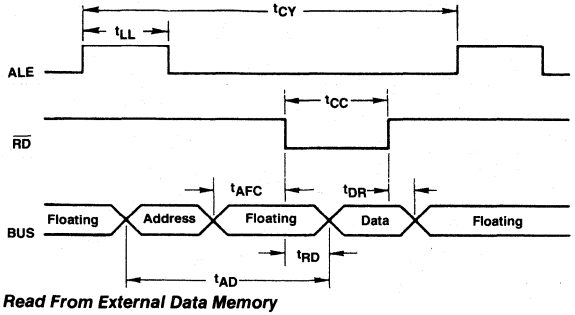
Parameter	Symbol	Limits ② Min	Limits ② Max	Unit	Limits ③ Min	Limits ③ Max	Unit	Test Conditions ①
Port Control Setup before Falling Edge of PROG	t_{CP}	110		ns	500		ns	
Port Control Hold after Falling Edge of PROG	t_{PC}		80	ns	0	400	ns	
PROG to Time P2 input must be Valid	t_{PR}		810	ns		4.0	μs	
Output Data Setup Time	t_{DP}	250		ns	0	500	ns	
Output Data Hold Time	t_{PD}	65		ns	5.0		μs	
Input Data Hold Time	t_{PF}	0	150	ns	1.0		μs	
PROG Pulse Width	t_{PP}	1200		ns	100		ns	
Port 2 I/O Data Setup	t_{PL}	350		ns	1.0		μs	
Port 2 I/O Data Hold	t_{LP}	150		ns	600		ns	

Notes:
① For Control Outputs: C_L = 80 pF
For Bus Outputs: C_L = 150 pF.
② V_{CC} = +5V ± 10%.
③ V_{CC} = +2.7V to +5.5V

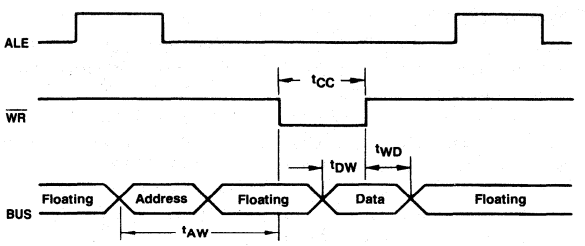
Timing Waveforms



Instruction Fetch From External Memory

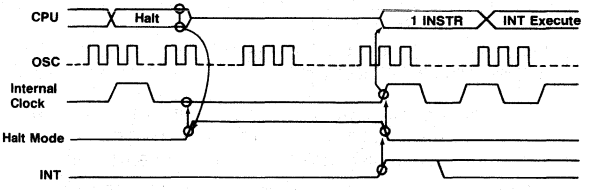


Read From External Data Memory

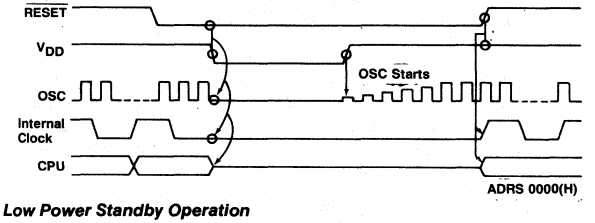


Write to External Memory

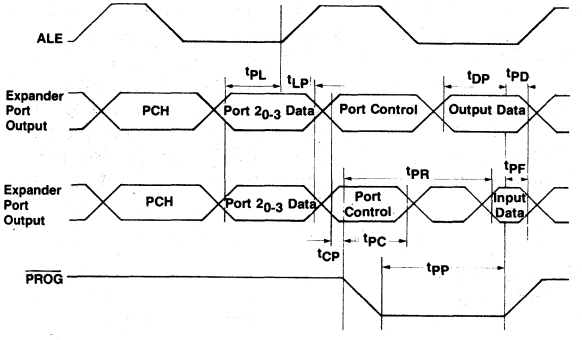
1) Halt Mode (When EI)



2) Stop Mode



Low Power Standby Operation



Port 2 Timing

Features

The NEC μPD80C48/μPD80C35 contains all the functional features of the industry standard 8048/8035. The power down mode of the μPD8048 is replaced with two additional power standby features for added power savings. Depending on desired power consumption savings and internal logic status maintenance, Halt mode or Stop mode may be used.

Halt Mode

The μPD80C48/80C35 includes a Halt instruction (01H) — an addition to the standard 8048 instruction set. Upon execution of the Halt instruction, the μPD80C48 enters a Halt mode where the internal clocks and internal logic are disabled. The oscillator, however, continues its operation. The state of all internal logic values and control status prior to the halt state is maintained. Under Halt mode, power consumption is less than 30% of normal μPD80C48 operation, and 2% of 8048 operation.

Halt mode is released through either of two methods: an active input on the $\overline{INT}$ line or a reset operation. Under the Interrupt Release mode, if interrupts are enabled (EI Mode), the $\overline{INT}$ input restarts the internal clocks to the internal logic. The μPD80C48 then executes the instruction immediately following the Halt instruction, before branching to the interrupt service routine.

If interrupts are disabled (DI Mode), an $\overline{INT}$ active signal causes the program operation to resume, beginning from the next sequential address after the Halt instruction.

A $\overline{RESET}$ input causes the normal reset function which starts the program at address 0H.

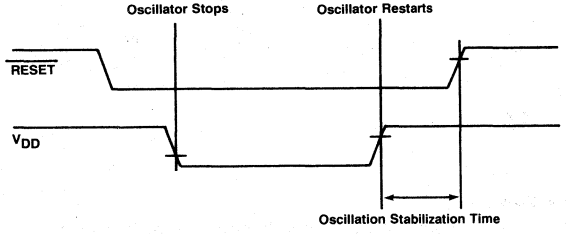
Note: The V_{CC} range under Halt mode must be maintained at +5V ± 10%, as in normal operation.

Stop Mode

Stop mode provides additional power consumption savings over the Halt mode of operation. Stop mode is initiated by forcing V_{DD} to the low state during a $\overline{RESET}$ low. While in Stop mode, oscillator operation is discontinued and only the contents of RAM are maintained.

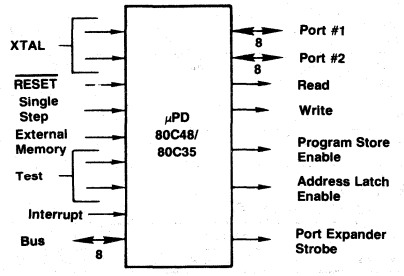
The μPD80C48 is released from Stop mode when V_{DD} is forced high during a $\overline{RESET}$ low. Clock generation is then restarted. When oscillator stabilization is achieved, $\overline{RESET}$ is pulled high and the program is restarted from location 0.

To ensure reliable Stop mode operation, V_{DD} must be brought back up to +5V ± 10%, when releasing the Stop mode. The V_{DD} pin must be protected against noise conditions since it controls oscillator operation. In the Stop mode, V_{CC} may be dropped as low as 2.0 volts to ensure RAM data retention (V_{CC} DR). $\overline{RESET}$ must be held low after oscillation stops until the oscillator is restarted.



Stop Mode Timing

Logic Symbol



Symbol Definitions:

Symbol	Description
A	Accumulator
AC	Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 — 7)
BS	Bank Switch
Bus	Bus Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
P_p	Port Designator (p = 1, 2 or 4 — 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 — 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T0, T1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
S	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
—	Replaced By

Instruction Set

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator																
ADD, A = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
Add A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add indirect the contents of the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, = data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, = data	(A) ← (A) AND data	Logical AND specified immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical AND contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical AND indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	Clear the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		Decimal Adjust the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	Decrement by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 - 6	Rotate Accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 - 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1), N = 0 - 6 (A_7) ← (A_0)	Rotate Accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 - 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ⇄ (A_{0}-3)	Swap the two 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 - 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 - 1	Logical XOR indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) - 1; r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 - 7) ← addr if Bb = 1 (PC) - (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF 0 addr	(PC 0 - 7) ← addr if FO = 1 (PC) ← (PC) + 2 if FO = 0	Jump to specified address if Flag F 0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF 1 addr	(PC 0 - 7) ← addr if F 1 = 1 (PC) ← (PC) + 2 if F 1 = 0	Jump to specified address if Flag F 1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 - 10) ← addr 8 – 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 7) ← addr if I = 0 (PC) ← (PC) + 2 if =1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Branch (Cont.)																
JNT0 addr	(PC 0 - 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 - 7) ←addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 - 7) ←addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified addres if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 - 7) ←addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 - 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) - 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENTO CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MBO	(DBF) ← 0	Select Bank 0 (locations 0 - 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 - 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 - 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 - 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
HALT		Initiate Halt State.	0	0	0	0	0	0	0	1	1	1				
Data Moves																
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, = data	(Rr) ← data; r = 0 - 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A), r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, = data	((Rr)) ← data; r = 0 - 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 - 7) ← (A) (PC 8 - 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A), r = 0 - 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4 bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement of Flag F 1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Input/Output																
ANL BUS, = data	(BUS) ← (BUS) AND data	Logical AND immediate specified data with contents of Bus.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL P_p, = data	(P_p) ← (P_p) AND data p = 1 - 2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD P_p, A	(P_p) ← (P_p) AND (A0 - 3) p = 4 - 7	Logical AND contents of Accumulator with designated port (4 - 7).	1	0	0	1	1	1	p	p	2	1				
IN A, P_p	(A) ← (P_p), p = 1 - 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed Bus data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, P_p	(A 0 - 3) ← (P_p); p = 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD P_p, A	(P_p) ← A 0 - 3; p = 4 - 7	Move contents of Accumulator designated port (4 - 7).	0	1	1	1	1	p	p	1	1					
ORL BUS, = data	(BUS) ← (BUS) OR data	Logical OR immediate specified data with contents of Bus.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD P_p, A	(P_p) ← (P_p) OR (A0 - 3) P = 4 - 7	Logical OR contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1				
ORL P_p, = data	(P_p) ← (P_p) OR data p = 1 - 2	Logical OR immediate specified data with designated port (1 - 2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto Bus.	0	0	0	0	0	0	1	0	1	1				
OUTL P_p, A	(P_p) ← (A); p = 1 - 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1				
Registers																
DEC Rr (Rr)	(Rr) ← (Rr) 1; r = 0 - 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1, r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ R	((Rr)) ← ((Rr)) + 1; r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
Subroutine																
Call addr	((SP)) ← (PC), (PSW 4 - 7)	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2				
	(SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
RET	(SP) ← (SP) 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 - 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
Timer/Counter																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Counter for Timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes:

① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

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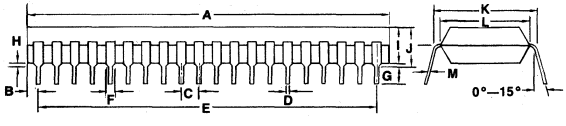
Package Outlines
μPD80C48C
μPD80C35C

Plastic

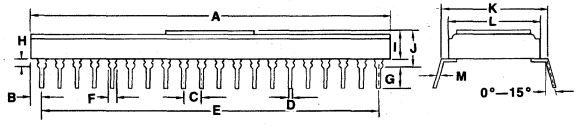
Item	Millimeters	Inches
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600 MAX
L	13.2 MAX	0.520 MAX
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD80C48D
μPD80C35D

Ceramic

Item	Millimeters	Inches
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004



HIGH PERFORMANCE SINGLE CHIP 8-BIT MICROCOMPUTERS

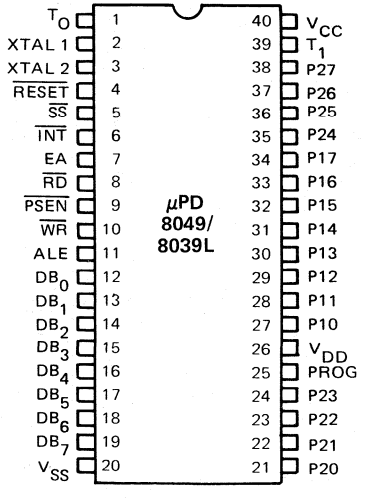
DESCRIPTION

The NEC μPD8049 and μPD8039L are single chip 8-bit microcomputers. The processors differ only in their internal program memory options: the μPD8049 has 2K x 8 bytes of mask ROM and the μPD8039L has external program memory. Both of these devices feature new, high performance 11 MHz operation.

FEATURES

- High Performance 11 MHz Operation
- Fully Compatible with Industry Standard 8049/8039
- Pin Compatible with the μPD8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V ±10% Supply
- 1.36 μs Cycle Time. All Instructions 1 or 2 Bytes
- Programmable Interval Timer/Event Counter
- 2K x 8 Bytes of ROM, 128 x 8 Bytes of RAM
- Single Level Interrupt
- 96 Instructions: 70 Percent Single Byte
- 27 I/O Lines
- Internal Clock Generator
- Expandable with 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40-Pin Packages

PIN CONFIGURATION



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μPD8049/8039L

FUNCTIONAL DESCRIPTION

The NEC μPD8049 and μPD8039L are high performance, single component, 8-bit parallel microcomputers using N-channel silicon gate MOS technology. The μPD8049 and μPD8039L function efficiently in control as well as arithmetic applications. The powerful instruction set eases bit handling applications and provides facilities for binary and BCD arithmetic. Standard logic functions implementation is facilitated by the large variety of branch and table look-up instructions.

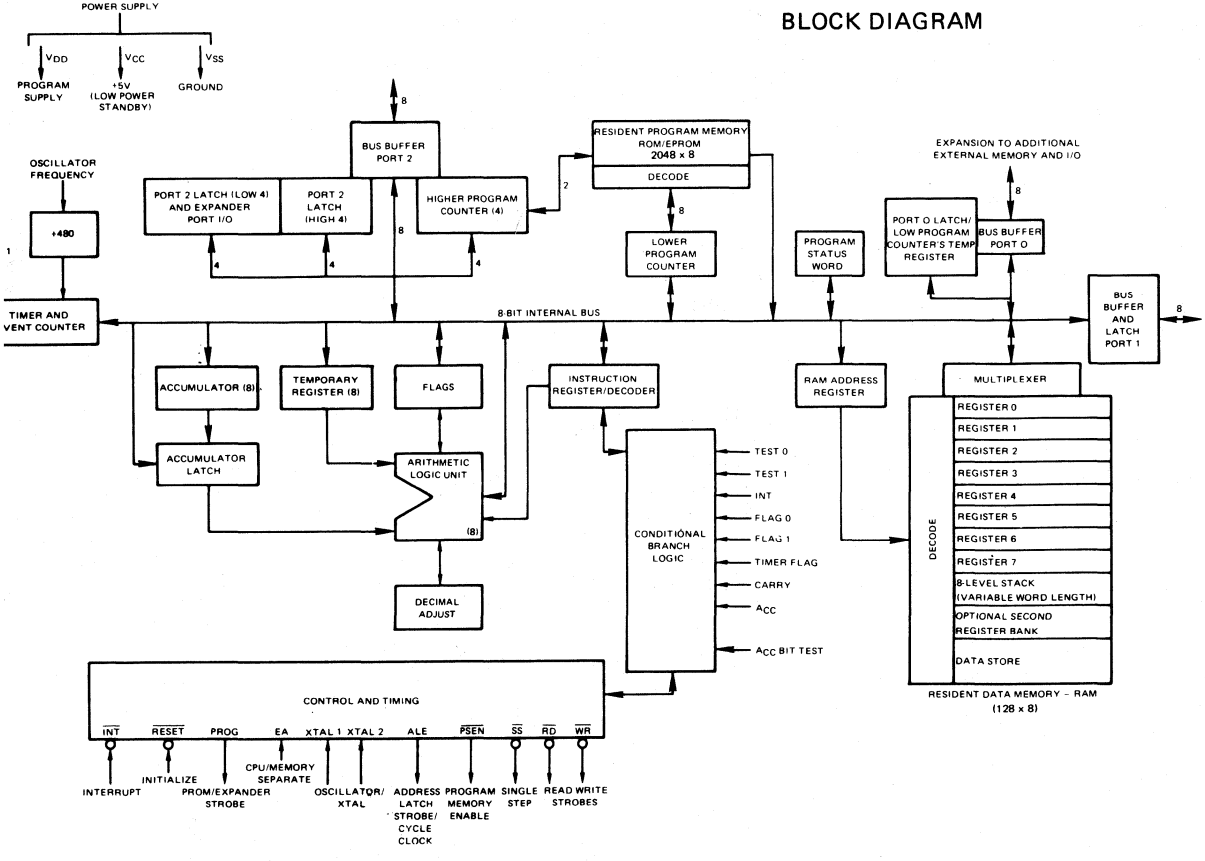
The μPD8049 and μPD8039L instruction set is comprised of 1 and 2 byte instructions with over 70 percent single-byte. The instruction set requires only 1 or 2 cycles per instruction with over 50 percent single-cycle.

The μPD8049 and μPD8039L microprocessors will function as stand-alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8049 contains the following functions usually found in external peripheral devices: 2048 x 8 bits of mask ROM program memory; 128 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; and oscillator and clock circuitry.

The μPD8039L is intended for applications using external program memory only. It contains all the features of the μPD8049 except the 2048 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENT0 CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal, LC, or external frequency source. (Non-TTL compatible V_{IH}.)
3	XTAL 2	The other side of the crystal or LC frequency source. For external sources, XTAL 2 must be driven with the logical complement of the XTAL 1 input.
4	$\overline{RESET}$	Active low input from processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe outputs (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12-19	D_0-D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the D_0-D_7 BUS can be latched in a static mode. During an external memory fetch, the D_0-D_7 BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0-D_7 BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21-24, 35-38	P_{20}-P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20}-P_{23}. Bits P_{20}-P_{23} are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	PROG is used as an output strobe for μPD8243's during I/O expansion. When the μPD8049 is used in a stand-alone mode the PROG pan can be allowed to float.
26	V_{DD}	V_{DD} is used to provide +5V to the 128 x 8 bit RAM section. During normal operation V_{CC} must also be +5V to provide power to the other functions in the device. During stand-by operation V_{DD} must remain at +5V while V_{CC} is at ground potential.
27-34	P_{10}-P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V during normal operation.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +150°C
Voltage on Any Pin	− 0.5 to +7 Volts ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

$T_a = 25°C$

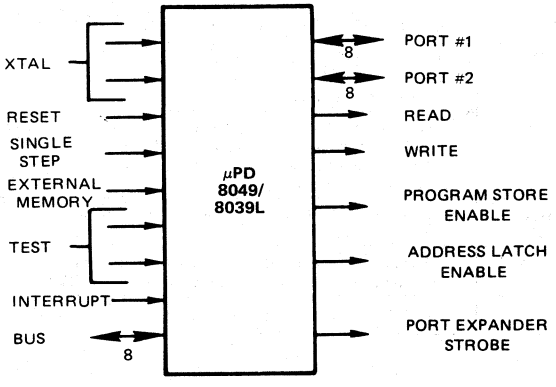
*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage ($\overline{RESET}$, XTAL 1, XTAL 2)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output Low Voltage (All Other Outputs Except PROG)	V_{OL1}			0.45	V	$I_{OL} = 1.6$ mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	$I_{OL} = 1.0$ mA
Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH}	2.4			V	$I_{OH} = -100\,\mu A$
Output High Voltage (All Other Outputs)	V_{OH1}	2.4			V	$I_{OH} = -50\,\mu A$
Input Leakage Current (T_1, EA, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (BUS, T_0 – High Impedance State)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$
Power Down Supply Current	I_{DD}		25	50	mA	$T_a = 25°C$
Total Supply Current	$I_{DD} + I_{CC}$		100	170	mA	$T_a = 25°C$

LOGIC SYMBOL



AC CHARACTERISTICS

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
ALE Pulse Width	t_{LL}	150			ns	
Address Setup before ALE	t_{AL}	70			ns	
Address Hold from ALE	t_{LA}	50			ns	
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	300			ns	
Data Setup before $\overline{WR}$	t_{DW}	250			ns	
Data Hold after $\overline{WR}$	t_{WD}	40			ns	C_L = 20 pF ③
Cycle Time	t_{CY}	1.36		15.0	μs	
Data Hold	t_{DR}	0		100	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			200	ns	
Address Setup before $\overline{WR}$	t_{AW}	200			ns	
Address Setup before Data In	t_{AD}			400	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	-40			ns	

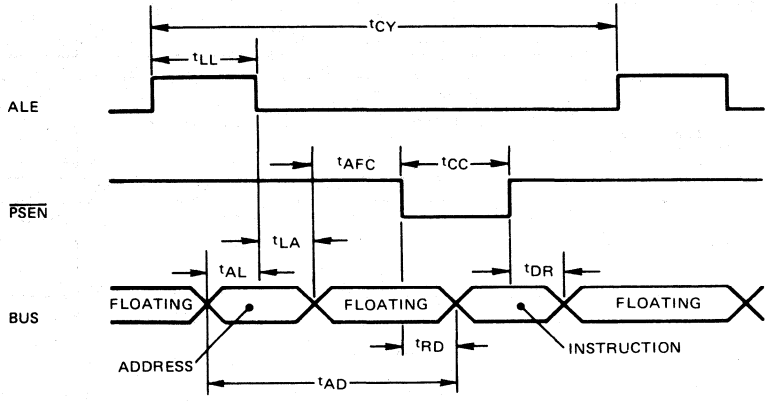
Notes: ① For Control Outputs: C_L = 80 pF
② For Bus Outputs: C_L = 150 pF
③ t_{CY} = 1.36 μs

PORT 2 TIMING

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

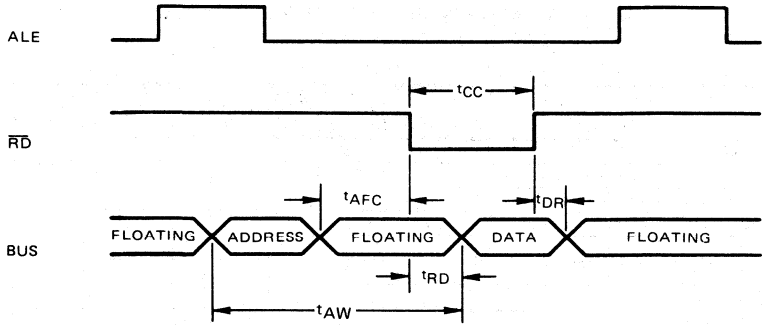
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Port Control Setup before Falling Edge of PROG	t_{CP}	100			ns	
Port Control Hold after Falling Edge of PROG	t_{PC}	60			ns	
PROG to Time P2 Input must be Valid	t_{PR}			650	ns	
Output Data Setup Time	t_{DP}	200			ns	
Output Data Hold Time	t_{PD}	20			ns	
Input Data Hold Time	t_{PF}	0		150	ns	
PROG Pulse Width	t_{PP}	700			ns	
Port 2 I/O Data Setup	t_{PL}	150			ns	
Port 2 I/O Data Hold	t_{LP}	20			ns	

TIMING WAVEFORMS

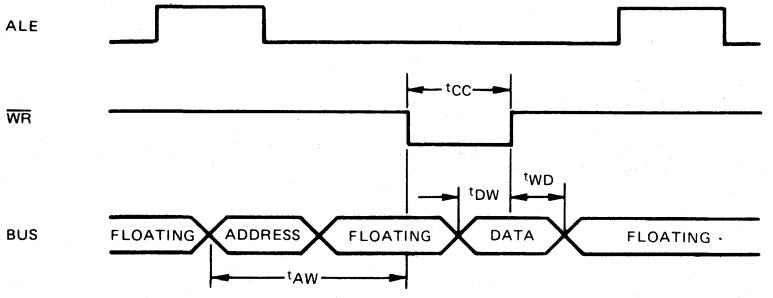


INSTRUCTION FETCH FROM EXTERNAL MEMORY

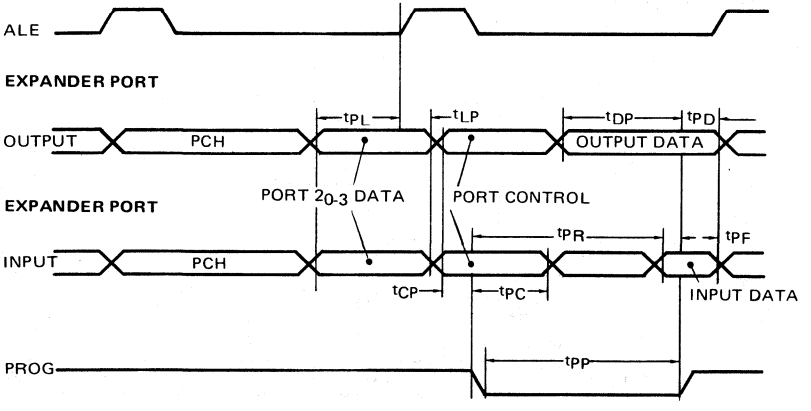
TIMING WAVEFORMS (CONT.)



READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL MEMORY



PORT 2 TIMING

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
ACCUMULATOR																
ADD A, = data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulatnr.	0	0	0	0	0	0	1	1	2	2	•			
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, = data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0	0	0	1	0	0	1	1	2	2	•			
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0	1	0	1	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0	1	0	0	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 7	Logical ORcontents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) $(A_0) \leftarrow (A_7)$ for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 6 $(A_0) \leftarrow$ (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 – 6 $(A_7) \leftarrow (A_0)$	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 – 6 $(A_7) \leftarrow$ (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	$(A_{4-7}) \rightarrow (A_{0-3})$	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1	1	0	1	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1	1	1	0	1	r	r	r	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2	b_1	b_0	1	0	0	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1	1	1	1	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1	0	1	1	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0	1	1	1	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10}	a_9	a_8	0	0	1	0	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1	1	1	0	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JNI addr	(PC 0 – 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1	0	0	0	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						

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INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 – 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 – 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
DATA MOVES																
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

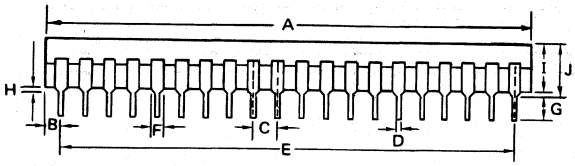
MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1
INPUT/OUTPUT																
ANL BUS, = data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1	0	0	1	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL Pp, = data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, = data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1	0	0	0	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, = data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2).	1	0	0	0	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	1	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) – 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) +1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4 – 7)	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2				
	(SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

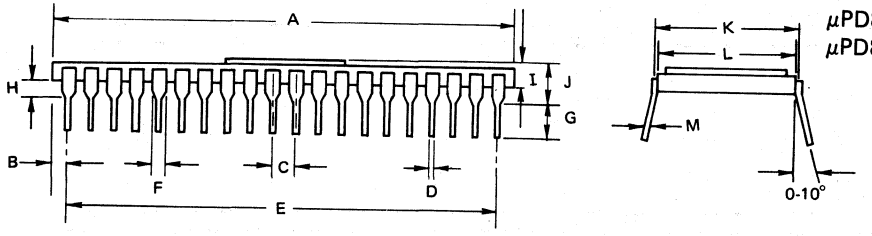
SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By



PACKAGE OUTLINES
μPD8049C
μPD8039LC

PLASTIC

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62 MAX	0.064 MAX
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24 TYP	0.600 TYP
L	13.2 TYP	0.520 TYP
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8049D
μPD8039LD

CERAMIC

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

μPD80C49/μPD80C39
CMOS 8-BIT SINGLE-CHIP MICROCOMPUTER

Description

The NEC μPD80C49 is a true stand-alone 8-bit microcomputer fabricated with CMOS technology. The μPD80C49 contains all the functional blocks — 1K bytes ROM, 64 bytes RAM, 28 I/O lines, on-chip 8-bit Timer/Event counter, on-chip clock generator — to enable its use in stand-alone applications. For designs requiring extra capability the μPD80C49 can be expanded using industry standard μPD8080A/μPD8085A peripherals and memory products. The μPD80C39 differs from the μPD80C49 only in that the μPD80C39 contains no internal program memory (ROM).

Compatible with the industry-standard 8049 and 8039, the CMOS-fabricated μPD80C49 provides significant power consumption savings in applications requiring low power and portability. In addition to the power savings gained through CMOS technology, the NEC μPD80C49 features Halt and Stop modes to further minimize power drain.

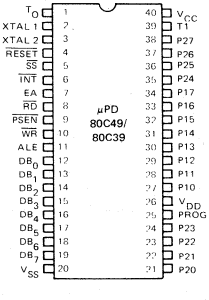
Features

- ☐ 8-bit CPU, ROM, RAM, I/O in a single package
- ☐ Hardware/Software-compatible with industry standard 8049, 8039 products
- ☐ 2K x 8 ROM
- ☐ 128 x 8 RAM
- ☐ 27 I/O lines
- ☐ 2.5 μs cycle time (6 MHz crystal)
- ☐ All instructions 1 or 2 cycles
- ☐ 97 instructions: 70% single-byte
- ☐ Internal Timer/Event Counter
- ☐ Two Interrupts (External and Timer)
- ☐ Easily expandable memory and I/O
- ☐ Bus-compatible with 8080A/8085A peripherals
- ☐ CMOS technology requiring a single +5V supply
- ☐ Available in 40-pin DIP
- ☐ Low-power Standby modes
- ☐ Halt Mode
  - 1 mA typical supply current
  - Maintains internal logic values and control status
  - Initiated by HALT instruction
  - Released by External Interrupt or Reset
- ☐ Stop Mode
  - 1 μA typical supply current
  - Disables internal clock generation and internal logic
  - Maintains RAM
  - Initiated via Hardware (V_{DD})
  - Released via Reset

Pin Identification

Pin No.	Pin Symbol	Function
1	T0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non-TTL-compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. RESET is also used for Halt/Stop Mode release (non-TTL-compatible V_{IH}).
5	$\overline{SS}$	Single step input (active-low). SS with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). INT starts an interrupt if an enable instruction has been executed. A reset disables the interrupt. INT can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	Read strobe output (active-low). RD pulses low when the processor performs a Bus Read. RD also enables data onto the processor Bus from a peripheral device and functions as a Read Strobe for external Data Memory.
9	$\overline{PSEN}$	Program Store Enable output (active-low). PSEN becomes active only during an external memory fetch.
10	$\overline{WR}$	Write strobe output (active-low). WR pulses low when the processor performs a Bus Write. WR can also function as a Write Strobe for external Data Memory.
11	ALE	Address Latch Enable output (active high). Occuring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12 — 19	D_0 — D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using RD and WR strobes. The contents of the D_0 — D_7 Bus can be latched in a static mode. During an external memory fetch, the D_0 — D_7 Bus holds the least significant bits of the program counter. PSEN controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0 — D_7 Bus, controlled by ALE, RD and WR, contains address and data information.
20	V_{SS}	Processor's Ground potential.
21 — 24, 35 — 38	P_{20} — P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20} — P_{23}. Bits P_{20} — P_{23} are also used as a 4-bit I/O bus for the μPD8243, Input/Output Expander.
25	PROG	PROG is used as an output strobe for the μPD8243.
26	V_{DD}	+5V during normal operation. V_{DD} is used in Stop Mode. By forcing V_{DD} low during a reset, the processor enters Stop Mode.
27 — 34	P_{10} — P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power Supply. V_{CC} must be +5V for operation of the μPD80C49 and μPD80C39.

Pin Configuration



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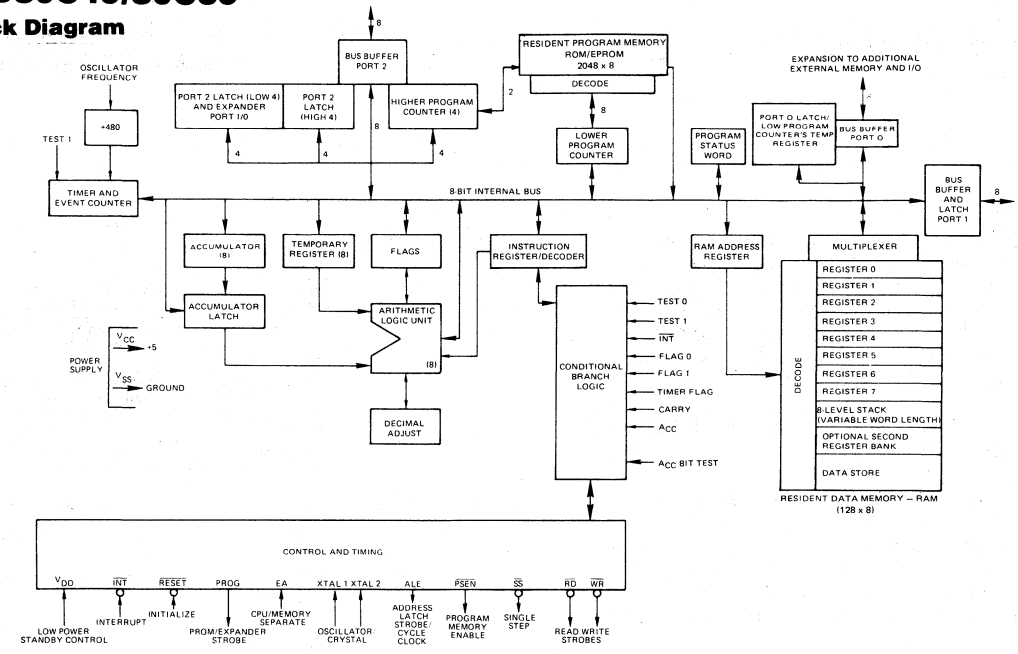
μPD80C49/80C39

Block Diagram



Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−40°C to +85°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +150°C
Voltage on Any Pin	V_{SS} −0.3V to V_{CC} +0.3V
Supply Voltage	V_{SS} −0.3 to +10V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −40°C to +85°C; V_{CC} = V_{DD} = +5V ± 10%, V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	−0.3		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}	V_{CC}−2		V_{CC}	V	
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}	V_{CC}−1		V_{CC}	V	
Output Low Voltage (BUS, RD, WR, PSEN, ALE)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage (BUS, RD, WR, PSEN, ALE)	V_{OH}	2.4			V	I_{OH} = −100μA
Output High Voltage (All Other Outputs)	V_{OH1}	2.4			V	I_{OH} = −5μA
Output High Voltage (All Outputs)	V_{OH2}	V_{CC}−0.5			V	I_{OH} = −0.2μA
Input Current (Port 1, Port 2)	I_{ILP}		−15	−40	μA	$V_{IN} \leq V_{IL}$
Input Current (SS, RESET)	I_{ILC}			−40	μA	$V_{IN} \leq V_{IL}$
Input Leakage Current: (T1, INT)	I_{IL}			±1	μA	$V_{SS} < V_{IN} < V_{CC}$
Input Leakage Current (EA)	I_{IL1}			±3	μA	$V_{SS} < V_{IN} < V_{CC}$
Output Leakage Current (BUS, T_0 — High Impedance State)	I_{OL}			±1	μA	$V_{SS} < V_{IN} < V_{CC}$
Total Supply Current	$I_{DD} + I_{CC}$		5	10	mA	T_a = 25°C 6 MHz
Halt Power Supply Current	I_{CC}		1	3	mA	6 MHz
Stop Mode Supply Current	I_{CC}		1	20	μA	6 MHz
RAM Data Retention Voltage	$V_{CC}DR$	2.0			V	Stop Mode (V_{DD}, RESET ≤ .4V) or RESET ≤ 0.4V

AC Characteristics

Read, Write and Instruction Fetch — External Data and Program Memory

T_a = −40°C to +85°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions①
ALE Pulse Width	t_{LL}	400			ns	
Address Setup before ALE	t_{AL}	120			ns	
Address Hold from ALE	t_{LA}	80			ns	
Control Pulse Width (PSEN, RD, WR)	t_{CC}	700			ns	
Data Setup before WR	t_{DW}	500			ns	
Data Hold after WR	t_{WD}	120			ns	C_L = 20 pF
Cycle Time	t_{CY}	2.5		100	μs	6 MHz XTAL
Data Hold	t_{DR}	0		200	ns	
PSEN, RD to Data In	t_{RD}			500	ns	
Address Setup before WR	t_{AW}	230			ns	
Address Setup before Data In	t_{AD}			950	ns	
Address Float to RD, PSEN	t_{AFC}	0			ns	
Control Pulse to ALE	t_{CA}	10			ns	

Notes:

① For Control Outputs: C_L = 80 pF
For Bus Outputs: C_L = 150 pF

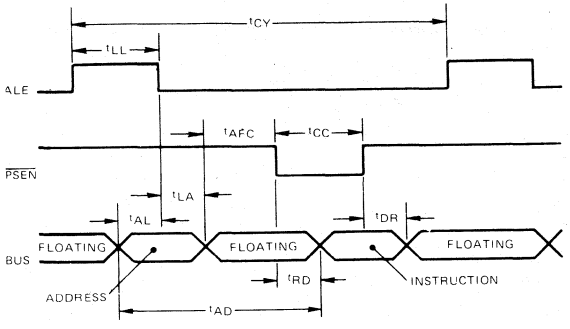
AC Characteristics (Cont.)

Port 2 Timing

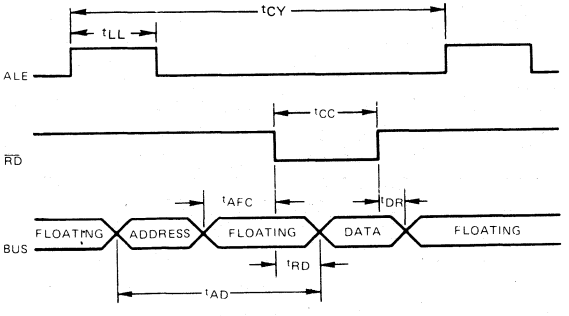
$T_a = -40°C$ to $85°C$; $V_{CC} = +5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port Control Setup before Falling Edge of PROG	t_{CP}	110			ns	
Port Control Hold after Falling Edge of PROG	t_{PC}			80	ns	
PROG to Time P2 input must be Valid	t_{PR}			810	ns	
Output Data Setup Time	t_{DP}	250			ns	
Output Data Hold Time	t_{PD}	65			ns	
Input Data Hold Time	t_{PF}	0		150	ns	
PROG Pulse Width	t_{PP}	1200			ns	
Port 2 I/O Data Setup	t_{PL}	350			ns	
Port 2 I/O Data Hold	t_{LP}	150			ns	

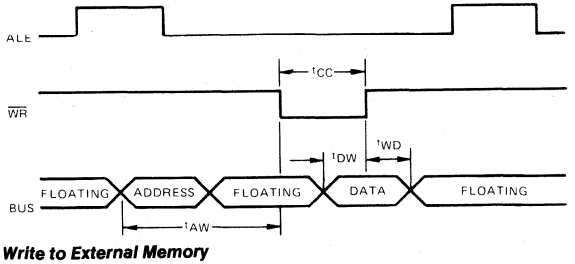
Timing Waveforms



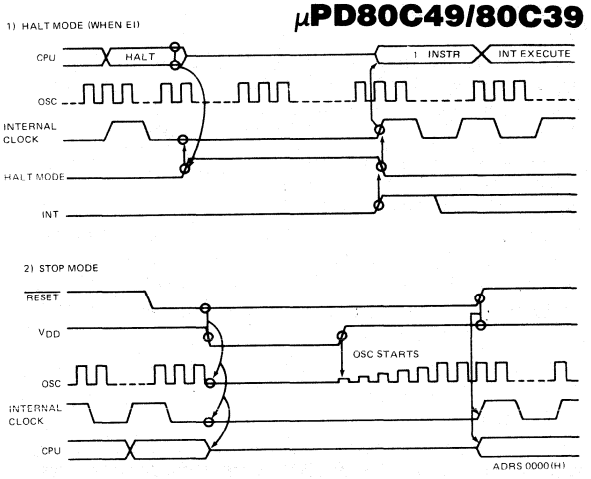
Instruction Fetch From External Memory



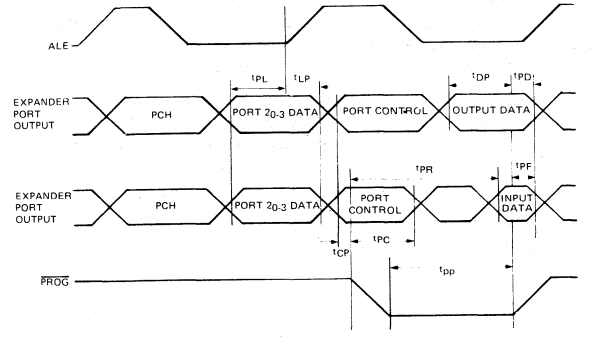
Read From External Data Memory



Write to External Memory



Low Power Standby Operation



Port 2 Timing

7

Features

The NEC μPD80C49/μPD80C39 contains all the functional features of the industry standard 8049/8039. The power down mode of the μPD8048 is replaced with two additional power standby features for added power savings. Depending on desired power consumption savings and internal logic status maintenance, Halt mode or Stop mode may be used.

Halt Mode

The μPD80C49/80C39 includes a Halt instruction (01H) — an addition to the standard 8049 instruction set. Upon execution of the Halt instruction, the μPD80C49 enters a Halt mode where the internal clocks and internal logic are disabled. The oscillator, however, continues its operation. The state of all internal logic values and control status prior to the halt state is maintained. Under Halt mode, power consumption is less than 10% of normal μPD80C49 operation, and 1% of 8049 operation.

Halt mode is released through either of two methods: an active input on the $\overline{INT}$ line or a reset operation. Under the Interrupt Release mode, if interrupts are enabled (EI Mode), the $\overline{INT}$ input restarts the internal clocks to the internal logic. The μPD80C49 then executes the instruction immediately following the Halt instruction, before branching to the interrupt service routine.

If interrupts are disabled (DI Mode), an $\overline{INT}$ active signal causes the program operation to resume, beginning from the next sequential address after the Halt instruction.

A $\overline{RESET}$ input causes the normal reset function which starts the program at address 0H.

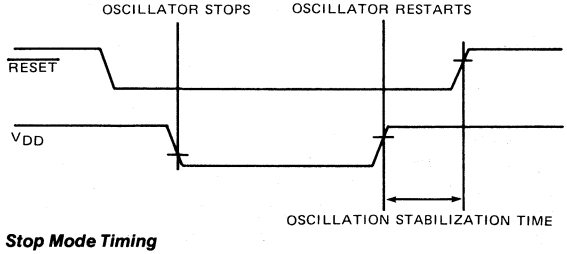
Note: The V_{CC} range under Halt mode must be maintained at +5V ± 10%, as in normal operation.

Stop Mode

Stop mode provides additional power consumption savings over the Halt mode of operation. Stop mode is initiated by forcing V_{DD} to the low state during a $\overline{RESET}$ low. While in Stop mode, oscillator operation is discontinued and only the contents of RAM are maintained.

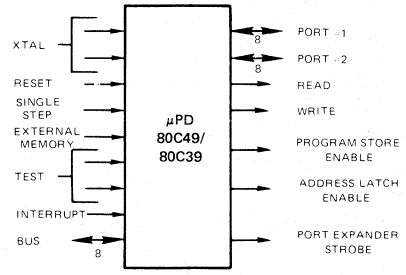
The μPD80C49 is released from Stop mode when V_{DD} is forced high during a $\overline{RESET}$ low. Clock generation is then restarted. When oscillator stabilization is achieved, $\overline{RESET}$ is pulled high and the program is restarted from location 0.

To ensure reliable Stop mode operation, V_{DD} must be brought back up to +5V ± 10%, when releasing the Stop mode. The V_{DD} pin must be protected against noise conditions since it controls oscillator operation. In the Stop mode, V_{CC} may be dropped as low as 2.0 volts to ensure RAM data retention (V_{CC} DR). $\overline{RESET}$ must be held low after oscillation stops until the oscillator is restarted.



Stop Mode Timing

Logic Symbol



Symbol Definitions:

Symbol	Description
A	Accumulator
AC	Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 — 7)
BS	Bank Switch
Bus	Bus Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
P_p	Port Designator (p = 1, 2 or 4 — 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 — 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T0, T1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
S	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
—	Replaced By

Instruction Set

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator																
ADD, A = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0	0	0	0	0	0	1	1	2	2	•			
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
Add A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add indirect the contents of the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, = data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator.	0	0	0	1	0	0	1	1	2	2	•			
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, = data	(A) ← (A) AND data	Logical AND specified immediate Data with Accumulator.	0	1	0	1	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical AND contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical AND indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	Clear the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		Decimal Adjust the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	Decrement by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	0	1	0	0	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 - 6	Rotate Accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 - 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1), N = 0 - 6 (A_7) ← (A_0)	Rotate Accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 - 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ⇄ (A_0-3)	Swap the two 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1	1	0	1	0	0	1	1	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 - 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 - 1	Logical XOR indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) - 1; r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents.	1	1	1	0	1	r	r	r	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JBb addr	(PC 0 - 7) ← addr if Bb = 1 (PC) - (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2	b_1	b_0	1	0	0	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1	1	1	1	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JF 0 addr	(PC 0 - 7) ← addr if FO = 1 (PC) ← (PC) + 2 if FO = 0	Jump to specified address if Flag F 0 is set.	1	0	1	1	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JF 1 addr	(PC 0 - 7) ← addr if F 1 = 1 (PC) ← (PC) + 2 if F 1 = 0	Jump to specified address if Flag F 1 is set.	0	1	1	1	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JMP addr	(PC 8 - 10) ← addr 8 – 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10}	a_9	a_8	0	0	1	0	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JMPP @ A	(PC 0 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1	1	1	0	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
JNI addr	(PC 0 7) ← addr if I = 0 (PC) ← (PC) + 2 if I=1	Jump to specified address if interrupt is low.	1	0	0	0	0	1	1	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						

Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Branch (Cont.)																
JNT0 addr	(PC 0 - 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 - 7) ←addr if T1 = 0 (PC) ←(PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 - 7) ←addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified addres if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 - 7) ←addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 - 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) - 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENTO CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MBO	(DBF) ← 0	Select Bank 0 (locations 0 - 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 - 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 - 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 - 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
HALT		Initiate Halt State.	0	0	0	0	0	0	0	1	1	1				
Data Moves																
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, = data	(Rr) ← data; r = 0 - 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A), r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, = data	((Rr)) ← data; r = 0 - 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 - 7) ← (A) (PC 8 - 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A), r = 0 - 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4 bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement of Flag F 1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Input/Output																
ANL BUS, = data	(BUS) ← (BUS) AND data	Logical AND immediate specified data with contents of Bus.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL P_p, = data	(P_p) ← (P_p) AND data p = 1 - 2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD P_p, A	(P_p) ← (P_p) AND (A0 - 3) p = 4 - 7	Logical AND contents of Accumulator with designated port (4 - 7).	1	0	0	1	1	1	p	p	2	1				
IN A, P_p	(A) ← (P_p), p = 1 - 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed Bus data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, P_p	(A 0 - 3) ← (P_p); p = 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD P_p, A	(P_p) ← A 0 - 3; p = 4 - 7	Move contents of Accumulator designated port (4 - 7).	0	1	1	1	1	p	p	1	1					
ORL BUS, = data	(BUS) ← (BUS) OR data	Logical OR immediate specified data with contents of Bus.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD P_p, A	(P_p) ← (P_p) OR (A0 - 3) P = 4 - 7	Logical OR contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1				
ORL P_p, = data	(P_p) ← (P_p) OR data p = 1 - 2	Logical OR immediate specified data with designated port (1 - 2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto Bus.	0	0	0	0	0	0	1	0	1	1				
OUTL P_p, A	(P_p) ← (A); p = 1 - 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1				
Registers																
DEC Rr (Rr)	(Rr) ← (Rr) 1; r = 0 - 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1, r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ R	((Rr)) ← ((Rr)) + 1; r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
Subroutine																
Call addr	((SP)) ← (PC), (PSW 4 - 7)	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2				
	(SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF		a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
RET	(SP) ← (SP) 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 - 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
Timer/Counter																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Counter for Timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes:

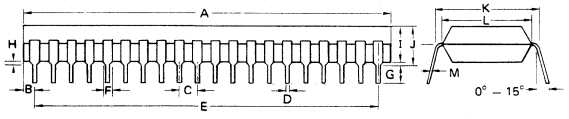
① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

7

Package Outlines
μPD80C49C
μPD80C39C

Plastic

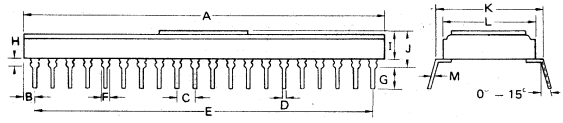
Item	Millimeters	Inches
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600 MAX
L	13.2 MAX	0.520 MAX
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD80C49D
μPD80C39D

Ceramic

Item	Millimeters	Inches
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004



NEC

NEC Electronics U.S.A. Inc.

Microcomputer Division

MICROCOMPUTERS

MICROPROCESSORS **8**

8-BIT N-CHANNEL MICROPROCESSOR COMPLETELY Z80™ COMPATIBLE

DESCRIPTION

The μPD780 and μPD780-1 processors are single-chip microprocessors developed from third-generation technology. Their increased computational power produces higher system through-put and more efficient memory utilization, surpassing that of any second-generation microprocessor. The single voltage requirement of the μPD780 and μPD780-1 processors makes it easy to implement them into a system. All output signals are fully decoded and timed to either standard memory or peripheral circuits. An N-channel, ion-implanted, silicon gate MOS process is utilized in implementing the circuit.

The block diagram shows the functions of the processor and details the internal register structure. The structure contains 26 bytes of Read/Write (R/W) memory available to the programmer. Included in the registers are two sets of six general purpose registers, which may be used individually as 8-bit registers, or as 16-bit register pairs. Also included are two sets of accumulator and flag registers.

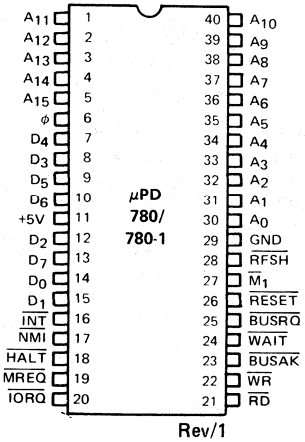
Through a group of exchange instructions the programmer has access to either set of main or alternate registers. The alternate register permits foreground/background mode of operation, or may be used for fast interrupt response. A 16-bit stack pointer is also included in each processor, simplifying implementation of multiple level interrupts, permitting unlimited subroutine nesting, and simplifying many types of data handling.

The two 16-bit index registers simplify implementation of relocatable code and manipulation of tabular data. The refresh register automatically refreshes external dynamic memories. A powerful interrupt response mode uses the I register to form the upper 8 bits of a pointer to an interrupt service address table, while the interrupting apparatus supplies the lower 8 bits of the pointer. An indirect call will then be made to service this address.

FEATURES

- Single Chip, N-Channel Silicon Gate Processor
- 158 Instructions – Including all 78 of the 8080A Instructions, Permitting Total Software Compatibility
- New 4-, 8-, and 16-Bit Operations Featuring Useful Addressing Modes such as Indexed, Bit and Relative
- 17 Internal Registers
- Three Modes of Rapid Interrupt Response, and One Non-Maskable Interrupt
- Directly Connects Standard Speed Dynamic or Static Memories, with Minimum Support Circuitry
- Single-Phase +5 Volt Clock and 5 VDC Supply
- TTL Compatibility
- Automatic Dynamic RAM Refresh Circuitry
- Available in Plastic Package

PIN CONFIGURATION

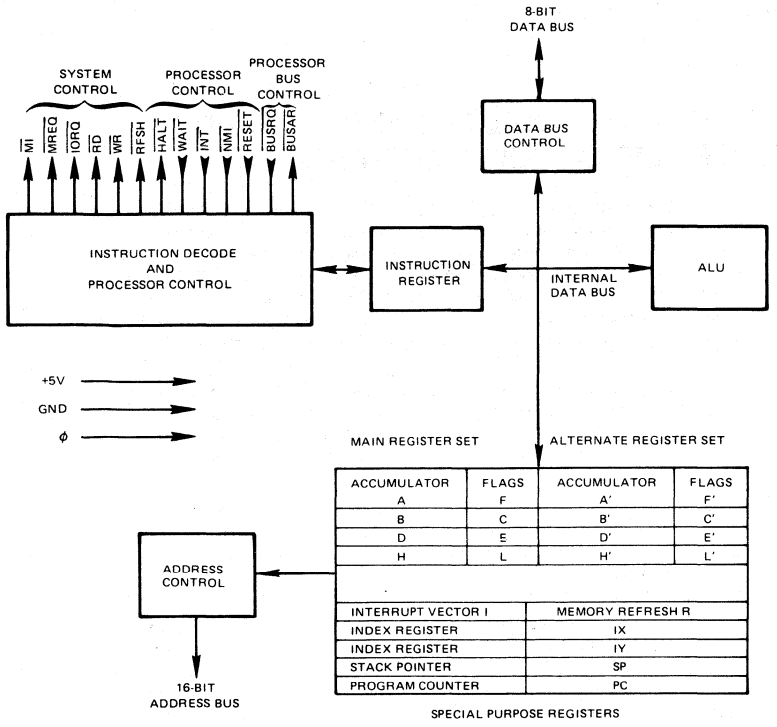


Rev/1

TM: Z80 is a registered trademark of Zilog, Inc.

8

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1-5, 30-40	A_0-A_{15}	Address Bus	3-State Output, active high. Pins A_0-A_{15} constitute a 16-bit address bus, which provides the address for memory and I/O device data exchanges. Memory capacity 65,536 bytes. A_0-A_6 is also needed as refresh cycle.
7-10, 12-15	D_0-D_7	Data Bus	3-State input/output, active high. Pins D_0-D_7 compose an 8-bit, bidirectional data bus, used for data exchanges with memory and I/O devices.
27	$\overline{M_1}$	Machine Cycle One	Output, active low. $\overline{M_1}$ indicates that the machine cycle in operation is the op code fetch cycle of an instruction execution.
19	$\overline{MREQ}$	Memory Request	3-State output, active low. $\overline{MREQ}$ indicates that a valid address for a memory read or write operation is held in the address.
20	$\overline{IORQ}$	Input/Output Request	3-State output, active low. The I/O request signal indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. The $\overline{IORQ}$ signal is also used to acknowledge an interrupt command, indicating that an interrupt response vector can be placed on the data bus.
21	$\overline{RD}$	Read	3-State output, active low. $\overline{RD}$ indicates that the processor is requesting data from memory or an I/O device. The memory or I/O device being addressed should use this signal to gate data onto the data bus.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
22	$\overline{WR}$	Write	3-State output, active low. The memory write signal indicates that the processor data bus is holding valid data to be stored in the addressed, memory or I/O device.
28	$\overline{RFSH}$	Refresh	Output, active low. $\overline{RFSH}$ indicates that a refresh address for dynamic memories is being held in the lower 7-bits of the address bus. The $\overline{MREQ}$ signal should be used to implement a refresh read to all dynamic memories.
18	$\overline{HALT}$	Halt State	Output, active low. $\overline{HALT}$ indicates that the processor has executed a HALT software instruction, and will not resume operation until either a non-maskable or a maskable (with mask enabled) interrupt has been implemented. The processor will execute NOP's while halted, to maintain memory refresh activity.
24	$\overline{WAIT}$	Wait	Input, active low. $\overline{WAIT}$ indicates to the processor that the memory or I/O devices being addressed are not ready for a data transfer. As long as this signal is active, the processor will reenter wait states.
16	$\overline{INT}$	Interrupt Request	Input, active low. The $\overline{INT}$ signal is produced by I/O devices. The request will be honored upon completion of the current instruction, if the interrupt enable flip-flop (IFF) is enabled by the internal software. There are three modes of interrupt response. Mode 0 is identical to 8080 interrupt response mode. The Mode 1 response is a restart location at 0038_H. Mode 2 is for simple vectoring to an interrupt service routine anywhere in memory.
17	$\overline{NMI}$	Non-Maskable Interrupt	Input, active low. The non-maskable interrupt has a higher priority than $\overline{INT}$. It is always acknowledged at the end of the current instruction, regardless of the status of the interrupt enable flip-flop. When the $\overline{NMI}$ signal is given, the μPD780 processor automatically restarts to location 0066_H.
26	$\overline{RESET}$	Reset	Input, active low. The $\overline{RESET}$ signal causes the processor to reset the interrupt enable flip-flop (IFF), clear PC and I and R registers, and set interrupt to 8080A mode. During the reset time, the address bus and data bus go to a state of high impedance, and all control output signals become inactive, after which processing continues at 0000H.
25	$\overline{BUSRQ}$	Bus Request	Input, active low. $\overline{BUSRQ}$ has a higher priority than $\overline{NMI}$, and is always honored at the end of the current machine cycle. It is used to allow other devices to take control over the processor address bus, data bus signals; by requesting that they go to a state of high impedance.
23	$\overline{BUSAK}$	Bus Acknowledge	Output, active low. $\overline{BUSAK}$ is used to inform the requesting device that the processor address bus, data bus and 3-state control bus signals have entered a state of high impedance, and the external device can now take control of these signals.

8

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin	−0.3 to +7 Volts ①
Power Dissipation	1.5W

Note: ① With Respect to Ground.

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage		V_{ILC}	−0.3		0.45	V	
Clock Input High Voltage		V_{IHC}	V_{CC}−0.6		V_{CC}+0.3	V	
Input Low Voltage		V_{IL}	−0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}	V	
Output Low Voltage		V_{OL}			0.4	V	I_{OL} = 1.8 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −250 μA
Power Supply Current	μPD780	I_{CC}			150	mA	t_c = 400 ns
	μPD780-1	I_{CC}		90	200	mA	t_c = 250 ns
Input Leakage Current		I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOH}			10	μA	V_{OUT} = 2.4 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOL}			−10	μA	V_{OUT} = 0.4 V
Data Bus Leakage Current in Input Mode		I_{LD}			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ			35	pF	f_c = 1 MHz
Input Capacitance	C_{IN}			5	pF	Unmeasured Pins
Output Capacitance	C_{OUT}			10	pF	Returned to Ground

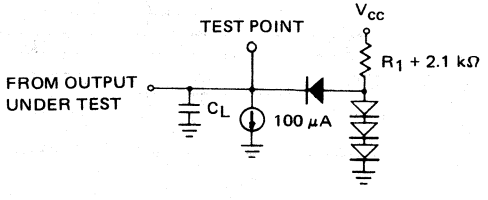
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS μPD780 MIN	LIMITS μPD780 MAX	LIMITS μPD780-1 MIN	LIMITS μPD780-1 MAX	UNIT	TEST CONDITIONS
Clock Period	t_c	0.4	⑫	0.25	⑫	μs	
Clock Pulse Width, Clock High	$t_{w(\Phi H)}$	180	⑬	110	⑬	ns	
Clock Pulse Width, Clock Low	$t_{w(\Phi L)}$	180	2000	110	2000	ns	
Clock Rise and Fall Time	$t_{r,f}$		30		30	ns	
Address Output Delay	$t_{D(AD)}$		145		110	ns	
Delay to Float	$t_{F(AD)}$		110		90	ns	
Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	t_{acm}	①		①		ns	C_L = 50 pF
Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	t_{aci}	②		②		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$	t_{ca}	③		③		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$ During Float	t_{caf}	④		④		ns	
Data Output Delay	$t_{D(D)}$		230		150	ns	
Delay to Float During Write Cycle	$t_{F(D)}$		90		90	ns	
Data Setup Time to Rising Edge of Clock During M1 Cycle	$t_{S\Phi(D)}$	50		35		ns	
Data Setup Time to Falling Edge of Clock During M2 to M5 Cycles	$t_{S\bar{\Phi}(D)}$	60		50		ns	C_L = 200 pF
Data Stable Prior to $\overline{WR}$ (Memory Cycle)	t_{dcm}	⑤		⑤		ns	
Data Stable Prior to $\overline{WR}$ (I/O Cycle)	t_{dci}	⑥		⑥		ns	
Data Stable from $\overline{WR}$	t_{cdf}	⑦		⑦		ns	
Any Hold Time for Setup Time	t_H	0			0	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ Low	$t_{DL\bar{\Phi}(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Rising Edge of Clock to $\overline{MREQ}$ High	$t_{DH\Phi(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ High	$t_{DH\bar{\Phi}(MR)}$		100		85	ns	
Pulse Width, $\overline{MREQ}$ Low	$t_{w(MRL)}$	⑧		⑧		ns	
Pulse Width, $\overline{MREQ}$ High	$t_{w(MRH)}$	⑨		⑨		ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\Phi(IR)}$		90		75	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\bar{\Phi}(IR)}$		110		85	ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ High	$t_{DH\Phi(IR)}$		100		85	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ High	$t_{DH\bar{\Phi}(IR)}$		110		85	ns	C_L = 50 pF
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ Low	$t_{DL\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ Low	$t_{DL\bar{\Phi}(RD)}$		130		95	ns	
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ High	$t_{DH\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ High	$t_{DH\bar{\Phi}(RD)}$		110		85	ns	
$\overline{WR}$ Delay from Rising Edge of Clock to $\overline{WR}$ Low	$t_{DL\Phi(WR)}$		80		65	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ Low	$t_{DL\bar{\Phi}(WR)}$		90		80	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ High	$t_{DH\Phi(WR)}$		100		80	ns	
Pulse Width to $\overline{WR}$ Low	$t_{w(WRL)}$	⑩		⑩		ns	
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ Low	$t_{DL(M1)}$		130		100	ns	C_L = 30 pF
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ High	$t_{DH(M1)}$		130		100	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ Low	$t_{DL(RF)}$		180		130	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ High	$t_{DH(RF)}$		150		120	ns	
$\overline{WAIT}$ Setup Time to Falling Edge of Clock	$t_{S(WT)}$	70		70		ns	
$\overline{HALT}$ Delay Time from Falling Edge of Clock	$t_{D(HT)}$		300		300	ns	C_L = 50 pF
$\overline{INT}$ Setup Time to Rising Edge of Clock	$t_{S(IT)}$	80		80		ns	
Pulse Width, $\overline{NMI}$ Low	$t_{w(NML)}$	80		80		ns	
$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	$t_{S(BQ)}$	80		50		ns	
$\overline{BUSAK}$ Delay from Rising Edge of Clock to $\overline{BUSAK}$ Low	$t_{DL(BA)}$		120		100	ns	C_L = 50 pF
$\overline{BUSAK}$ Delay from Falling Edge of Clock to $\overline{BUSAK}$ High	$t_{DH(BA)}$		110		100	ns	
$\overline{RESET}$ Setup Time to Rising Edge of Clock	$t_{S(RS)}$	90		60		ns	
Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	$t_{F(C)}$		100		80	ns	
$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	t_{mr}	⑪		⑪		ns	

Notes:
① $t_{acm} = t_{w(\Phi H)} + t_f - 65$ (75)*
② $t_{aci} = t_c - 70$ (80)*
③ $t_{ca} = t_{w(\Phi L)} + t_r - 50$ (40)*
④ $t_{caf} = t_{w(\Phi L)} + t_r - 45$ (60)*
⑤ $t_{dcm} = t_c - 170$ (210)*
⑥ $t_{dci} = t_{w(\Phi L)} + t_r - 170$ (210)*
⑦ $t_{cdf} = t_{w(\Phi L)} + t_r - 70$ (80)*
⑧ $t_{w(MRL)} = t_c - 30$ (40)*
⑨ $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 20$ (30)*
⑩ $t_{w(WR)} = t_c - 30$ (40)*
⑪ $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$ (80)*
⑫ $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$
⑬ Though the structure of the 780 is static, 200 μs is a guaranteed maximum.

*These values apply to the μPD780.

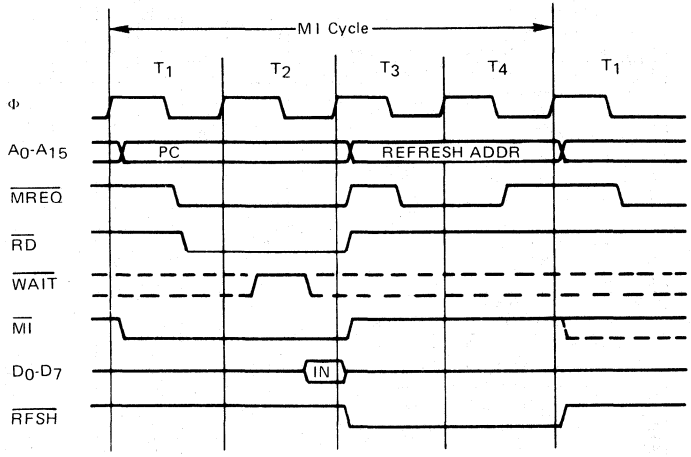


LOAD CIRCUIT FOR OUTPUT

8

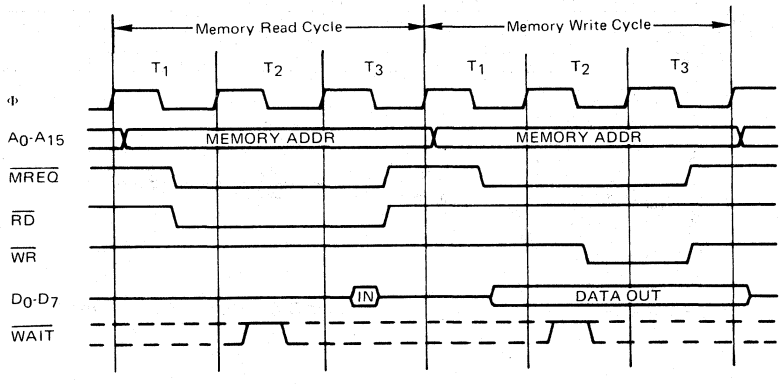
Instruction Op Code Fetch

The contents of the program counter (PC) are placed on the address bus at the start of the cycle. $\overline{MREQ}$ goes active one-half clock cycle later, and the falling edge of this signal can be used directly as a chip enable to dynamic memories. The memory data should be enabled onto the processor data bus when $\overline{RD}$ goes active. The processor takes data with the rising edge of the clock state T_3. The processor internally decodes and executes the instruction, while clock states T_3 and T_4 of the fetch cycle are used to refresh dynamic memories. The refresh control signal $\overline{RFSH}$ indicates that a refresh read should be done to all dynamic memories.



Memory Read or Write Cycles

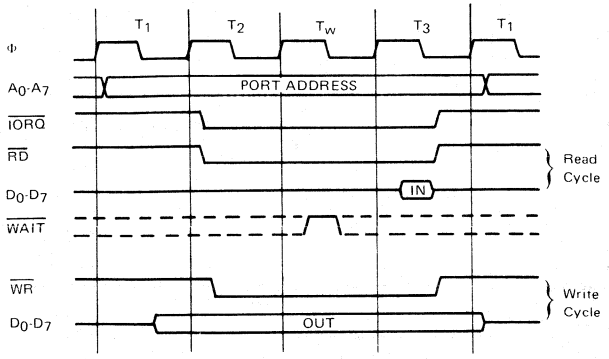
This diagram illustrates the timing of memory read or write cycles other than an op code fetch (M_1 cycle). The function of the $\overline{MREQ}$ and $\overline{RD}$ signals is exactly the same as in the op code fetch cycle. When a memory write cycle is implemented, the $\overline{MREQ}$ becomes active and is used directly as a chip enable for dynamic memories, when the address bus is stable. The $\overline{WR}$ line is used directly as a R/W pulse to any type of semiconductor memory, and is active when data on the data bus is stable.



TIMING WAVEFORMS (CONT.)

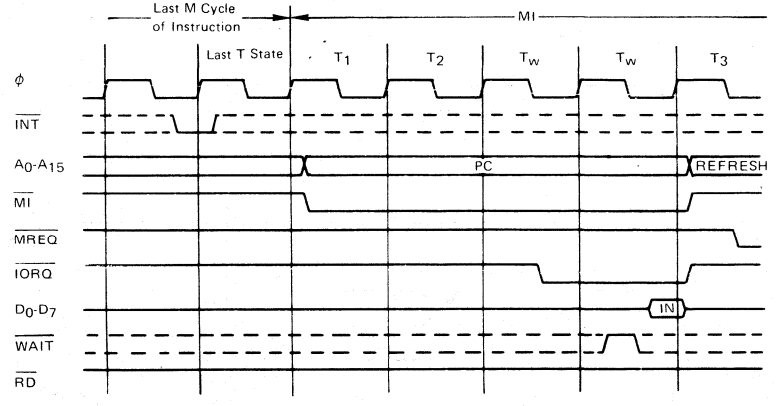
Input or Output Cycles

This illustrates the timing for an I/O read or I/O write operation. A single wait-state (T_W) is automatically inserted in I/O operations to allow sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line, if necessary.



Interrupt Request/Acknowledge Cycle

The processor samples the interrupt signal with the rising edge of the last clock at the end of any instruction. A special M_1 cycle is started when an interrupt is accepted. During the M_1 cycle, the $\overline{IORQ}$ (instead of $\overline{MREQ}$) signal becomes active, indicating that the interrupting device can put an 8-bit vector on the data bus. Two wait states (T_W) are automatically added to this cycle. This makes it easy to implement a ripple priority interrupt scheme.



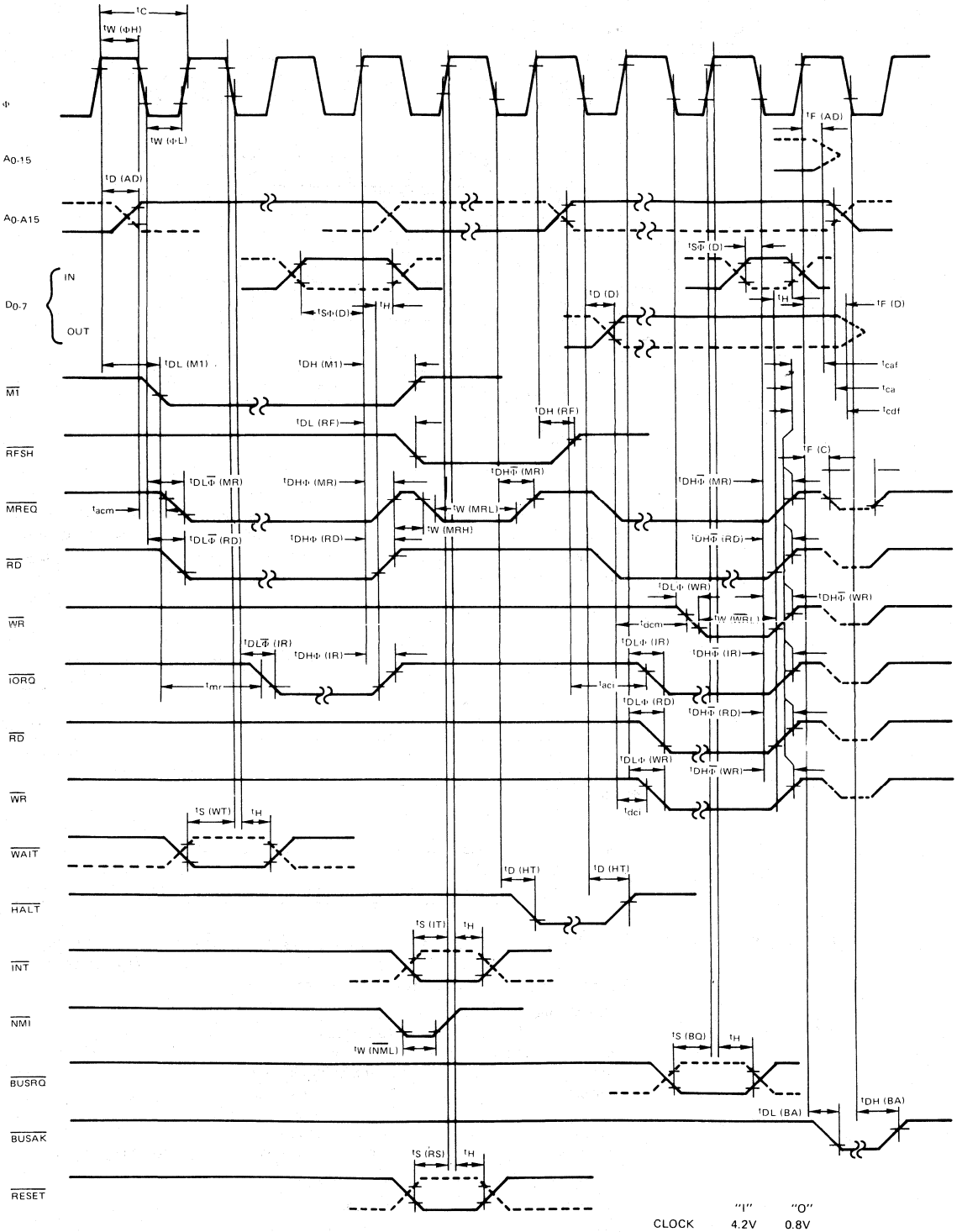
INSTRUCTION SET

The following summary shows the assembly language mnemonic and the symbolic operation performed by the instructions of the μPD780 and μPD780-1 processors. The instructions are divided into 16 categories:

Miscellaneous Group	8-Bit Loads
Rotates and Shifts	16-Bit Loads
Bit Set, Reset and Test	Exchanges
Input and Output	Memory Block Moves
Jumps	Memory Block Searches
Calls	8-Bit Arithmetic and Logic
Restarts	16-Bit Arithmetic
Returns	General Purpose Accumulator and Flag Operations

The addressing Modes include combinations of the following:

Indexed	Immediate
Register	Immediate Extended
Implied	Modified Page Zero
Register Indirect	Relative
Bit	Extended



	"I"	"O"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	±0.5V

Note: ① Timing measurements are made at the following voltages unless otherwise specified:

INSTRUCTION SET TABLE

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
ADC HL, ss	HL ← HL + ss + CY	Add with carry reg. pair ss to HL	1	15	↕	↕	V	↕	0	X	11 101 101 Ⓐ 01 ss1 010
ADC A, r	A ← A + r + CY	Add with carry Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 001 rrr Ⓑ
ADC A,n	A ← A + n + CY	Add with carry value n to ACC		7	↕	↕	V	↕	0	↕	11 001 110 nn nnn nnn
ADC A, (HL)	A ← A + (HL) + CY	Add with carry loc. (HL) to ACC		7	↕	↕	V	↕	0	↕	10 001 110
ADC A, (IX + d)	A ← A + (IX + d) + CY	Add with carry loc. (IX + d) to ACC		19	↕	↕	V	↕	0	↕	11 011 101 10 001 110 dd ddd ddd
ADC A, (IY + d)	A ← A + (IY + d) + CY	Add with carry loc. (IY + d) to ACC		19	↕	↕	V	↕	0	↕	11 111 101 10 001 110 dd ddd ddd
ADD A, n	A ← A + n	Add value n to ACC	2	7	↕	↕	V	↕	0	↕	11 000 110 nn nnn nnn
ADD A, r	A ← A + r	Add Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 000 rrr Ⓑ
ADD A, (HL)	A ← A + (HL)	Add location (HL) to ACC	1	7	↕	↕	V	↕	0	↕	10 000 110
ADD A, (IX + d)	A ← A + (IX + d)	Add location (IX + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 011 101 10 000 110 dd ddd ddd
ADD A, (IY + d)	A ← A + (IY + d)	Add location (IY + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 111 101 10 000 110 dd ddd ddd
ADD HL, ss	HL ← HL + ss	Add Reg. pair ss to HL	1	11	↕	•	•	•	0	X	00 ss 1 001 Ⓐ
ADD IX, pp	IX ← IX + pp	Add Reg. pair pp to IX	2	15	↕	•	•	•	0	X	11 011 101 Ⓒ 00 pp1 001
ADD IY, rr	IY ← IY + rr	Add Reg. pair rr to IY	2	15	↕	•	•	•	0	X	11 111 101 Ⓓ 00 rr1 001
AND r	A ← A∧r	Logical 'AND' of Reg. r ∧ ACC		4	0	↕	P	↕	0	↕	10 100 rrr Ⓑ
AND n	A ← A∧n	Logical 'AND' of value n ∧ ACC		7	0	↕	P	↕	0	↕	11 100 110 nn nnn nnn
AND (HL)	A ← A∧(HL)	Logical 'AND' of loc. (HL) ∧ ACC		7	0	↕	P	↕	0	↕	10 100 110
AND (IX + d)	A ←A∧(IX + d)	Logical 'AND' of loc. (IX + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 011 101 10 100 110 dd ddd ddd
AND (IY + d)	A ←A∧(IY + d)	Logical 'AND' of loc. (IY + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 111 101 10 100 110 dd ddd ddd
BIT b, (HL)	$Z \leftarrow (\overline{HL})_b$	Test BIT b of location (HL)	2	12	•	↕	X	X	0	1	11 001 011 Ⓔ 01 bbb 110
BIT b, (IX + d)	$Z \leftarrow (\overline{IX + d})_b$	Test BIT b at location (IX + d)	4	20	•	↕	X	X	0	1	11 011 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, (IY + d)	$Z \leftarrow (\overline{IY + d})_b$	Test BIT b at location (IY + d)	4	20	•	↕	X	X	0	1	11 111 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, r	$Z \leftarrow \overline{r}_b$	Test BIT of Reg. r	2	8	•	↕	X	X	0	1	11 001 011 ⒷⒺ 01 bbb rrr
CALL cc, nn	If condition cc false continue, else same as CALL nn	Call subroutine at location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 100 Ⓗ nn nnn nnn nn nnn nnn
CALL nn	$(SP - 1) \leftarrow PC_H$ $(SP - 2) \leftarrow PC_L$ PC ← nn	Unconditional call subroutine at location nn	3	17	•	•	•	•	•	•	11 001 101 nn nnn nnn nn nnn nnn
CCF	CY ← CY	Complement carry flag	1	4	↕	•	•	•	0	X	00 111 111
CP r	A − r	Compare Reg. r with ACC		4	↕	↕	V	↕	1	↕	10 111 rrr Ⓑ
CP n	A − n	Compare value n with ACC		7	↕	↕	V	↕	1	↕	11 111 110 nn nnn nnn
CP (HL)	A − (HL)	Compare loc. (HL) with ACC		7	↕	↕	V	↕	1	↕	10 111 110
CP (IX + d)	A − (IX + d)	Compare loc. (IX + d) with ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 111 110 dd ddd ddd
CP (IY + d)		Compare loc. (IY + d) with ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 111 110 dd ddd ddd
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	Compare location (HL) and ACC, decrement HL and BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 101 001
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, decrement HL and BC, repeat until BC = 0	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 111 001

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MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
CPI	A – (HL) HL ← HL + 1 BC ← BC – 1	Compare location (HL) and ACC, increment HL and decrement BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 100 001
CPIR	A – (HL) HL ← HL + 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, increment HL, decrement BC Repeat until BC = C	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 110 001
CPL	A ← A	Complement ACC (1's comp.)	1	4	•	•	•	•	1	1	00 101 111
DAA		Decimal adjust ACC	1	4	↕	↕	P	↕	•	↕	00 100 111
DEC r	r ← r – 1	Decrement Reg. r		4	•	↕	V	↕	1	↕	00 rrr 101Ⓑ
DEC (HL)	(HL) ← (HL) – 1	Decrement loc. (HL)		11	•	↕	V	↕	1	↕	00 110 101
DEC (IX + d)	(IX + d) ← (IX + d) – 1	Decrement loc. (IX + d)		23	•	↕	V	↕	1	↕	11 011 101 00 110 101 dd ddd ddd
DEC (IY + d)	(IY + d) ← (IY + d) – 1	Decrement loc. (IY + d)		23	•	↕	V	↕	1	↕	11 111 101 00 110 101 dd ddd ddd
DEC IX	IX ← IX – 1	Decrement IX	2	10	•	•	•	•	•	•	11 011 101 00 101 011
DEC IY	IY ← IY – 1	Decrement IY	2	10	•	•	•	•	•	•	11 111 101 00 101 011
DEC ss	ss ← ss – 1	Decrement Reg. pair ss	1	6	•	•	•	•	•	•	00 ss1 011Ⓐ
DI	IFF ← 0	Disable interrupts	1	4	•	•	•	•	•	•	11 110 011
DJNZ, e	B ← B – 1 if B = 0 continue if B ≠ 0 PC ← PC + e	Decrement B and jump relative if B = 0	2	8	•	•	•	•	•	•	00 010 000 ◄—e-2—►
EI	IFF ← 1	Enable interrupts	1	4	•	•	•	•	•	•	11 111 011
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	Exchange the location (SP) and HL	1	19	•	•	•	•	•	•	11 100 011
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	Exchange the location (SP) and IX	2	23	•	•	•	•	•	•	11 011 101 11 100 011
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	Exchange the location (SP) and IY	2	23	•	•	•	•	•	•	11 111 101 11 100 011
EX AF, AF'	AF ↔ AF'	Exchange the contents of AF, AF'	1	4	•	•	•	•	•	•	00 001 000
EX DE, HL	DE ↔ HL	Exchange the contents of DE and HL	1	4	•	•	•	•	•	•	11 101 011
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	Exchange the contents of BC, DE, HL with contents of BC', DE', HL', respectively	1	4	•	•	•	•	•	•	11 011 001
HALT	Processor Halted	HALT (wait for interrupt or reset)	1	4	•	•	•	•	•	•	01 110 110
IM 0		Set Interrupt mode 0	2	8	•	•	•	•	•	•	11 101 101 01 000 110
IM 1		Set interrupt mode 1	2	8	•	•	•	•	•	•	11 101 101 01 010 110
IM 2		Set Interrupt mode 2	2	8	•	•	•	•	•	•	11 101 101 01 011 110
IN A, (n)	A ← (n)	Load ACC with input from device n	2	11	•	•	•	•	•	•	11 011 011 nn nnn nnn
IN r, (C)	r ← (C)	Load Reg. r with input from device (C)	2	12	•	↕	P	↕	0	↕	11 101 101Ⓘ 01 rrr 000
INC (HL)	(HL) ← (HL) + 1	Increment location (HL)	1	11	•	↕	V	↕	0	↕	00 110 100
INC IX	IX ← IX + 1	Increment IX	2	10	•	•	•	•	•	•	11 011 101 00 100 011
INC (IX + d)	(IX + d) ← (IX + d) + 1	Increment location (IX + d)	3	23	•	↕	V	↕	0	↕	11 011 101 00 110 100 dd ddd ddd
INC IY	IY ← IY + 1	Increment IY	2	10	•	•	•	•	•	•	11 111 101 00 100 011
INC (IY + d)	(IY + d) ← (IY + d) + 1	Increment location (IY + d)	3	23	•	↕	V	↕	0	↕	11 111 101 00 110 100 dd ddd ddd
INC r	r ← r + 1	Increment Reg. r	1	4	•	↕	V	↕	0	↕	00 rrr 100Ⓑ
INC ss	ss ← ss + 1	Increment Reg. pair ss	1	6	•	•	•	•	•	•	00 ss0 011Ⓐ
IND	(HL) ← (C) B ← B – 1 HL ← HL – 1	Load location (HL) with input from port (C), decrement HL and B	2	16	•	↕③	X	X	1	X	11 101 101 10 101 010

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
INDR	(HL) ← (C) B ← B − 1 HL ← HL − 1 until B = 0	Load location (HL) with input from port (C), decrement HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 111 010
INI	(HL) ← (C) B ← B − 1 HL ← HL + 1	Load location (HL) with input from port (C), and increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 100 010
INIR	(HL) ← (C) B ← B − 1 HL ← HL + 1 until B = 0	Load location (HL) with input from port (C), increment HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 110 010
JP (HL)	PC ← HL	Unconditional jump to (HL)	1	4	•	•	•	•	•	•	11 101 001
JP (IX)	PC ← IX	Unconditional jump to (IX)	2	8	•	•	•	•	•	•	11 011 101 11 101 001
JP (IY)	PC ← IY	Unconditional jump to (IY)	2	8	•	•	•	•	•	•	11 111 101 11 101 001
JP cc, nn	If cc true PC ← nn else continue	Jump to location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 010Ⓗ nn nnn nnn nn nnn nnn
JP nn	PC ← nn	Unconditional jump to location nn	3	10	•	•	•	•	•	•	11 000 011 nn nnn nnn nn nnn nnn
JR C, e	If C = 0 continue If C = 1 PC ← PC + e	Jump relative to PC + e, if carry = 1	2	7 if condition met, 12, if not	•	•	•	•	•	•	00 111 000 ◄— e-2 —►
JR e	PC ← PC + e	Unconditional jump relative to PC + e	2	12	•	•	•	•	•	•	00 011 000 ◄— e-2 —►
JR NC, e	If C = 1 continue If C = 0 PC ← PC + e	Jump relative to PC + e if carry = 0	2	7	•	•	•	•	•	•	00 110 000 ◄— e-2 —►
JR NZ, e	If Z = 1 continue	Jump relative to PC + e if non-zero (Z = 0)	2	7	•	•	•	•	•	•	00 100 000 ◄— e-2 —►
JR Z, e	If Z = 0 continue	Jump relative to PC + e if zero (Z = 1)	2	7	•	•	•	•	•	•	00 101 000 ◄— e-2 —►
LD A, (BC)	A ← (BC)	Load ACC with location (BC)	1	7	•	•	•	•	•	•	00 001 010
LD A, (DE)	A ← (DE)	Load ACC with location (DE)	1	7	•	•	•	•	•	•	00 011 010
LD A, I	A ← I	Load ACC with I	2	9	•	↕	IFF	↕	0	0	11 101 101 01 010 111
LD A, (nn)	A ← (nn)	Load ACC with location nn	3	13	•	•	•	•	•	•	00 111 010 nn nnn nnn nn nnn nnn
LD A, R	A ← R	Load ACC with Reg. R	2	9	•	↕	IFF	↕	0	0	11 101 101 01 011 111
LD (BC), A	(BC) ← A	Load location (BC) with ACC	1	7	•	•	•	•	•	•	00 000 010
LD (DE), A	(DE) ← A	Load location (DE) with ACC	1	7	•	•	•	•	•	•	00 010 010
LD (HL), n	(HL) ← n	Load location (HL) with value n	2	10	•	•	•	•	•	•	00 110 110 nn nnn nnn
LD ss, nn	ss ← nn	Load Reg. pair ss with value nn	4	20	•	•	•	•	•	•	00 ss0 001Ⓐ nn nnn nnn nn nnn nnn
LD HL, (nn)	H ← (nn + 1) L ← (nn)	Load HL with location (nn)	3	16	•	•	•	•	•	•	00 101 010 nn nnn nnn nn nnn nnn
LD (HL), r	(HL) ← r	Load location (HL) with Reg. r	1	7	•	•	•	•	•	•	01 110 rrrⒷ
LD I, A	I ← A	Load I with ACC	2	9	•	•	•	•	•	•	11 101 101 01 000 111
LD IX, nn	IX ← nn	Load IX with value nn	4	19	•	•	•	•	•	•	11 011 101 00 100 001 nn nnn nnn nn nnn nnn
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	Load IX with location (nn)	4	20	•	•	•	•	•	•	11 011 101 00 101 010 nn nnn nnn nn nnn nnn
LD (IX + d), n	(IX + d) ← n	Load location (IX + d) with value n	4	19	•	•	•	•	•	•	11 011 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IX + d), r	(IX + d) ← r	Load location (IX + d) with Reg. r	3	19	•	•	•	•	•	•	11 011 101Ⓑ 01 110 rrr dd ddd ddd

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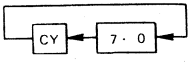
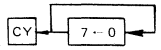
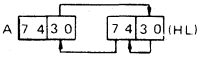
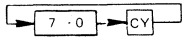
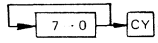
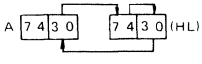
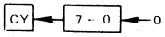
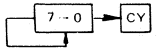
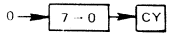
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
LD IY, nn	IY ← nn	Load IY with value nn	4	14	•	•	•	•	•	•	11 111 101 00 100 001 nn nnn nnn nn nnn nnn
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	Load IY with location (nn)	4	20	•	•	•	•	•	•	11 111 101 00 101 010 nn nnn nnn nn nnn nnn
LD ss, (nn)	ss_H ← (nn + 1) ss_L ← (nn)	Load Reg. pair dd with location (nn)	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss1 011 nn nnn nnn nn nnn nnn
LD (IY + d), n	(IY + d) ← n	Load (IY + d) with value n	4	19	•	•	•	•	•	•	11 111 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IY + d), r	(IY + d) ← r	Load location (IY + d) with Reg. r	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 110 rrr dd ddd ddd
LD (nn), A	(nn) ← A	Load location (nn) with ACC	3	13	•	•	•	•	•	•	00 110 010 nn nnn nnn nn nnn nnn
LD (nn), ss	(nn + 1) ← ss_H (nn) ← ss_L	Load location (nn) with Reg. pair dd	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss0 011 nn nnn nnn nn nnn nnn
LD (nn), HL	(nn + 1) ← H (nn) ← L	Load location (nn) with HL	3	16	•	•	•	•	•	•	00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	Load location (nn) with IX	4	20	•	•	•	•	•	•	11 011 101 00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	Load location (nn) with IY	4	20	•	•	•	•	•	•	11 111 101 00 100 010 nn nnn nnn nn nnn nnn
LD R, A	R ← A	Load R with ACC	2	9	•	•	•	•	•	•	11 101 101 01 001 111
LD r, (HL)	r ← (HL)	Load Reg. r with location (HL)	1	7	•	•	•	•	•	•	01 rrr 110 Ⓑ
LD r, (IX + d)	r ← (IX + d)	Load Reg. r with location (IX + d)	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, (IY + d)	r ← (IY + d)	Load Reg. r with location (IY + d)	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, n	r ← n	Load Reg. r with value n	2	7	•	•	•	•	•	•	00 rrr 110 Ⓑ nn nnn nnn
LD, r, r'	r ← r'	Load Reg. r with Reg. r'	1	4	•	•	•	•	•	•	01 rrr rrr Ⓕ
LD SP, HL	SP ← HL	Load SP with HL	1	6	•	•	•	•	•	•	11 111 001
LD SP, IX	SP ← IX	Load SP with IX	2	10	•	•	•	•	•	•	11 011 101 11 111 001
LD SP, IY	SP ← IY	Load SP with IY	2	10	•	•	•	•	•	•	11 111 101 11 111 001
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	Load location (DE) with location (HL), decrement DE, HL and BC	2	16	•	•	↕	•	0	0	11 101 101 10 101 000
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL)	2	21	•	•	0	•	0	0	11 101 101 10 111 000
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	Load location (DE) with location (HL), increment DE, HL; decrement BC	2	16	•	•	↕ Ⓣ	•	0	0	11 101 101 10 100 000
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL), increment DE, HL; decrement BC and repeat until BC = 0	2	21 if BC ≠ 0 16 if BC = 0	•	•	0	•	0	0	11 101 101 10 110 000
NEG	A ← 0 − A	Negate ACC (2's complement)	2	8	↕	↕	V	↕	1	↕	11 101 101 01 000 100

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
NOP		No operation	1	4	•	•	•	•	•	•	00 000 000
OR r	A ← A ∨ r	Logical 'OR' of Reg. r and ACC		4	0	↕	P	↕	0	↕	10 110 rrr (B)
OR n	A ← A ∨ n	Logical 'OR' of value n and ACC		7	•	↕	P	↕	0	↕	11 110 110 nn nnn nnn
OR (HL)	A ← A ∨ (HL)	Logical 'OR' of loc. (HL) and ACC		7	•	↕	P	↕	0	↕	10 110 110
OR (IX + d)	A ← A ∨ (IX + d)	Logical 'OR' of loc. (IX + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 011 101 10 110 110 dd ddd ddd
OR (IY + d)	A ← A ∨ (IY + d)	Logical 'OR' of loc. (IY + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 111 101 10 110 110 dd ddd ddd
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 until B = 0	Load output port (C) with contents of location (HL), decrement HL and B, repeat until B = 0	2	21 if B ≠ 0 16 if B = 0	•	1	X	X	1	X	11 101 101 10 111 011
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 until B = 0	Load output port (C) with location (HL), increment HL, decrement B, repeat until B = 0	2	21 if B ≠ 0 16 if B = 0	•	1	X	X	1	X	11 101 101 10 110 011
OUT (C), r	(C) ← r	Load output port (C) with Reg. r	2	12	•	•	•	•	•	•	11 101 101 (B) 01 rrr 001
OUT (n), A	(n) ← A	Load output port (n) with ACC	2	11	•	•	•	•	•	•	11 010 011 nn nnn nnn
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕ (3)	X	X	1	X	11 101 101 10 101 011
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕ (3)	X	X	1	X	11 101 101 10 100 011
POP IX	IX_H ← (SP + 1) IX_L ← (SP)	Load IX with top of stack	2	14	•	•	•	•	•	•	11 011 101 11 100 001
POP IY	IY_H ← (SP + 1) IY_L ← (SP)	Load IY with top of stack	2	14	•	•	•	•	•	•	11 111 101 11 100 001
POP qq	qq_H ← (SP + 1) qq_L ← (SP)	Load Reg. pair qq with top of stack	1	10	•	•	•	•	•	•	11 qq0 001 (G)
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H	Load IX onto stack	2	15	•	•	•	•	•	•	11 011 101 11 100 101
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H	Load IY onto stack	2	15	•	•	•	•	•	•	11 111 101 11 100 101
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H	Load Reg. pair qq onto stack	1	11	•	•	•	•	•	•	11 qq0 101 (G)
RES b, r	S_b ← 0	Reset Bit b of Reg. r		8	•	•	•	•	•	•	11 001 011 (B) 10 bbb rrr (E)
RES b, (HL)	S_b ← 0, (HL)	Reset Bit b of loc. (HL)		15	•	•	•	•	•	•	11 001 011 10 bbb 110
RES b, (IX + d)	S_b ← 0, (IX + d)	Reset Bit b of loc. (IX + d)		23	•	•	•	•	•	•	11 011 101 11 001 011 dd ddd ddd 10 bbb 110
RES b, (IY + d)	S_b ← 0, (IY + d)	Reset Bit b of loc. (IY + d)		23	•	•	•	•	•	•	11 111 101 11 001 011 dd ddd ddd 10 bbb 110
RET	PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine	1	10	•	•	•	•	•	•	11 001 001
RET cc	If condition cc is false cont. else (PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine if condition cc is true	1	5 if CC false 11 if CC true	•	•	•	•	•	•	11 cc 000 (H)
RETI		Return from interrupt	2	14	•	•	•	•	•	•	11 101 101 01 001 101
RETN		Return from non-maskable interrupt	2	14	•	•	•	•	•	•	11 101 101 01 000 101
RL r		Rotate left through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 010 rrr
RL (HL)		Rotate left through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 010 110
RL (IX + d)		Rotate left through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 010 110
RL (IY + d)	m r, (HL), (IX + d), (IY + d), A	Rotate left through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 010 110
RLA		Rotate left ACC through carry	1	4	↕	•	•	•	0	0	00 010 111

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
RLC (HL)		Rotate location (HL) left circular	2	15	↕	↕	P	↕	0	0	11 001 011 00 000 110
RLC (IX + d)		Rotate location (IX + d) left circular	4	23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 000 110
RLC (IY + d)	 m ≅ r, (HL), (IX + d), (IY + d), A	Rotate location (IY + d) left circular	4	23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 000 110
RLC r		Rotate Reg. r left circular	2	8	↕	↕	P	↕	0	0	11 001 011 (B) 00 000 rrr
RLCA		Rotate left circular ACC	1	4	↕	•	•	•	0	0	00 000 111
RLD		Rotate digit left and right between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 101 111
RR r		Rotate right through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 011 rrr
RR (HL)		Rotate right through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 011 110
RR (IX + d)		Rotate right through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 011 110
RR (IY + d)	 m ≅ r, (HL), (IX + d), (IY + d), A	Rotate right through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 011 110
RRA		Rotate right ACC through carry	1	4	↕	•	•	•	0	0	00 011 111
RRC r		Rotate Reg. r right circular		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 001 rrr
RRC (HL)		Rotate loc. (HL) right circular		4	↕	↕	P	↕	0	0	11 001 011 00 001 110
RRC (IX + d)		Rotate loc. (IX + d) right circular		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 001 110
RRC (IY + d)	m ≅ r, (HL), (IX + d), (IY + d), A	Rotate loc. (IY + d) right circular		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 001 110
RRCA		Rotate right circular ACC	1	4	↕	•	•	•	0	0	00 001 111
RRD		Rotate digit right and left between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 100 111
RST_t	(SP − 1) ← PC_H (SP − 2) ← PC_L PC_H ← 0, PC_L ← T	Restart to location T	1	11	•	•	•	•	•	•	11 ttt 111
SBC A, r	A ← A − r − CY	Subtract Reg. r from ACC w/carry	1	4	↕	↕	V	↕	1	↕	10 011 rrr (B)
SBC A, n	A ← A − n − CY	Subtract value n from ACC with carry		7	↕	↕	V	↕	1	↕	11 011 110 nn nnn nnn
SBC A, (HL)	A ← A − (HL) − CY	Sub. loc. (HL) from ACC w/carry		7	↕	↕	V	↕	1	↕	10 011 110
SBC A, (IX + d)	A ← A − (IX + d) − CY	Subtract loc. (IX + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 011 101 10 011 110 dd ddd ddd
SBC A, (IY + d)	A ← A − (IY + d) − CY	Subtract loc. (IY + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 111 101 10 011 110 dd ddd ddd
SBC HL, ss	HL ← HL − ss − CY	Subtract Reg. pair ss from HL with carry	2	15	↕	↕	V	↕	1	X	11 101 101 (A) 01 ss0 010
SCF	CY ← 1	Set carry flag (C = 1)	1	4	1	•	•	•	0	0	00 110 111
SET b, (HL)	$(HL)_b$ ← 1	Set Bit b of location (HL)	2	15	•	•	•	•	•	•	11 001 011 (E) 11 bbb 110
SET b, (IX + d)	$(IX + d)_b$ ← 1	Set Bit b of location (IX + d)	4	23	•	•	•	•	•	•	11 011 101 (E) 11 001 011 dd ddd ddd 11 bbb 110

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	Set Bit b of location (IY + d)	4	23	•	•	•	•	•	•	11 111 101 Ⓔ 11 001 011 dd ddd ddd 11 bbb 110
SET b, r	$r_b \leftarrow 1$	Set Bit b of Reg. r	2	8	•	•	•	•	•	•	11 001 011 Ⓑ 11 bbb rrr
SLA r		Shift Reg. r left arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 100 rrr
SLA (HL)		Shift loc. (HL) left arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 100 110
SLA (IX + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IX + d) left arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 100 110
SLA (IY + d)		Shift loc. (IY + d) left arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 100 110
SRA r		Shift Reg. r right arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 101 rrr
SRA (HL)		Shift loc. (HL) right arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 101 110
SRA (IX + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IX + d) right arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 101 110
SRA (IY + d)		Shift loc. (IY + d) right arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 101 110
SRL r		Shift Reg. r right logical		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 111 rrr
SRL (HL)		Shift loc. (HL) right logical		15	↕	↕	P	↕	0	0	11 001 011 00 111 110
SRL (IX + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IX + d) right logical		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 111 110
SRL (IY + d)		Shift loc. (IY + d) right logical		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 111 110
SUB r	A ← A − r	Subtract Reg. r from ACC		4	↕	↕	V	↕	1	↕	10 010 rrr Ⓑ
SUB n	A ← A − n	Subtract value n from ACC		7	↕	↕	V	↕	1	↕	11 010 110 nn nnn nnn
SUB (HL)	A ← A − (HL)	Subtract loc. (HL) from ACC		7	↕	↕	V	↕	1	↕	10 010 110
SUB (IX + d)	A ← A − (IX + d)	Subtract loc. (IX + d) from ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 010 110 dd ddd ddd
SUB (IY + d)	A ← A − (IY + d)	Subtract loc. (IY + d) from ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 010 110 dd ddd ddd
XOR r	A ← A∀r	Exclusive 'OR' Reg. r and ACC		4	↕	↕	P	↕	1	↕	10 101 rrr Ⓑ
XOR n	A ← A∀n	Exclusive 'OR' value n and ACC		7	↕	↕	P	↕	1	↕	11 101 110 nn nnn nnn
XOR (HL)	A ← A∀ (HL)	Exclusive 'OR' loc. (HL) and ACC		7	↕	↕	P	↕	1	↕	10 101 110
XOR (IX + d)	A ← A∀ (IX + d)	Exclusive 'OR' loc. (IX + d) and ACC		19	↕	↕	P	↕	1	↕	11 011 101 10 101 110 dd ddd ddd
XOR (IY + d)	A ← A∀ (IY + d)	Exclusive 'OR' loc. (IY + d) and ACC		19	↕	↕	P	↕	1	↕	11 111 101 10 101 110 dd ddd ddd

FLAG NOTES:

① P/V flag is 0 if B-1=0, else P/V=1

② Z=1 if A=(HL), else Z=0

③ If B-1=0, Z flag set, else reset

FLAG DEFINITIONS:

• = Flag not affected

0 = Flag reset

1 = Flag set

X = Flag unknown

↕ = Flag affected according to result of operation

V = Overflow set

P = Parity set

IFF = Interrupt flip-flop set

Ⓐ

Reg	ss
BC	00
DE	01
HL	10
SP	11

Ⓑ

Reg	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓒ

Reg	pp
BC	00
DE	01
IX	10
SP	11

Ⓓ

Reg	rr
BC	00
DE	01
IY	10
SP	11

Ⓔ

Bit	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Ⓕ

Reg	r,r'
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓖ

Reg	qq
BC	00
DE	01
HL	10
AF	11

Ⓗ

CC	Condition		Relevant Flag
000	NZ	Non Zero	Z
001	Z	Zero	Z
010	NC	Non Carry	C
011	C	Carry	C
100	PO	Parity Odd	P/V
101	PE	Parity Even	P/V
110	P	Sign Positive	S
111	M	Sign Negative	S

Ⓘ

Reg	r
B	000
C	001
D	010
E	011
H	100
L	101
F	110
A	111

FLAG DESCRIPTION:

C = Carry/Link
Z = Zero
P/V = Parity/Overflow
S = Sign
N = Add/Subtract
H = Half Carry

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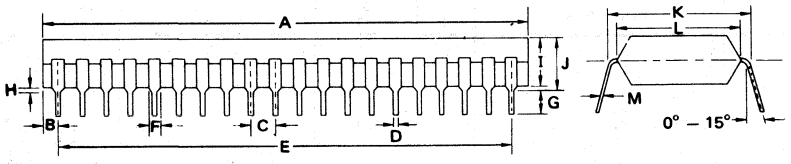


PACKAGE OUTLINE
μ PD780C
μ PD780-1C

(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD8080AF 8-BIT N-CHANNEL MICROPROCESSOR FAMILY

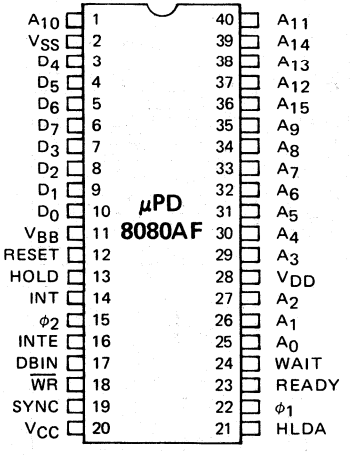
DESCRIPTION

The μPD8080AF is a complete 8-bit parallel processor for use in general purpose digital computer systems. It is fabricated on a single LSI chip using N-channel silicon gate MOS process, which offers much higher performance than conventional microprocessors (1.28 μs minimum instruction cycle). A complete microcomputer system is formed when the μPD8080AF is interfaced with I/O ports (up to 256 input and 256 output ports) and any type or speed of semiconductor memory. It is available in a 40 pin ceramic or plastic package.

FEATURES

- 78 Powerful Instructions
- Three Devices – Three Clock Frequencies
  μPD8080AF – 2.0 MHz
  μPD8080AF-2 – 2.5 MHz
  μPD8080AF-1 – 3.0 MHz
- Direct Access to 64K Bytes of Memory with 16-Bit Program Counter
- 256 8-Bit Input Ports and 256 8-Bit Output Ports
- Double Length Operations Including Addition
- Automatic Stack Memory Operation with 16-Bit Stack Pointer
- TTL Compatible (Except Clocks)
- Multi-byte Interrupt Capability
- **Fully** Compatible with Industry Standard 8080A
- Available in either Plastic or Ceramic Package

PIN CONFIGURATION



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μPD8080AF

FUNCTIONAL DESCRIPTION

The μPD8080AF contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8080AF also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8080AF utilizes a 16-bit address bus to directly address 64K bytes of memory, is TTL compatible (1.9 mA), and utilizes the following addressing modes: Direct; Register; Register Indirect; and Immediate.

The μPD8080AF has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8080AF also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

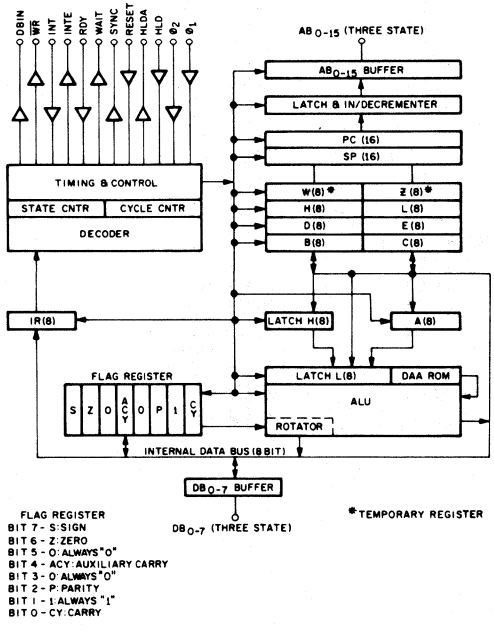
This processor is designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data buses are employed to allow direct interface to memories and I/O ports. Control signals, requiring no decoding, are provided directly by the processor. All buses, including the control bus, are TTL compatible.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address and data lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data buses.

The μPD8080AF has the capability to accept a multiple byte instruction upon an interrupt. This means that a CALL instruction can be inserted so that any address in the memory can be the starting location for an interrupt program. This allows the assignment of a separate location for each interrupt operation, and as a result no polling is required to determine which operation is to be performed.

NEC offers three versions of the μPD8080AF. These processors have all the features of the μPD8080AF except the clock frequency ranges from 2.0 MHz to 3.0 MHz. These units meet the performance requirements of a variety of systems while maintaining software and hardware compatibility with other 8080A devices.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 25-27, 29-40	$A_{15} - A_0$	Address Bus (output three-state)	The address bus is used to address memory (up to 64K 8-bit words) or specify the I/O device number (up to 256 input and 256 output devices). A_0 is the least significant bit.
2	V_{SS}	Ground (input)	Ground
3-10	$D_7 - D_0$	Data Bus (input/ output three-state)	The bidirectional data bus communicates between the processor, memory, and I/O devices for instructions and data transfers. During each sync time, the data bus contains a status word that describes the current machine cycle. D_0 is the least significant bit.
11	V_{BB}	V_{BB} Supply Voltage (input)	−5V ± 5%
12	RESET	Reset (input)	If the RESET signal is activated, the program counter is cleared. After RESET, the program starts at location 0 in memory. The INTE and HLDA flip-flops are also reset. The flags, accumulator, stack pointer, and registers are not cleared. (Note: External synchronization is not required for the RESET input signal which must be active for a minimum of 3 clock periods.)
13	HOLD	Hold (input)	HOLD requests the processor to enter the HOLD state. The HOLD state allows an external device to gain control of the μPD8080AF address and data buses as soon as the μPD8080AF has completed its use of these buses for the current machine cycle. It is recognized under the following conditions: • The processor is in the HALT state. • The processor is in the T_2 or T_W stage and the READY signal is active. As a result of entering the HOLD state, the ADDRESS BUS ($A_{15} - A_0$) and DATA BUS ($D_7 - D_0$) are in their high impedance state. The processor indicates its state on the HOLD ACKNOWLEDGE (HLDA) pin.
14	INT	Interrupt Request (input)	The μPD8080AF recognizes an interrupt request on this line at the end of the current instruction or while halted. If the μPD8080AF is in the HOLD state, or if the Interrupt Enable flip-flop is reset, it will not honor the request.
15	ϕ_2	Phase Two (input)	Phase two of processor clock.
16	INTE ①	Interrupt Enable (output)	INTE indicates the content of the internal interrupt enable flip-flop. This flip-flop is set by the Enable (EI) or reset by the Disable (DI) interrupt instructions and inhibits interrupts from being accepted by the processor when it is reset. INTE is automatically reset (disabling further interrupts) during T_1 of the instruction fetch cycle (M_1) when an interrupt is accepted and is also reset by the RESET signal.
17	DBIN	Data Bus In (output)	DBIN indicates that the data bus is in the input mode. This signal is used to enable the gating of data onto the μPD8080AF data bus from memory or input ports.
18	$\overline{WR}$	Write (output)	$\overline{WR}$ is used for memory WRITE or I/O output control. The data on the data bus is valid while the $\overline{WR}$ signal is active ($\overline{WR}$ = 0).
19	SYNC	Synchronizing Signal (output)	The SYNC signal indicates the beginning of each machine cycle.
20	V_{CC}	V_{CC} Supply Voltage (input)	+5V ± 5%
21	HLDA	Hold Acknowledge (output)	HLDA is in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at: • T_3 for READ memory or input operations. • The clock period following T_3 for WRITE memory or OUTPUT operations. In either case, the HLDA appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.
22	ϕ_1	Phase One (input)	Phase one of processor clock.
23	READY	Ready (input)	The READY signal indicates to the μPD8080AF that valid memory or input data is available on the μPD8080AF data bus. READY is used to synchronize the processor with slower memory or I/O devices. If after sending an address out, the μPD8080AF does not receive a high on the READY pin, the μPD8080AF enters a WAIT state for as long as the READY pin is low. (READY can also be used to single step the processor.)
24	WAIT	Wait (output)	The WAIT signal indicates that the processor is in a WAIT state.
28	V_{DD}	V_{DD} Supply Voltage (input)	+12V ± 5%

Note: ① After the EI instruction, the μPD8080AF accepts interrupts on the second instruction following the EI. This allows proper execution of the RET instruction if an interrupt operation is pending after the service routine.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages ①	-0.3 to +20 Volts
All Input Voltages ①	-0.3 to +20 Volts
Supply Voltages V_{CC}, V_{DD} and V_{SS} ①	-0.3 to +20 Volts
Power Dissipation	1.5W

Note: ① Relative to V_{BB}.

$T_a = 25°C$

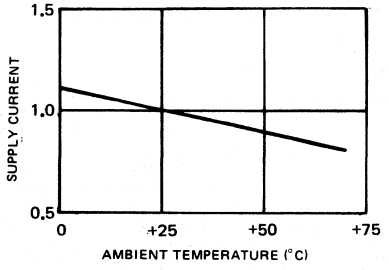
*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage	V_{ILC}	$V_{SS}-1$		$V_{SS}+0.8$	V	
Clock Input High Voltage	V_{IHC}	9.0		$V_{DD}+1$	V	
Input Low Voltage	V_{IL}	$V_{SS}-1$		$V_{SS}+0.8$	V	
Input High Voltage	V_{IH}	3.3		$V_{CC}+1$	V	
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 1.9$ mA on all outputs
Output High Voltage	V_{OH}	3.7			V	$I_{OH} = -150\,\mu A$ ②
Avg. Power Supply Current (V_{DD})	$I_{DD(AV)}$		40	70	mA	t_{CY} min
Avg. Power Supply Current (V_{CC})	$I_{CC(AV)}$		60	80	mA	t_{CY} min
Avg. Power Supply Current (V_{BB})	$I_{BB(AV)}$		0.01	1	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ②	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Clock Leakage	I_{CL}			±10 ②	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
Data Bus Leakage in Input Mode	I_{DL} ①			-100 ②	μA	$V_{SS} \leq V_{IN} \leq V_{SS}+0.8V$
				-2 ②	mA	$V_{SS}+0.8V \leq V_{IN} \leq V_{CC}$
Address and Data Bus Leakage During HOLD	I_{FL}			+10	μA	$V_{ADDR/DATA} = V_{CC}$
				-100 ②		$V_{ADDR/DATA} = V_{SS}+0.45V$

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED ③



Notes: ① When DBIN is high and $V_{IN} > V_{IH}$ internal active pull-up resistors will be switched onto the data bus.
② Minus (–) designates current flow out of the device.
③ ΔI supply/$\Delta T_a = -0.45\%/°C$.

CAPACITANCE

$T_a = 25°C$, $V_{CC} = V_{DD} = V_{SS} = 0V$, $V_{BB} = -5V$.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ		17	25	pF	$f_c = 1$ MHz
Input Capacitance	C_{IN}		6	10	pF	Unmeasured Pins
Output Capacitance	C_{OUT}		10	20	pF	Returned to V_{SS}

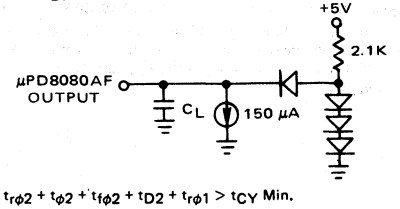
AC CHARACTERISTICS μPD8080AF

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.48		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	220			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	80			nsec	
Address Output Delay From φ2	t_{DA} ②			200	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			220	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	30			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	150			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	120			nsec	
HOLD Setup Time to φ2	t_{HS}	140			nsec	
INT Setup Time During φ2 (During φ1 in Halt Mode)	t_{IS}	120			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

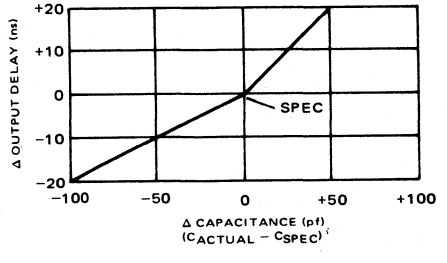
Notes: ① Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.

② Load Circuit.



③ Actual $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} > t_{CY}$ Min.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



AC CHARACTERISTICS
μPD8080AF-1

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.32		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		25	nsec	
φ1 Pulse Width	$t_{\phi1}$	50			nsec	
φ2 Pulse Width	$t_{\phi2}$	145			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	60			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	60			nsec	
Address Output Delay From φ2	t_{DA} ②			150	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			180	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			110	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		130	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	10			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	120			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued:

④ The following are relevant when interfacing the μPD8080AF to devices having V_{IH} = 3.3V.

a. Maximum output rise time from 0.8V to 3.3V = 100 ns at C_L = SPEC.

b. Output delay when measured to 3.0V = SPEC +60 ns at C_L = SPEC.

c. If $C_L \neq$ SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.

AC CHARACTERISTICS
μPD8080AF-2

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.38		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	175			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	70			nsec	
Address Output Delay From φ2	t_{DA} ②			175	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			200	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	20			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	130			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued: ⑤

Device	t_{AW}
μPD8080AF	$2t_{CY} - t_{D3} - t_{r\phi2} - 140$
μPD8080AF-2	$2t_{CY} - t_{D3} - t_{r\phi2} - 130$
μPD8080AF-1	$2t_{CY} - t_{D3} - t_{r\phi2} - 110$

⑥

Device	t_{DW}
μPD8080AF	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-2	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-1	$t_{CY} - t_{D3} - t_{r\phi2} - 150$

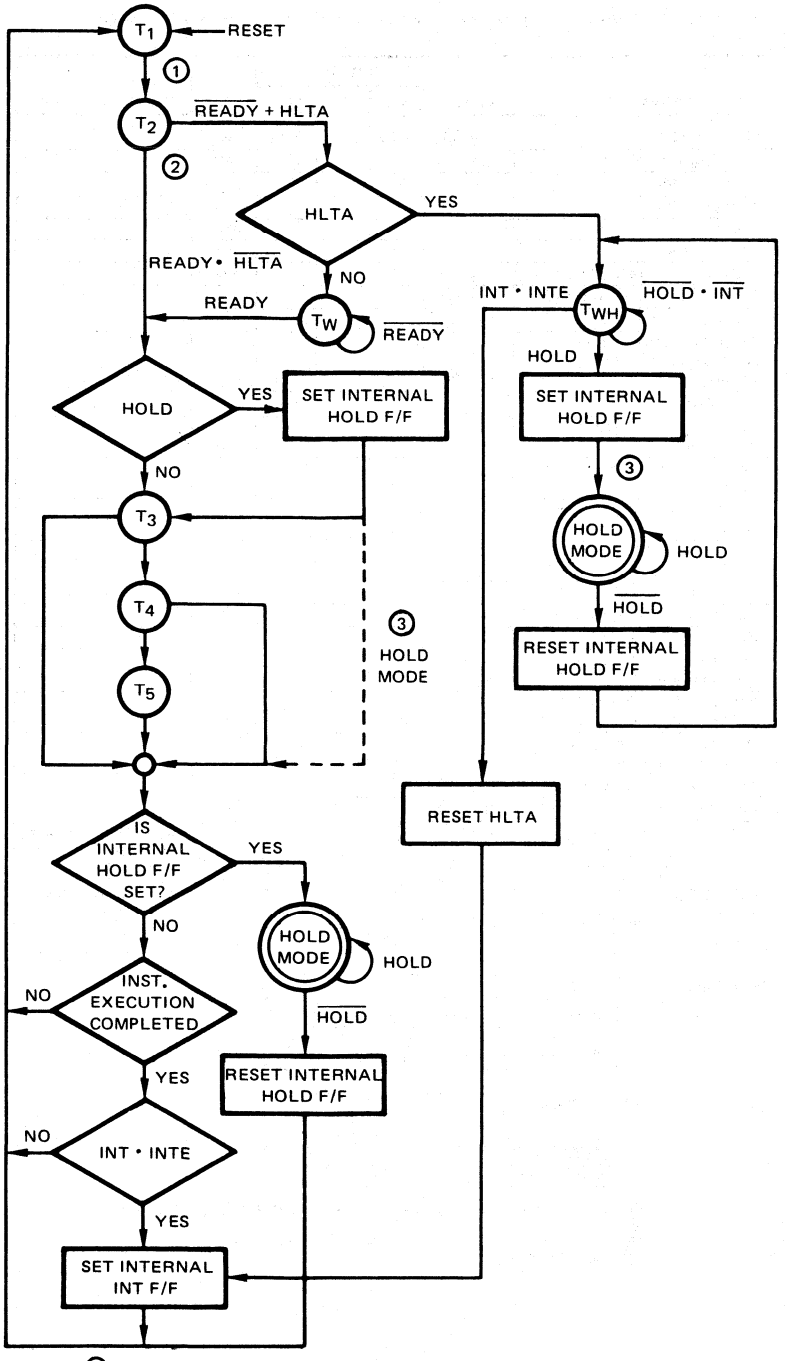
⑦ If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.

⑧ $t_{HF} = t_{D3} + t_{r\phi2} - 50$ ns.

⑨ $t_{WF} = t_{D3} + t_{r\phi2} - 10$ ns.

8

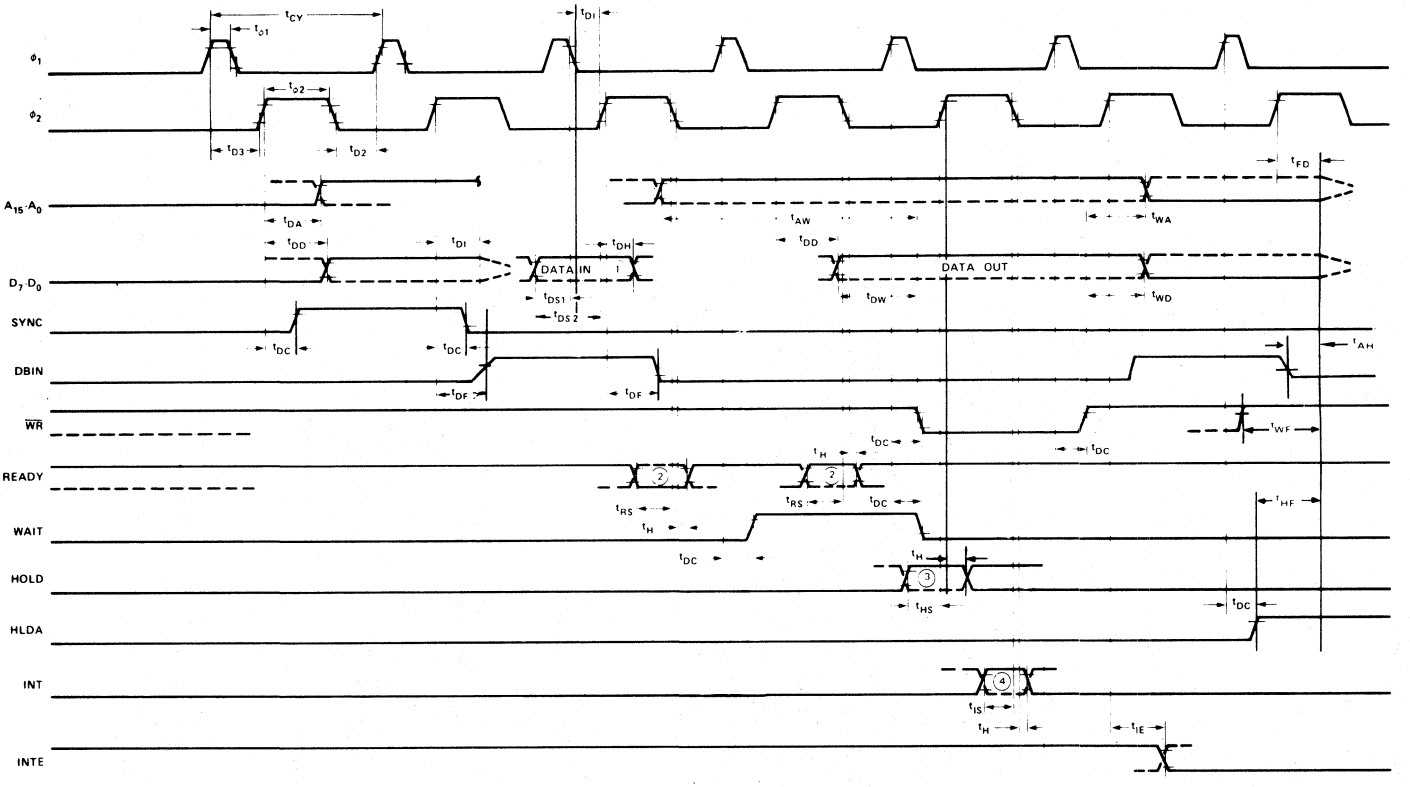
PROCESSOR STATE TRANSITION DIAGRAM



Notes:
1. INTE F/F is reset if internal INT F/F is set.
2. Internal INT F/F is reset if INTE F/F is reset.
3. If required, T_4 and T_5 are completed simultaneously with entering hold state.

TIMING WAVEFORMS (5)

(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



Notes:
(1) Data in must be stable for this period during DBIN • T_3. Both t_{DS1} and t_{DS2} must be satisfied.
(2) Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
(3) Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
(4) Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized in the following instruction. (External synchronization is not required.)
(5) This timing diagram shows timing relationships only; it does not represent any specific machine cycle.
(6) Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V; "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.

INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8080AF has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8080AF. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8080AF instruction set.

The special instruction group completes the μPD8080AF instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the μPD8080AF is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Immediate mode or I/O instructions
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	
Three Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Jump, call or direct load and store instructions
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS OR OPERAND 1	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS OR OPERAND 2	

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	5				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	5	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	5	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	17				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	11/17				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	11/17				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	11/17				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	11/17				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	11/17				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	11/17				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	11/17				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	11/17				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	5/11				
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11				
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11				
RC	Return on carry	1	1	0	1	1	0	0	0	5/11				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11				
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11				
RP	Return on positive	1	1	1	1	0	0	0	0	5/11				
RM	Return on minus	1	1	1	1	1	0	0	0	5/11				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	11				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	11				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	11				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	11				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	5				
INX D	Increment DE	0	0	0	1	0	0	1	1	5				
INX H	Increment HL	0	0	1	0	0	0	1	1	5				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	5				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	5				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	5				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	5				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	5				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	1	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	18				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	5				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	5				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RST A	Restart	1	1	A	A	A	1	1	1	11				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				CY
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	7				

Notes:

[1]Operand Symbols used
- A = 8-bit address or expression
- s = source register
- d = destination register
- PSW = Processor Status Word
- SP = Stack Pointer
- D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
- D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
- ADDR = 16-bit Memory address expression

[2]ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101L – 110 Memory – 111 A.

[3]Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4]• – flag affected
- = flag not affected
0 – flag reset
1 = flag set

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INSTRUCTION CYCLE TIMES

One to five machine cycles (M_1 -- M_5) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$). During ϕ_1 • SYNC of each machine cycle, a status word that identifies the type of machine cycle is available on the data bus.

Execution times and machine cycles used for each type of instruction are shown below.

INSTRUCTION	MACHINE CYCLES EXECUTED	CLOCK TIMES (MIN/MAX)
RST X and PUSH RP	PCR5 ① SPW3 ⑤ SPW3 ⑤	11
All CALL Instructions	PCR5 ① PCR3 ② PCR3 ② SPW3 ⑤ SPW3 ⑤	11/17
Conditional TURN Instructions	PCR5 ① SPR3 ④ SPR3 ④	5/11
RET Instruction	PCR4 ① SPR3 ④ SPR3 ④	10
XTHL	PCR4 ① SPR3 ④ SPR3 ④ SPW3 ⑤ SPW5 ⑤	18
DAD RP	PCR4 ① PCX3 ⓧ PCX3 ⓧ	10
INR R; INX RP, DCR R; DCX RP; PCHL; MOV R, R; SPHL	PCR5 ①	5
All JUMP Instructions and LXI RP	PCR4 ① PCR3 ② PCR3 ②	10
POP RP	PCR4 ① SPR3 ④ SPR3 ④	10
LDA	PCR4 ① PCR3 ② PCR3 ② BBR3 ②	13
STA	PCR4 ① PCR3 ② PCR3 ② BBW3 ③	13
LHLD	PCR4 ① PCR3 ② PCR3 ② BBR3 ② BBR3 ②	16
SHLD	PCR4 ① PCR3 ② PCR3 ② BBW3 ③ BBW3 ③	16
STAX B	PCR4 ① BCW3 ③	7
STAX D	PCR4 ① DEW3 ③	7
LDAX B	PCR4 ① BCR3 ②	7
LDAX D	PCR4 ① DER3 ②	7
MOV R, M; ADD M; ADC M; SUB M; SB B M; ANA M; XRA M; ORA M; CMP M	PCR4 ① HLR3 ②	7
INR M and DCR M	PCR4 ① HLR3 ② HLW3 ③	10
MVI M	PCR4 ① PCR3 ② HLW3 ③	10
MVI R; ADI; ACI; SUI; SBI; ANI; XRI; ORI; CPI	PCR4 ① PCR3 ②	7
MOV M, R	PCR4 ① HLW3 ③	7
EI; DI ADD R; ADC R; SUB R; SBB R; ANA R; XRA R; ORA R; CMP R; RLC; RRC; RAL; RAR; DAA; CMA; STC; CMC; NOP; XCHG	PCR4 ①	4
OUT	PCR4 ① PCR3 ② ABW3 ⑦	10
IN	PCR4 ① PCR3 ② ABR3 ⑥	10
HLT	PCR4 ① PCX3 ⑨	7

Machine Cycle Symbol Definition

XX Y Z (N)
- XX: HL = Registers H and L used as address; BC = Registers B and C used as address; DE = Registers D and E used as address; SP = Stack Pointer used as address; BB = Byte 2 and 3 used as address; AB = Byte 2 used as address
- Y: Status word defining type of machine cycle (See Status Word Chart)
- Z: Number of clocks for this machine cycle
- (N): R = Read cycle – data into processor; W = Write cycle – data out of processor; X = No data transfer; PC = Program Counter used as address

Underlined (XXYZ(N)) indicates machine cycle is executed if condition is True.

STATUS INFORMATION DEFINITION

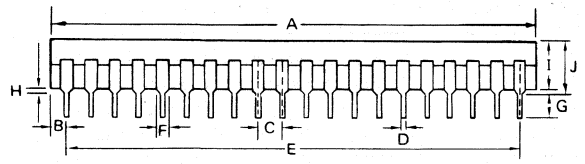
SYMBOLS	DATA BUS BIT	DEFINITION
INTA ①	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart or CALL instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO}$ = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP ①	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR ①	D_7	Designates that the data bus will be used for memory read data.

Note: ① These three status bits can be used to control the flow of data onto the μPD8080AF data bus.

STATUS WORD CHART

TYPE OF MACHINE CYCLE

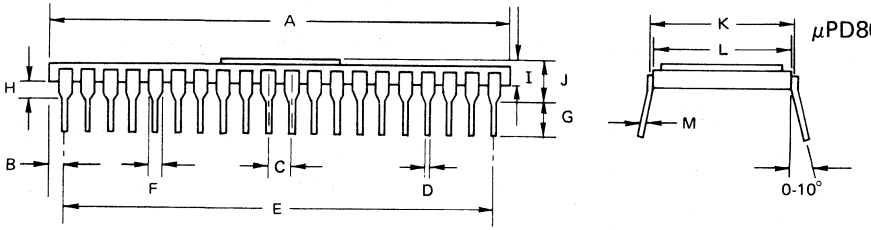
DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INT. ACK. WHILE HALT
											← Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0



PACKAGE OUTLINE
μPD8080AFC

(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62 MAX	0.064 MAX
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24 TYP	0.600 TYP
L	13.2 TYP	0.520 TYP
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8080AFD

(CERAMIC)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

μPD8085A SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

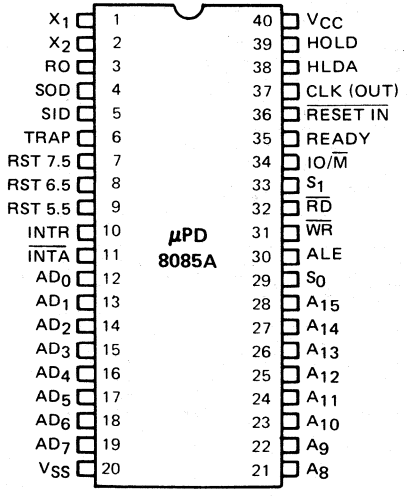
DESCRIPTION

The μPD8085A is a single chip 8-bit microprocessor which is 100 percent software compatible with the industry standard 8080A. It has the ability of increasing system performance of the industry standard 8080A by operating at a higher speed. Using the μPD8085A in conjunction with its family of ICs allows the designer complete flexibility with minimum chip count.

FEATURES

- Single Power Supply: +5 Volt, ±10%
- Internal Clock Generation and System Control
- Internal Serial In/Out Port.
- Fully TTL Compatible
- Internal 4-Level Interrupt Structure
- Multiplexed Address/Data Bus for Increased System Performance
- Complete Family of Components for Design Flexibility
- Software Compatible with Industry Standard 8080A
- Higher Throughput: μPD8085A — 3 MHz
  μPD8085A-2 — 5 MHz
- Available in Either Plastic or Ceramic Package

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The μPD8085A contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8085A also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8085A has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8085A also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

The μPD8085A was designed with speed and simplicity of the overall system in mind. The multiplexed address/data bus increases available pins for advanced functions in the processor and peripheral chips while providing increased system speed and less critical timing functions. All signals to and from the μPD8085A are fully TTL compatible.

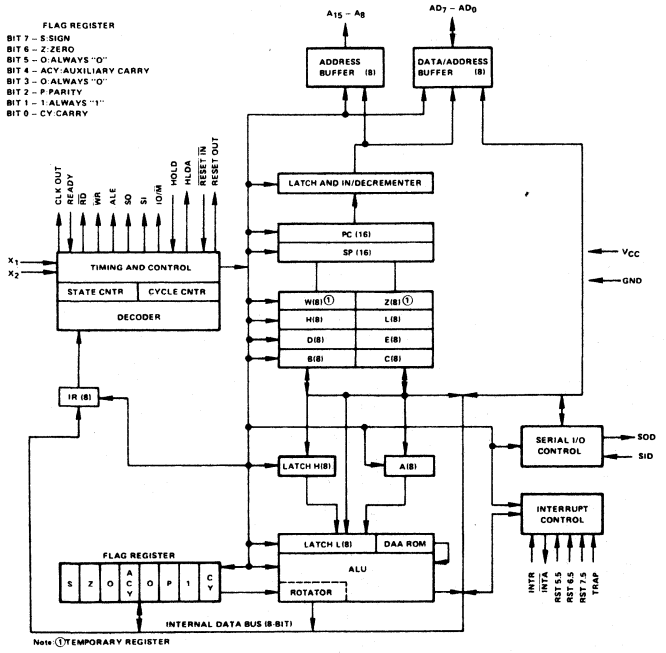
The internal interrupt structure of the μPD8085A features 4 levels of prioritized interrupt with three levels internally maskable.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address, data and control lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8085A features internal clock generation with status outputs available for advanced read/write timing and memory/IO instruction indications. The clock may be crystal controlled, RC controlled, or driven by an external signal.

On chip serial in/out port is available and controlled by the newly added RIM and SIM instructions.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2	X_1, X_2	Crystal In	Crystal, RC, or external clock input
3	RO	Reset Out	Acknowledge that the processor is being reset to be used as a system reset
4	SOD	Serial Out Data	1-bit data out by the SIM instruction
5	SID	Serial In Data	1-bit data into ACC bit 7 by the RIM instruction
6	Trap	Trap Interrupt Input	Highest priority nonmaskable restart interrupt
7 8 9	RST 7.5 RST 6.5 RST 5.5	Restart Interrupts	Priority restart interrupt inputs, of which 7.5 is the highest and 5.5 the lowest priority
10	INTR	Interrupt Request In	A general interrupt input which stops the PC from incrementing, generates $\overline{INTA}$, and samples the data bus for a restart or call instruction
11	$\overline{INTA}$	Interrupt Acknowledge	An output which indicates that the processor has responded to INTR
12-19	$AD_0 - AD_7$	Low Address/Data Bus	Multiplexed low address and data bus
20	V_{SS}	Ground	Ground Reference
21-28	$A_8 - A_{15}$	High Address Bus	Nonmultiplexed high 8-bits of the address bus
29, 33	S_0, S_1	Status Outputs	Outputs which indicate data bus status: Halt, Write, Read, Fetch
30	ALE	Address Latch Enable Out	A signal which indicates that the lower 8-bits of address are valid on the AD lines
31, 32	$\overline{WR}, \overline{RD}$	Write/Read Strobes Out	Signals out which are used as write and read strobes for memory and I/O devices
34	IO/$\overline{M}$	I/O or Memory Indicator	A signal out which indicates whether $\overline{RD}$ or $\overline{WR}$ strobes are for I/O or memory devices
35	Ready	Ready Input	An input which is used to increase the data and address bus access times (can be used for slow memory)
36	$\overline{Reset\ In}$	Reset Input	An input which is used to start the processor activity at address 0, resetting IE and HLDA flip-flops
37	CLK	Clock Out	System Clock Output
38, 39	HLDA, HOLD	Hold Acknowledge Out and Hold Input Request	Used to request and indicate that the processor should relinquish the bus for DMA activity. When hold is acknowledged, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, Address and Data busses are all 3-stated.
40	V_{CC}	5V Supply	Power Supply Input

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.3 to +7 Volts
All Input Voltages	−0.3 to +7 Volts
Supply Voltage V_{CC}	−0.3 to +7 Volts
Power Dissipation	1.5W

$T_a = 25°C$; $V_{CC} = \pm5V \pm 5\%$, 8085A-2

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, $V_{SS} = GND$, unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	$V_{SS} - 0.5$		$V_{SS} + 0.8$	V	
Input High Voltage	V_{IH}	2.0		$V_{CC} + 0.5$	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA on all outputs
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -400\ \mu s$ ①
Power Supply Current (V_{CC})	I_{CC} (AV)			170	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ①	μA	$V_{IN} = V_{CC}$
Output Leakage	I_{LO}			±10 ①	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
Input Low Level, Reset	V_{ILR}	−0.5		+0.8	V	
Input High Level, Reset	V_{IHR}	2.4		$V_{CC} + 0.5$	V	
Hysteresis, Reset	V_{HY}	0.25			V	

Note: ① Minus (−) designates current flow out of the device.

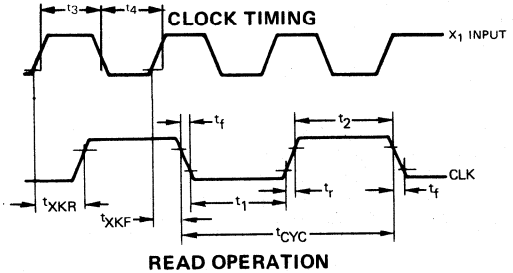
AC CHARACTERISTICS

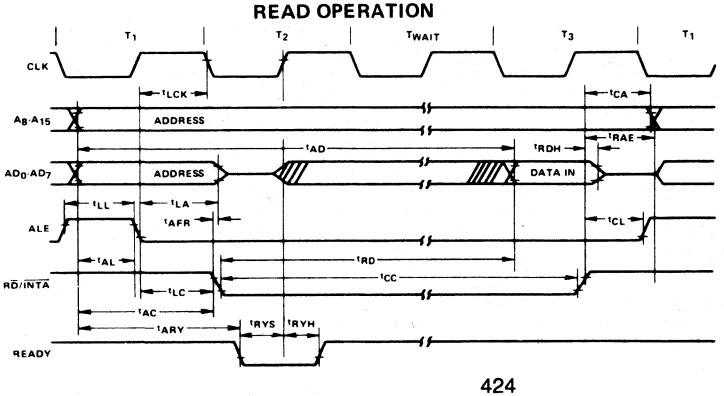
T_a = 0°C to +70°C; V_{CC} = 5V ± 5%, 8085A-2

PARAMETER	SYMBOL	LIMITS μPD8085A MIN	LIMITS μPD8085A MAX	LIMITS μPD8085A-2 MIN	LIMITS μPD8085A-2 MAX	UNIT	TEST CONDITIONS
CLK Cycle Period	T_{CYC}	320	2000	200	2000	ns	
CLK Low Time	t_1	80		40		ns	
CLK High Time	t_2	120		70		ns	
CLK Rise and Fall Time	t_r, t_f		30		30	ns	T_{CYC} = 320 ns C_L = 150 pF
Address Hold Time After ALE	t_{LA}	100		50		ns	
ALE Width	t_{LL}	140		80		ns	
ALE Low During CLK High	t_{LCK}	100		50		ns	
Training Edge of ALE to Leading Edge of Control	t_{LC}	130		60		ns	Output Voltages V_L = 0.8 Volts V_H = 2.0 Volts
Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)	t_{AFR}		0		0	ns	
Valid Address to Valid Data In	t_{AD}		575		350	ns	
$\overline{READ}$ (or $\overline{INTA}$) to Valid Data	t_{RD}		300		150	ns	Input Voltages V_L = 0.8 Volts V_H = 1.5 Volts at 20 ns rise and fall times
Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)	t_{RDH}	0		0		ns	
Training Edge of READ to Re-Enabling of Address	t_{RAE}	150		90		ns	
Address (A_8-A_{15}) Valid After Control ①	t_{CA}	120		60		ns	
Data Valid to Training Edge of $\overline{WRITE}$	t_{DW}	420		230		ns	For outputs where C_L = 150 pf, correct as follows: 25 pf ≤ CL < 150 pf −0.10 ns/pf
Data Valid After Training Edge of $\overline{WRITE}$	t_{WD}	100		60		ns	
Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	t_{CC}	400		230		ns	
Training Edge of Control to Leading Edge of ALE	t_{CL}	50		25		ns	
READY Valid from Address Valid	t_{ARY}		220		100	ns	
READY Setup Time to Leading Edge of CLK	t_{RYS}	110		100		ns	150 pf < CL ≤ 300 pf + 0.30 ns/pf
READY Hold Time	t_{RYH}	0		0		ns	
HLDA Valid to Training Edge of CLK	t_{HACK}	110		40		ns	
Bus Float After HLDA	t_{HABF}		210		150	ns	Outputs measured with only capacitive load
HLDA to Bus Enable	t_{HABE}		210		150	ns	
ALE to Valid Data In	t_{LDR}		460		270	ns	
Control Training Edge to Leading Edge of Next Control	t_{RV}	400		220		ns	
Address Valid to Leading Edge of Control	t_{AC}	270		115		ns	
HOLD Setup Time to Training Edge of CLK	t_{HDS}	170		120		ns	
HOLD Hold Time	t_{HDH}	0		0		ns	
INTR Setup Time to Leading Edge of CLK (M1, T1 only). Also RST and TRAP	t_{INS}	160		150		ns	
INTR Hold Time	t_{INH}	0		0		ns	
X Falling to CLK Rising	t_{XKR}	30	120	30	100	ns	
X_1 Falling to CLK Falling	t_{XKF}	30	150	30	110	ns	
Leading Edge of Write to Data Valid	t_{WDL}		40		20		
A_{8-15} Valid Before Trailing Edge of ALE	t_{AL}	115		50		ns	
A_{0-7} Valid Before Trailing Edge of ALE	t_{ALL}	90		50		ns	
ALE to Valid Data During Write	t_{LDW}		200		120	ns	
ALE to READY Stable	t_{LRY}		110		30	ns	
A_{0-7} Valid to Leading Edge of Control	t_{ACL}	240		115		ns	
Minimum Clock in Low-High Time	t_3, t_4	64		40		ns	

Note: ① IO/$\overline{M}$, SO, SI

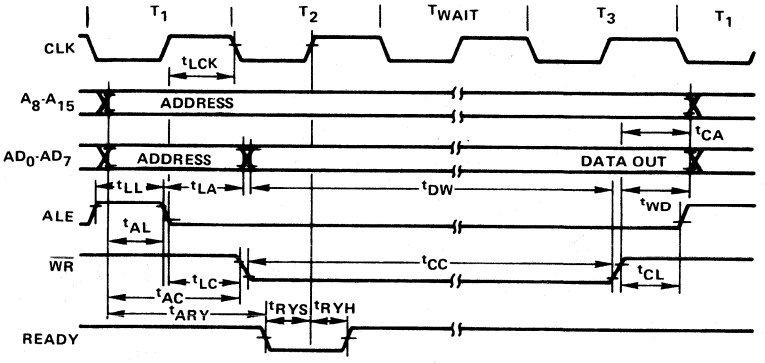
TIMING WAVEFORMS





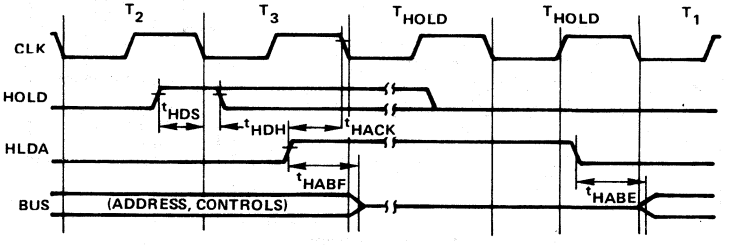
TIMING WAVEFORMS (CONT.)

WRITE OPERATION

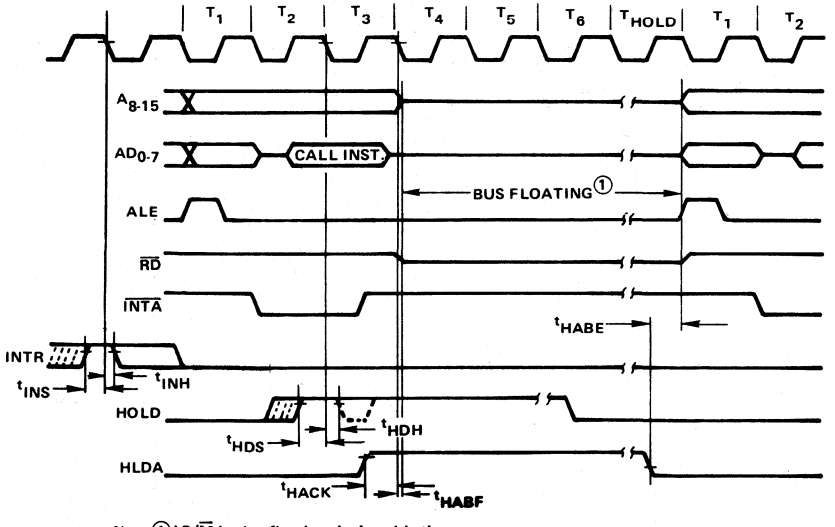


Note: READY must remain stable during setup and hold time.

HOLD OPERATION

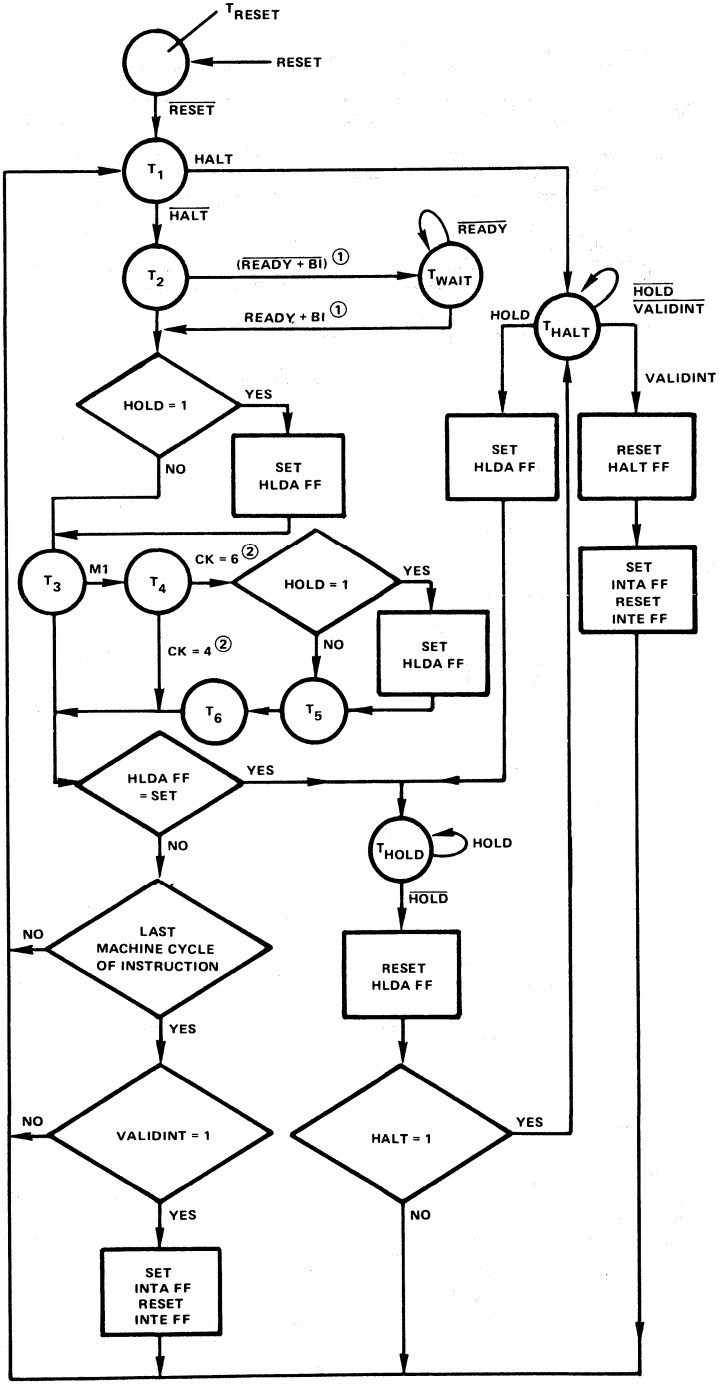


INTERRUPT TIMING



Note: ① IO/$\overline{M}$ is also floating during this time.

PROCESSOR STATE TRANSITION DIAGRAM



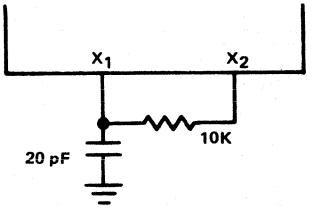
Notes: ① BI indicates that the bus is idle during this machine cycle.

② CK indicates the number of clock cycles in this machine cycle.

CLOCK INPUTS ①

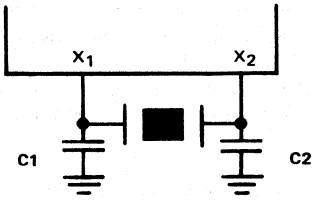
As stated, the timing for the μPD8085A may be generated in one of three ways; crystal, RC, or external clock. Recommendations for these methods are shown below.

RC



≈3 MHz Input Frequency
RC Resonance

CRYSTAL

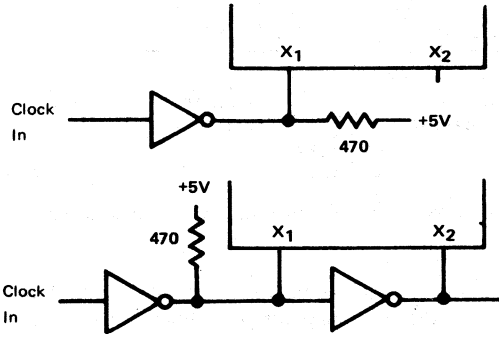


1-6 MHz Input Frequency
Parallel Resonant Crystal

For 1-6 MHz Input Frequency,
C1 = C2 = 10 pF max.

For 6-10 MHz Input Frequency,
C1 = C2 = 5 pF max.

EXTERNAL



1-6 MHz 25-50% DC
X_2 not used

1-6 MHz > 50% DC

Note: ① Input frequency must be twice the internal operating frequency.

STATUS OUTPUTS

The Status Outputs are valid during ALE time and have the following meaning:

	S1	S0
Halt	0	0
Write	0	1
Read	1	0
Fetch	1	1

These pins may be decoded to portray the processor's data bus status.

INTERRUPTS

The μPD8085A has five interrupt pins available to the user. INTR is operationally the same as the 8080 interrupt request, three (3) internally maskable restart interrupts: RESTART 5.5, 6.5 and 7.5, and TRAP, a non-maskable restart.

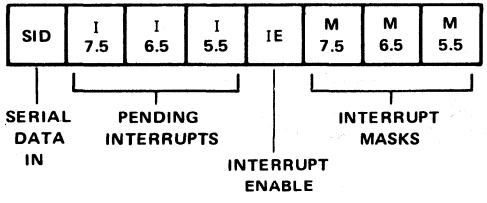
PRIORITY	INTERRUPT	RESTART ADDRESS
Highest	TRAP	24_{16}
|	RST 7.5	$3C_{16}$
|	RST 6.5	34_{16}
|	RST 5.5	$2C_{16}$
Lowest	INTR	

INTR, RST 5.5 and RST 6.5 are all level sensing inputs while RST 7.5 is set on a rising edge. TRAP, the highest priority interrupt, is non-maskable and is set on the rising edge or positive level. It must make a low to high transition and remain high to be seen, but it will not be generated again until it makes another low to high transition.

SERIAL I/O

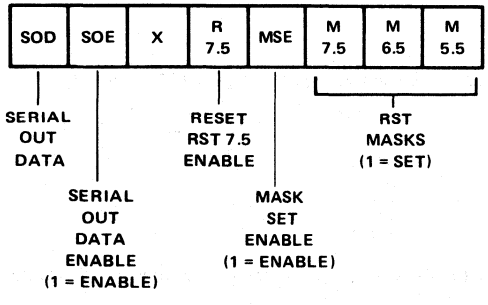
Serial input and output is accomplished with two new instructions not included in the 8080: RIM and SIM. These instructions serve several purposes: serial I/O, and reading or setting the interrupt mask.

The RIM (Read Interrupt Mask) instruction is used for reading the interrupt mask and for reading serial data. After execution of the RIM instruction the ACC content is as follows:



Note: After the TRAP interrupt, the RIM instruction must be executed to preserve the status of IE.

The SIM (Set Interrupt Mask) instruction is used to program the interrupt mask and to output serial data. Presetting the ACC for the SIM instruction has the following meaning:



INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also, the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8085A has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8085A. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8085A instruction set.

Two instructions, RIM and SIM, are used for reading and setting the internal interrupt mask as well as input and output to the serial I/O port.

The special instruction group completes the μPD8085A instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

8

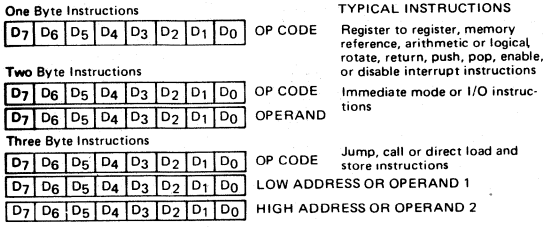
DATA AND INSTRUCTION FORMATS

Data in the μPD8085A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.



INSTRUCTION SET TABLE

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	4				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	4	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	4	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR Memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	7/10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	7/10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	7/10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	7/10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	7/10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	7/10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	7/10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	7/10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	18				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	9/18				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	9/18				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	9/18				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	9/18				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	9/18				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	9/18				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	9/18				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	9/18				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	6/12				
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12				
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12				
RC	Return on carry	1	1	0	1	1	0	0	0	6/12				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12				
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12				
RP	Return on positive	1	1	1	1	0	0	0	0	6/12				
RM	Return on minus	1	1	1	1	1	0	0	0	6/12				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	12				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	12				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	12				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	6				
INX D	Increment DE	0	0	0	1	0	0	1	1	6				
INX H	Increment HL	0	0	1	0	0	0	1	1	6				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	6				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	6				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	6				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	6				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	6				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	16				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	6				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	6				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4				
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4				
RST A	Restart	1	1	A	A	A	1	1	1	12				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				CY
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	5				

Notes:

[1] Operand Symbols used
- A = 8-bit address or expression
- s = source register
- d = destination register
- PSW = Processor Status Word
- SP = Stack Pointer
- D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
- D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
- ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.

[3] Two possible cycle times (7/10) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
- = flag not affected
- 0 = flag reset
- 1 = flag set

INSTRUCTION CYCLE TIMES

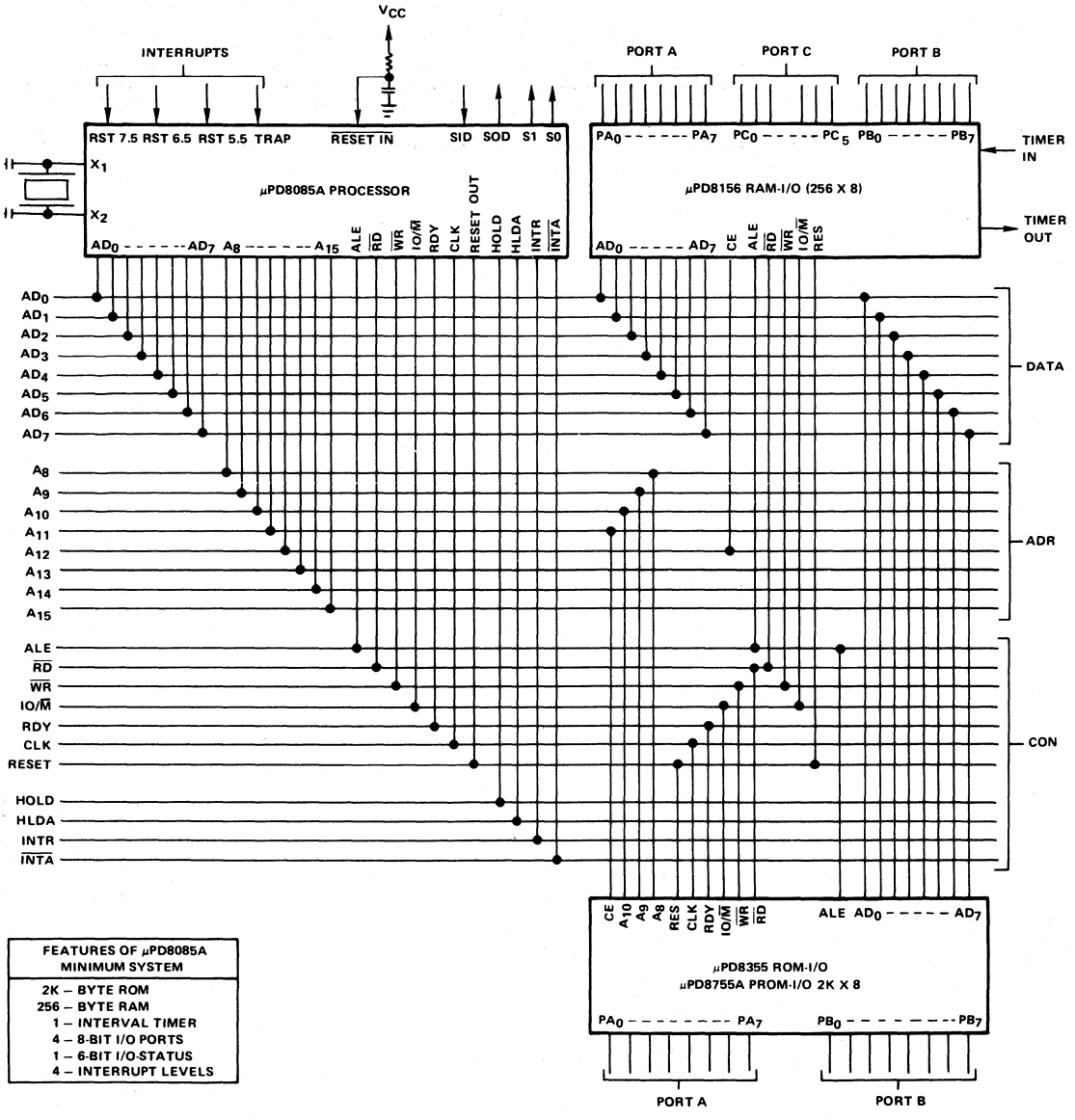
One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$).

Machine cycles and clock states used for each type of instruction are shown below.

INSTRUCTION TYPE	MACHINE CYCLES EXECUTED MIN/MAX	CLOCK STATUS MIN/MAX
ALU R	1	4
CMC	1	4
CMA	1	4
DAA	1	4
DCR R	1	4
DI	1	4
EI	1	4
INR R	1	4
MOV R, R	1	4
NOP	1	4
ROTATE	1	4
RIM	1	4
SIM	1	4
STC	1	4
XCHG	1	4
HLT	1	5
DCX	1	6
INX	1	6
PCHL	1	6
RET COND.	1/3	6/12
SPHL	1	6
ALU I	2	7
ALU M	2	7
JNC	2/3	7/10
LDAX	2	7
MVI	2	7
MOV M, R	2	7
MOV R, M	2	7
STAX	2	7
CALL COND.	2/5	9/18
DAD	3	10
DCR M	3	10
IN	3	10
INR M	3	10
JMP	3	10
LOAD PAIR	3	10
MVI M	3	10
OUT	3	10
POP	3	10
RET	3	10
PUSH	3	12
RST	3	12
LDA	4	13
STA	4	13
LHLD	5	16
SHLD	5	16
XTHL	5	16
CALL	5	18

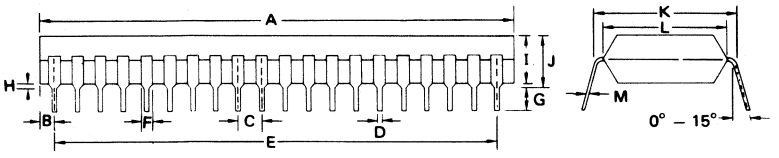
A minimum computer system consisting of a processor, ROM, RAM, and I/O can be built with only 3-40 pin packs. This system is shown below with its address, data, control busses and I/O ports.

μPD8085A FAMILY MINIMUM SYSTEM CONFIGURATION



FEATURES OF μPD8085A MINIMUM SYSTEM
2K – BYTE ROM
256 – BYTE RAM
1 – INTERVAL TIMER
4 – 8-BIT I/O PORTS
1 – 6-BIT I/O-STATUS
4 – INTERRUPT LEVELS

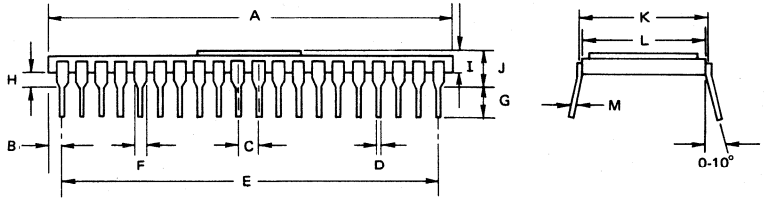
PACKAGE OUTLINE
μPD8085AC



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD8085AD



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

8

16-BIT MICROPROCESSOR

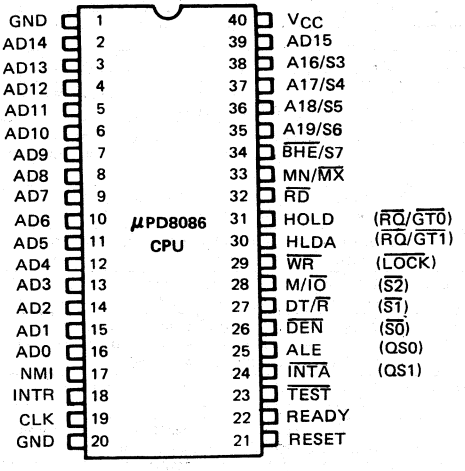
DESCRIPTION

The μPD8086 is a 16-bit microprocessor that has both 8-bit and 16-bit attributes. It has a 16-bit wide physical path to memory for high performance. Its architecture allows higher throughput than the 5 MHz μPD8085A-2.

FEATURES

- Can Directly Address 1 Megabyte of Memory
- Fourteen 16-Bit Registers with Symmetrical Operations
- Bit, Byte, Word, and Block Operations
- 8- and 16-Bit Signed and Unsigned Arithmetic Operations in Binary or Decimal
- Multiply and Divide Instructions
- 24 Operand Addressing Modes
- Assembly Language Compatible with the μPD8080/8085
- Complete Family of Components for Design Flexibility

PIN CONFIGURATION



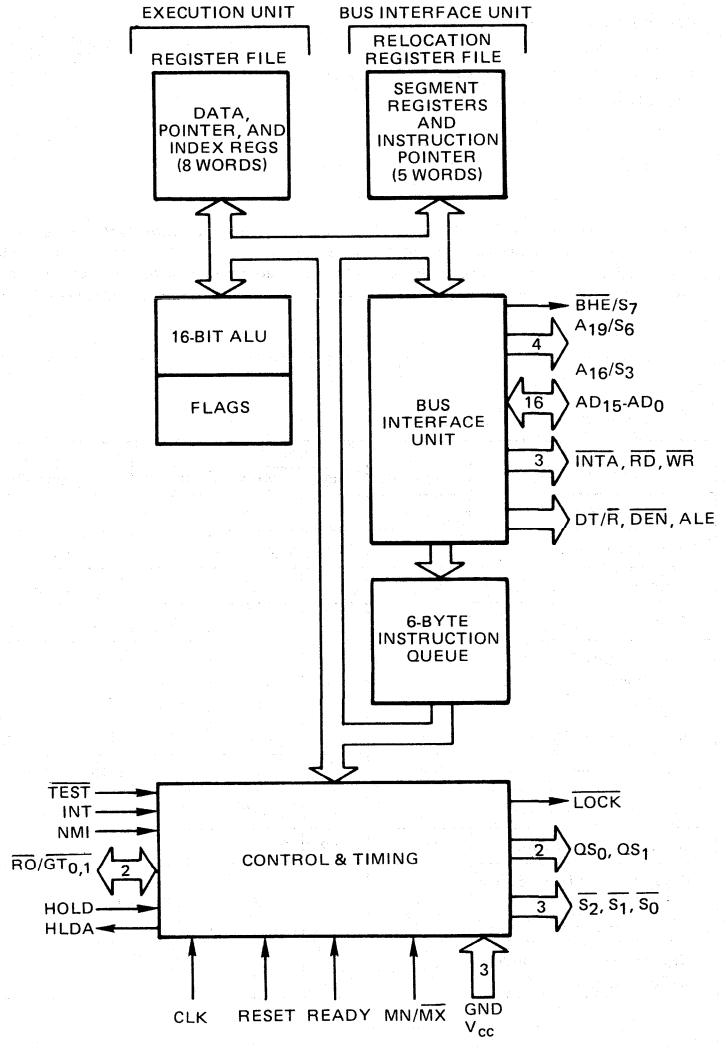
8

*Preliminary

PIN IDENTIFICATION

NO.	SYMBOL	NAME	FUNCTION
2-16, 39	AD0-AD15	Address/Data Bus	Multiplexed address (T_1) and data (T_2, T_3, T_W, T_4) bus. 8-bit peripherals tied to the lower 8 bits, use A0 to condition chip select functions. These lines are tri-state during interrupt acknowledge and hold states.
17	NMI	Non-Maskable Interrupt	This is an edge triggered input causing a type 2 interrupt. A look-up table is used by the processor for vectoring information.
18	INTR	Interrupt Request	A level triggered input sampled on the last clock cycle of each instruction. Vectoring is via an interrupt look-up table. INTR can mask in software by resetting the interrupt enable bit.
19	CLK	Clock	The clock input is a 1/3 duty cycle input basic timing for the processor and bus controller.
21	RESET	Reset	This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.
22	READY	Ready	An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.
23	$\overline{TEST}$	Test	This input is examined by the "WAIT" instruction, and if low, execution continues. Otherwise the processor waits in an "Idle" state. Synchronized by the processor on the leading edge of CLK.
24	$\overline{INTA}$	Interrupt Acknowledge	This is a read strobe for reading vectoring information. During T_2, T_3, and T_W of each interrupt acknowledge cycle it is low.
25	ALE	Address Latch Enable	This is used in conjunction with the μPD8282/8283 latches to latch the address, during T_1 of any bus cycle.
26	$\overline{DEN}$	Data Enable	This is the output enable for the μPD8282/8287 transceivers. It is active low during each memory and I/O access and INTA cycles.
27	DT/$\overline{R}$	Data Transmit/Receive	Used to control the direction of data flow through the transceivers.
28	M/$\overline{IO}$	Memory/IO Status	This is used to separate memory access from I/O access.
29	$\overline{WR}$	Write	Depending on the state of the M/$\overline{IO}$ line, the processor is either writing to I/O or memory.
30	HLDA	Hold Acknowledge	A response to the HOLD input, causing the processor to tri-state the local bus. The bus return active one cycle after HOLD goes back low.
31	HOLD	Hold	When another device requests the local bus, driving HOLD high, will cause the μPD8086 to issue a HLDA.
32	$\overline{RD}$	Read	Depending on the state of the M/$\overline{IO}$ line, the processor is reading from either memory or I/O.
33	MN/$\overline{MX}$	Minimum/Maximum	This input is to tell the processor which mode it is to be used in. This effects some of the pin descriptions.
34	$\overline{BHE}$/S_7	Bus/High Enable	This is used in conjunction with the most significant half of the data bus. Peripheral devices on this half of the bus use BHE to condition chip select functions.
35-38	A16-A19	Most Significant Address Bits	The four most significant address bits for memory operations. Low during I/O operations.
26, 27, 28 34-38	S_0-S_7	Status Outputs	These are the status outputs from the processor. They are used by the μPD8288 to generate bus control signals.
24, 25	QS_1, QS_0	Que Status	Used to track the internal μPD8086 instruction que.
29	$\overline{LOCK}$	Lock	This output is set by the "LOCK" instruction to prevent other system bus masters from gaining control.
30, 31	$\overline{RQ}$/$\overline{GT_0}$ $\overline{RQ}$/$\overline{GT_1}$	Request/Grant	Other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.

BLOCK DIAGRAM



8

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . -1.0 to +7V
Power Dissipation 2.5W

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	+0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.5 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -400 μA
Power Supply Current μPD8086/ μPD8086-2	I_{CC}		 340 350	 mA mA	$T_a = 25°C$
Input Leakage Current	I_{LI}		±10	μA	$0V < V_{IN} < V_{CC}$
Output Leakage Current	I_{LO}		±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
Clock Input Low Voltage	V_{CL}	-0.5	+0.6	V	
Clock Input High Voltage	V_{CH}	3.9	V_{CC} + 1.0	V	
Capacitance of Input Buffer (All input except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IN}		15	pF	fc = 1 MHz
Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IO}		15	pF	fc = 1 MHz

μPD8086: $T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

AC CHARACTERISTICS

MINIMUM COMPLEXITY SYSTEM

TIMING REQUIREMENTS

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1.0V to 3.5V
CLK Fall Time	TCL2CL1		10		10	ns	From 3.5V to 1.0V
Data In Setup Time	TDVCL	30		20		ns	
Data In Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ① ②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ① ②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY Inactive to CLK ③	TRYLCL	–8		–8		ns	
HOLD Setup Time	THVCH	35		20		ns	
INTR, NMI, $\overline{TEST}$ Setup Time ②	TINVCH	30		15		ns	
Input Rise Time	TILIH		20			ns	From 0.8V to 2.0V
Input Fall Time	TIHIL		12			ns	From 2.0V to 0.8V

TIMING RESPONSES

TIMING RESPONSES

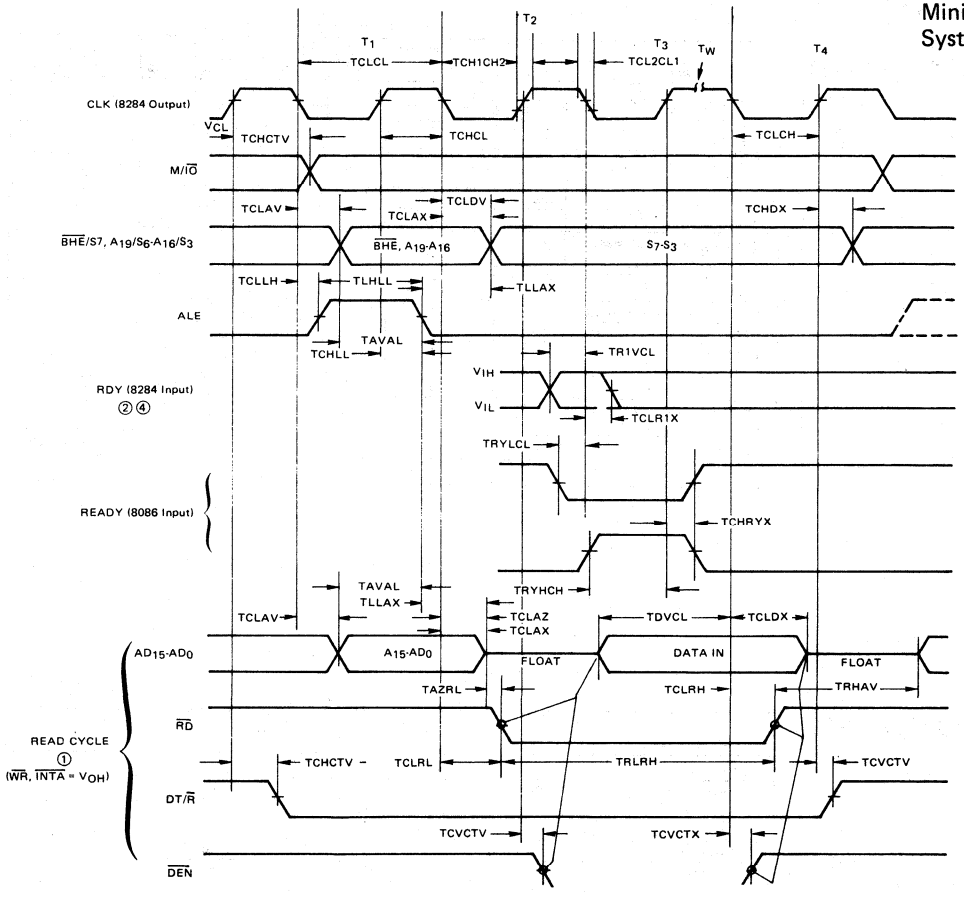
PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Address Valid Delay	TCLAV	10	110	10	60		C_L = 20-100 pF for all μPD8086 Outputs (In addition to μPD8086 self-load)
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
ALE Width	TLHLL	TCLCH–20		TCLCH–10		ns	
ALE Active Delay	TCLLH		80		50	ns	
ALE Inactive Delay	TCHLL		85		55	ns	
Address Hold Time to ALE Inactive	TLLAX	TCHCL–10		TCHCL–10		ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	
Data Hold Time	TCHDX	10		10		ns	
Data Hold Time After WR	TWHDX	TCLCH–30		TCLCH–30		ns	
Control Active Delay 1	TCVCTV	10	110	10	70	ns	
Control Active Delay 2	TCHCTV	10	110	10	60	ns	
Control Active Delay	TCVCTX	10	110	10	70	ns	
Address Float to READ Active	TAZRL	0		0		ns	
$\overline{RD}$ Active Delay	TCLRL	10	165	10	100	ns	
$\overline{RD}$ Inactive Delay	TCLRH	10	150	10	80	ns	
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL–45		TCLCL–40		ns	
HLDA Valid Delay	TCLHAV	10	160	10	100	ns	
$\overline{RD}$ Width	TRLRH	2TCLCL–75		2TCLCL–50		ns	
$\overline{WR}$ Width	TWLWH	2TCLCL–60		2TCLCL–40		ns	
Address Valid to ALE Low	TAVAL	TCLCH–60		TCLCH–40		ns	
Output Rise Time	TOLOH		20			ns	From 0.8V to 2.0V
Output Fall Time	TOHOL		12			ns	From 2.0V to 0.8V

NOTES: ① Signal at μPD8284 shown for reference only.
② Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
③ Applies only to T2 state. (8 ns into T3)

8

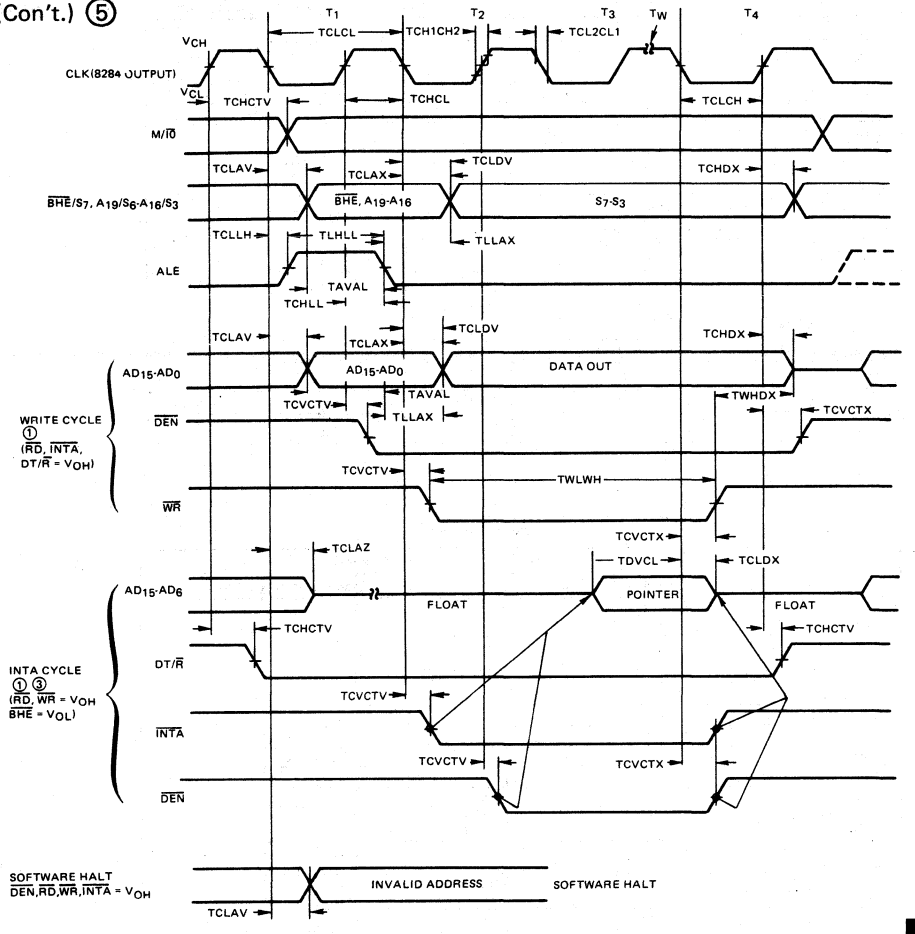
TIMING WAVEFORMS

Minimum Complexity Systems ⑤



TIMING WAVEFORMS

Minimum Complexity Systems (Con't.) ⑤



NOTES: ① All signals switch between V_{OH} and V_{OL} unless otherwise specified.

② RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.

③ Two INTA cycles run back-to-back. The μPD8086 local ADDR/Data Bus is floating during both INTA cycles. Control signals shown for second INTA cycle.

④ Signals at μPD8284 are shown for reference only.

⑤ All timing measurements are made at 1.5V unless otherwise noted.

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MAXIMUM MODE SYSTEM
With μPB8288 Bus Controller

TIMING WITH μPB8288 BUS CONTROLLER

TIMING REQUIREMENTS

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1.0V to 3.5V
CLN Fall Time	TCL2CL1		10		10	ns	From 3.5V to 1.0V
Data in Setup Time	TDVCL	30		20		ns	
Data in Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ① ②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ①, ②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY inactive to CLK ④	TRYLCL	-8		-8		ns	
Setup Time for Recognition (INTR, NMI, TEST) ②	TINVCH	30		15		ns	
$\overline{RQ}$/GT Setup Time	TGVCH	30		15		ns	
$\overline{RQ}$ Hold Time into μPD8086	TCHGX	40		30		ns	
Input Rise Time	TILIH		20			ns	From 0.8V to 2.0V
Input Fall Time	TIHIL		12			ns	From 2.0V to 0.8V

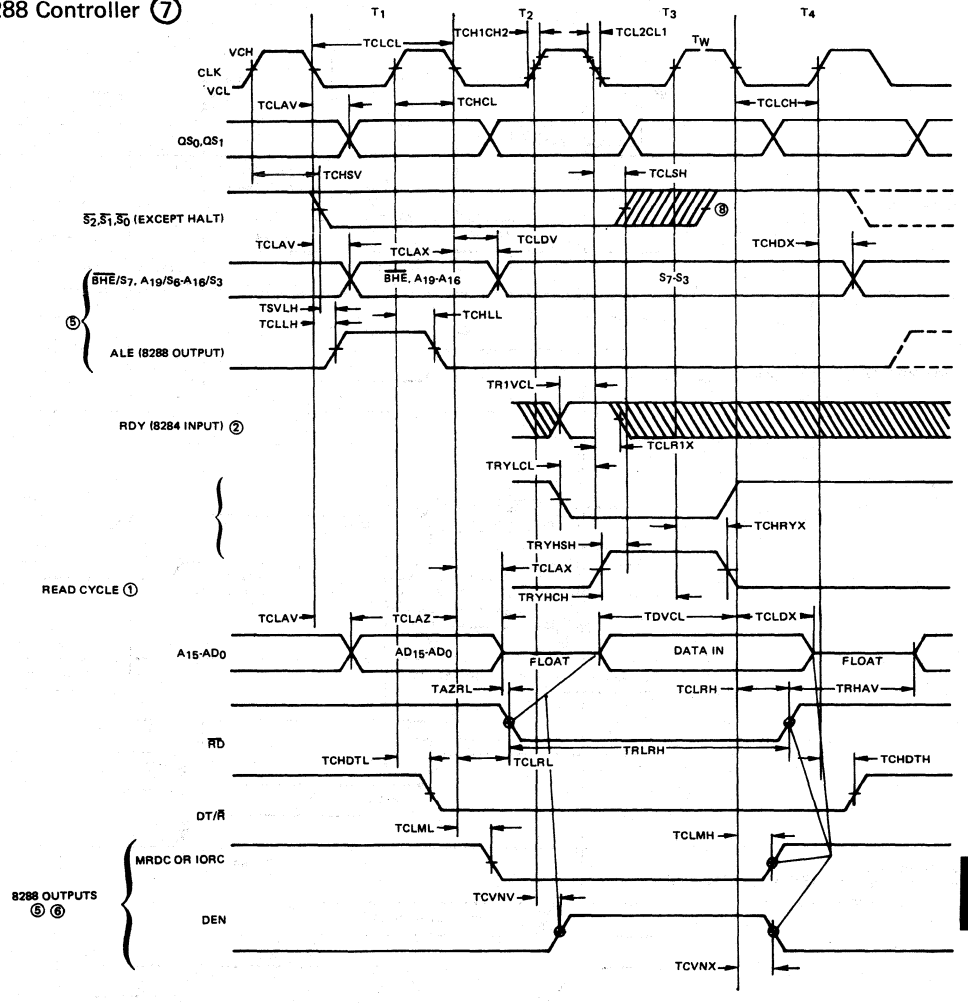
TIMING RESPONSES

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Command Active Delay (See Note 1)	TCLML	10	35	10	35	ns	
Command Inactive Delay (See Note 1)	TCLMH	10	35	10	35	ns	
READY Active to Status Passive (See Note 3)	TRYHSH		110		65	ns	
Status Active Delay	TCHSV	10	110	10	60	ns	
Status Inactive Delay	TCLSH	10	130	10	70	ns	
Address Valid Delay	TCLAV	10	110	10	60	ns	
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
Status Valid to ALE High (See Note 1)	TSVLH		15		15	ns	
Status Valid to MCE High (See Note 1)	TSVMCH		15		15	ns	
CLK Low to ALE Valid (See Note 1)	TCLLH		15		15	ns	
CLK Low to MCE High (See Note 1)	TCLMCH		15		15	ns	
ALE Inactive Delay (See Note 1)	TCHLL		15		15	ns	C_L = 20-100 pF for all μPD8086 Outputs (In addition to μPD8086 self-load)
MCE Inactive Delay (See Note 1)	TCLMCL		15		15	ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	
Data Hold Time	TCHDX	10		10		ns	
Control Active Delay (See Note 1)	TCVNV	5	45	5	45	ns	
Control Inactive Delay (See Note 1)	TCVNX	10	45	10	45	ns	
Address Float to Read Active	TAZRL	0		0		ns	
RD Active Delay	TCLRL	10	165	10	100	ns	
RD Inactive Delay	TCLRH	10	150	10	80	ns	
RD Inactive to Next Address Active	TRHAV	TCLCL-45		TCLCL-40		ns	
Direction Control Active Delay (See Note 1)	TCHDTL		50		50	ns	
Direction Control Inactive Delay (See Note 1)	TCHDTH		30		30	ns	
$\overline{GT}$ Active Delay	TCLGL	0	85	0	50	ns	
$\overline{GT}$ Inactive Delay	TCLGH	0	85	0	50	ns	
$\overline{RD}$ Width	TRLRH	2TCLCL-50		2TCLCL-50		ns	
Output Rise Time	TOLOH		20			ns	From 0.8V to 2.0V
Output Fall Time	TOHOL		12			ns	From 2.0V to 0.8V

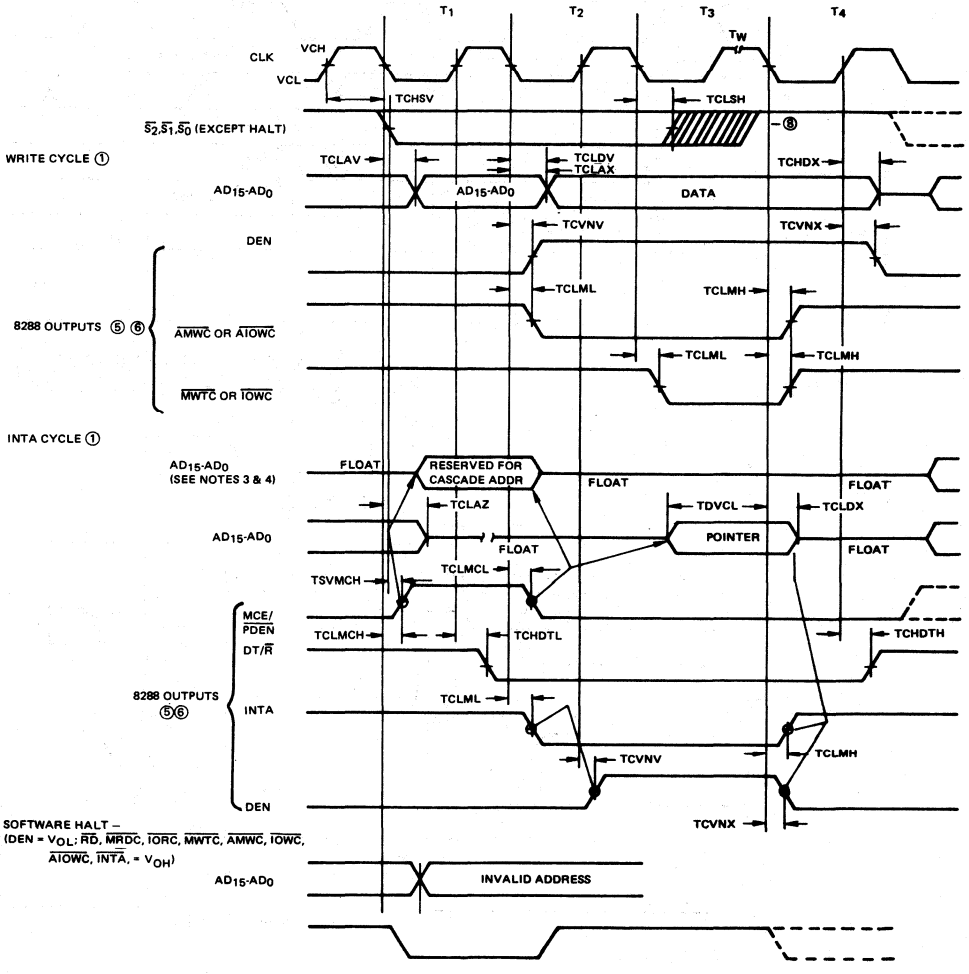
NOTES: ① Signal at μPB8284 or μPB8288 shown for reference only.
② Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
③ Applies only to T3 and wait states.
④ Applies only to T2 state (8 ns into T3).

TIMING WAVEFORMS

Maximum Mode System Using μPB8288 Controller ⑦

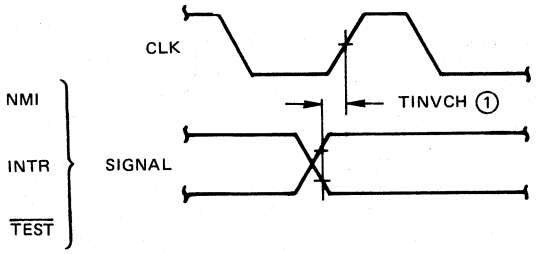


TIMING WAVEFORMS
Maximum Mode
System Using
μPB8288 Controller
(Con't.) ⑦



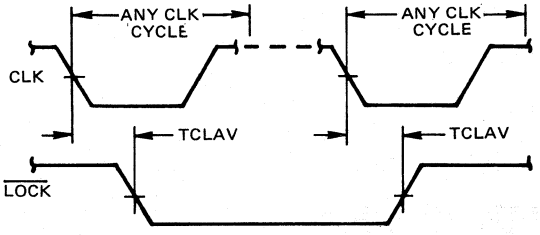
NOTES:
① All signals switch between V_{OH} and V_{OL} unless otherwise specified.
② RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
③ Cascade address is valid between first and second INTA cycle.
④ Two INTA cycles run back-to-back. The 8086 local ADDR/Data Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
⑤ Signals at 8284 or 8288 are shown for reference only.
⑥ The issuance of the 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 8288 CEN.
⑦ All timing measurements are made at 1.5V unless otherwise noted.
⑧ Status inactive in state just prior to T_4.

ASYNCHRONOUS SIGNAL RECOGNITION

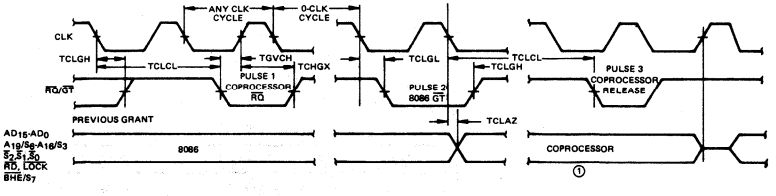


NOTE: (1) Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

BUS LOCK SIGNAL TIMING



REQUEST/GRANT SEQUENCE TIMING*

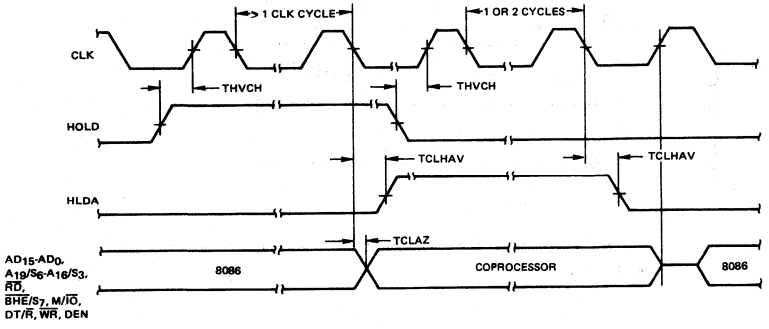


NOTE: (1) The coprocessor may not drive the buses outside the region shown without risking contention.

*for Maximum Mode only

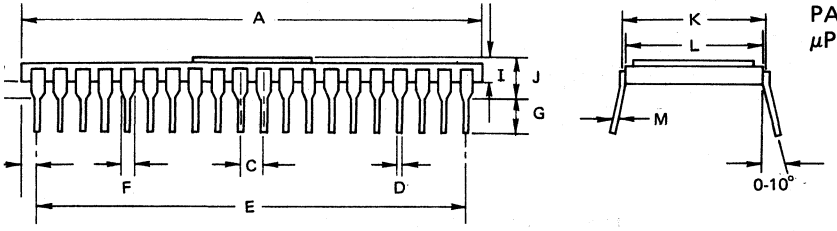
8

HOLD/HOLD ACKNOWLEDGE TIMING*



*for Minimum Mode only

PACKAGE OUTLINE μPD8086D



Cerdip

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP.	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

μPD8088
HIGH-PERFORMANCE 8-BIT MICROPROCESSOR

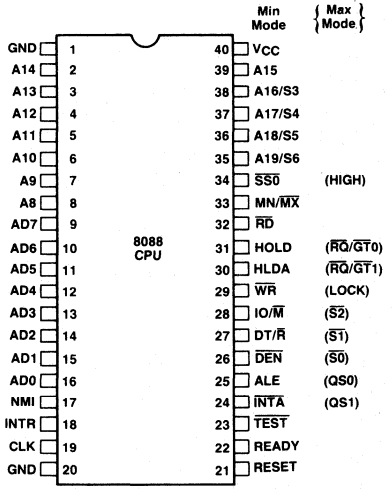
Description

The μPD8088 is a powerful 8-bit microprocessor that is software-compatible with the μPD8086. The μPD8088 has the same bus interface signals as the μPD8085A, allowing it to interface directly with multiplexed bus peripherals. The μPD8088 has a 20-bit address space which can be divided into four segments of up to 64K bytes each.

Features

- ☐ 8-bit data bus interface
- ☐ 16-bit internal architecture
- ☐ Addresses 1 M-byte of memory
- ☐ Software-compatible with the 8086
- ☐ Provides byte, word, and block operations
- ☐ Performs 8- and 16-bit signed and unsigned arithmetic in binary and decimal
- ☐ Multiply and divide instruction
- ☐ Directly interfaces to 8155, 8355, and 8755A multiplexed peripherals
- ☐ 40-pin DIP

Pin Configuration

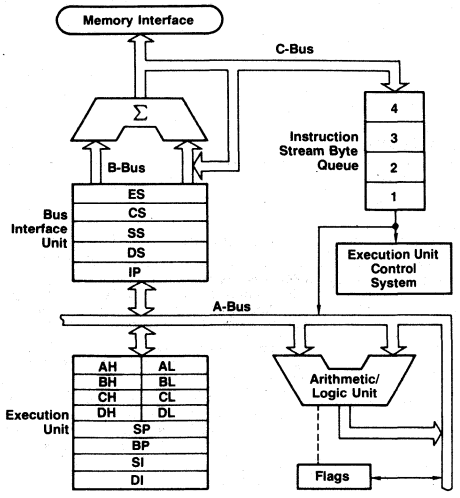


Pin Identification

No.	Symbol	Name	Function
1, 20	GND	Ground	
2–8, 35–39	A_{19}–A_8	Most significant address bits	Most significant bits for memory operations.
9–16	AD_7–AD_0	Address/Data bus	Multiplexed address and data bus. 8-bit peripherals tied to these bits use A_0 to condition chip select functions. These lines are tri-state during hold and interrupt acknowledge states.
17	NMI	Non-maskable interrupt	This edge-triggered input causes a type 2 interrupt. The processor uses a lookup table for vectoring information.
18	INTR	Interrupt request	This is a level-triggered interrupt sampled on the last clock cycle of each instruction. A lookup table is used for vectoring. INTR can be masked by software by resetting the interrupt enable bit.
19	CLK	Clock	The clock is a 1/3 duty cycle input providing basic timing for the processor and bus controller.
21	RESET	Reset	This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.
22	READY	Ready	An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.
23	$\overline{TEST}$	Test	This input is examined by the "WAIT" instruction and if low, execution continues. Otherwise the processor waits in an "idle" state. Synchronized by the processor on the leading edge of CLK.
24	$\overline{INTA}$	Interrupt Acknowledge	This is a read strobe for reading vectoring information. During T_2, T_3, and T_W of each interrupt acknowledge cycle it is low.
25	$\overline{ALE}$	Address Latch Enable	Used with the μPD8282/8283 latches to latch the address during T_1 of any bus cycle.
24, 25	QS_1, QS_0	Queue Status	(Max Mode) Tracks the internal μPD8088 instruction queue.
26	$\overline{DEN}$	Data Enable	This is the output enable for the μPD8286/8287 transceivers. It is active low during memory and I/O access and INTA cycles.
27	DT/$\overline{R}$	Data Transmit/ Receive	Controls the direction of data flow through the transceivers.
28	IO/M	I/O/Memory Status	Separates memory access from I/O access.
29	$\overline{WR}$	Write	The processor is writing to memory or I/O, depending on the state of the IO/M line.
29	LOCK	Lock	(Max Mode) This output is set by the lock instruction to prevent other system bus masters from gaining control.
30	HLDA	Hold Acknowledge	A response to the HOLD input, causing the processor to tri-state the local bus. The bus becomes active one cycle after HOLD returns low.
31	HOLD	Hold	When another device requests the local bus, HOLD is driven high, causing the μPD8088 to issue a HLDA.
30, 31	$\overline{RQ}/GT_0$ $\overline{RQ}/GT_1$	Request/Grant	(Max Mode) Other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.
32	$\overline{RD}$	Read	Depending on the state of the $\overline{IO}$/M line, the processor is reading from memory or I/O.
33	MN/$\overline{MX}$	Minimum/ Maximum	This input tells the processor in which mode it is to be used. This affects some of the pin descriptions.
34	$\overline{SS0}$	Status Line	Equivalent to $\overline{S_0}$ in Max Mode.
26–28	$\overline{S_0}$–$\overline{S_2}$	Status Outputs	(Max Mode)
35–38	S_3–S_6	Status Outputs	These outputs from the processor are used by the μPD8288 to generate bus control signals.
40	V_{CC}	Power Supply	5V power input.

8

ıck Diagram



solute Maximum Ratings*
= 25°C

itative	
bient Temperature under Bias	0°C to 70°C
rage Temperature	−65°C to +150°C
tage on any Pin with respect to Ground	−0.5V to +7V
ver Dissipation	1.5 Watt

OMMENT: Exposing the device to stresses above se listed in Absolute Maximum Ratings could cause manent damage. The device is not meant to be oper- d under conditions outside the limits described in operational sections of this specification. Exposure absolute maximum rating conditions for extended iods may affect device reliability.

Characteristics
= 0°C to +70°C, V_{CC} = +5V ± 10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{CL}	−0.5		+0.6	V	
Input High Voltage	V_{CH}	3.9		V_{CC} + 1.0	V	
Low Voltage	V_{IL}	−0.5		+0.8	V	
High Voltage	V_{IH}	2.0		VCC + 0.5	V	
ut Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
ut High Voltage	V_{OH}	2.4			V	I_{OH} = 400 μA
r Supply Current	I_{CC}			340	mA	
Leakage	I_{LI}			±10	μA	OV < V_{IN} < V_{CC}
ut Leakage	I_{LO}			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}

pacitance

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
citance of Input r (All input except AD_7 RQ/GT)	C_{IN}			15	pF	fc = 1 MHz
citance of I/O Buffer AD_7 RQ/GT)	C_{IO}			15	pF	fc = 1 MHz

AC Characteristics
Minimum Mode Timing Requirements
T_a = 0°C to +70°C, V_{CC} = +5V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
CLK Period	t_{CLCL}	200		500	ns	
CLK Low Time	t_{CLCH}	$(2/3t_{CLCL})-15$			ns	
CLK High Time	t_{CHCL}	$(1/3t_{CLCL})+2$			ns	
CLK Rise Time	t_{CH1CH2}			10	ns	1.0V to 3.5V
CLK Fall Time	t_{CL2CL1}			10	ns	3.5V to 1.0V
Data In Setup Time	t_{DVCL}	30			ns	
Data In Hold Time	t_{CLDX}	10			ns	
RDY Setup Time μPD8284 ① ②	t_{R1VCL}	35			ns	
RDY Hold Time into μPD8284 ① ②	t_{CLR1X}	0			ns	
READY Setup Time into μPD8088	t_{RYHCH}	$(2/3t_{CLCL})-15$			ns	
READY Hold Time into μPD8088	t_{CHRYX}	30			ns	
READY Inactive to CLK ③	t_{RYLCL}	−8			ns	
HOLD Setup Time	t_{HVCH}	35			ns	
INTR, NMI, TEST Setup Time ②	t_{INVCH}	30			ns	

Notes:

① Signal at μPD8284 shown for reference only.

② Setup requirement for asynchronous signal guarantees recognition at next CLK.

③ Applies to T_2 state (8 ns into T_3 state).

Timing Responses

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Address Valid Delay	t_{CLAV}	15		110	ns	
Address Hold Time	t_{CLAX}	10			ns	
Address Float Delay	t_{CLAZ}	t_{CLAX}		80	ns	
ALE Width	t_{LHLL}	$t_{CLCH}-20$			ns	
ALE Active Delay	t_{CLLH}			80	ns	
ALE Inactive Delay	t_{CHLL}			85	ns	
Address Hold Time to ALE Inactive	t_{LLAX}	$t_{CHCL}-10$			ns	
Data Valid Delay	t_{CLDV}	10		110	ns	C_L = 20-100 pF for all 8088 outputs and internal loads
Data Hold Time	t_{CHDX}	10			ns	
Data Hold Time After WR	t_{WHDX}	$t_{CLCH}-30$			ns	
Control Active Delay 1	t_{CVCTV}	10		110	ns	
Control Active Delay 2	t_{CHCTV}	10		110	ns	
Control Inactive Delay	t_{CVCTX}	10		110	ns	
Address Float to READ Active	t_{AZRL}	0			ns	
RD Active Delay	t_{CLRL}	10		165	ns	
RD Inactive Delay	t_{CLRH}	10		150	ns	
RD Inactive to Next Address Active	t_{RHAV}	$t_{CLCL}-45$			ns	
HLDA Valid Delay	t_{CLHAV}	10		160	ns	
RD Width	t_{RLRH}	$2t_{CLCL}-75$			ns	
WR Width	t_{WLWH}	$2t_{CLCL}-60$			ns	
Address Valid to ALE Low	t_{AVAL}	$t_{CLCH}-60$			ns	

AC Characteristics (Cont.)

Max Mode System Timing Requirements (Using 8288 Bus Controller)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
CLK Period	t_{CLCL}	200		500	ns	
CLK Low Time	t_{CLCH}	$(2/3t_{CLCL})-15$			ns	
CLK High Time	t_{CHCL}	$(1/3t_{CLCL})+2$			ns	
CLK Rise Time	t_{CH1CH2}			10	ns	1.0V to 3.5V
CLK Fall Time	t_{CL2CL1}			10	ns	3.5V to 1.0V
Data In Setup Time	t_{DVCL}	30			ns	
Data In Hold Time	t_{CLDX}	10			ns	
RDY Setup Time into μPD8284 ① ②	t_{R1VCL}	35			ns	
RDY Hold Time into μPD8284 ①●②	t_{CLR1X}	0			ns	
READY Setup Time into μPD8088	t_{RYHCH}	$(2/3t_{CLCL})-15$			ns	
READY Hold Time into μPD8088	t_{CHRYX}	30			ns	
READY Inactive to CLK ④	t_{RYLCL}	−8			ns	
Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) ②	t_{INVCH}	30			ns	
RQ/$\overline{GT}$ Setup Time	t_{GVCH}	30			ns	
RQ Hold Time into μPD8088	t_{CHGX}	40			ns	

Timing Responses

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Command Active Delay ①	t_{CLML}	10		35	ns	
Command Inactive Delay ①	t_{CLMH}	10		35	ns	
READY Active to Status Passive ③	t_{RYHSH}			110	ns	
Status Active Delay	t_{CHSV}	10		110	ns	
Status Inactive Delay	t_{CLSH}	10		130	ns	
Address Valid Delay	t_{CLAV}	15		110	ns	
Address Hold Time	t_{CLAX}	10			ns	
Address Float Delay	t_{CLAZ}	t_{CLAX}		80	ns	
Status Valid to ALE High ①	t_{SVLH}			15	ns	
Status Valid to MCE High ①	t_{SVMCH}			15	ns	
CLK Low to ALE Valid ①	t_{CLLH}			15	ns	
CLK Low to MCE High ①	t_{CLMCH}			15	ns	
ALE Inactive Delay ①	t_{CHLL}			15	ns	C_L = 20-100 pF for all 8088 outputs and internal loads
MCE Inactive Delay ①	t_{CLMCL}			15	ns	
Data Valid Delay	t_{CLDV}	15		110	ns	
Data Hold Time	t_{CHDX}	10			ns	
Control Active Delay ①	t_{CVNV}	5		45	ns	
Control Inactive Delay ①	t_{CVNX}	10		45	ns	
Address Float to $\overline{READ}$ Active	t_{AZRL}	0			ns	
$\overline{RD}$ Active Delay	t_{CLRL}	10		165	ns	
$\overline{RD}$ Inactive Delay	t_{CLRH}	10		150	ns	
$\overline{RD}$ Inactive to Next Address Active	t_{RHAV}	$t_{CLCL}-45$			ns	
Direction Control Active Delay ①	t_{CHDTL}			50	ns	
Direction Control Inactive Delay ①	t_{CHDTH}			30	ns	
$\overline{GT}$ Active Delay	t_{CLGL}			110	ns	
$\overline{GT}$ Inactive Delay	t_{CLGH}			85	ns	
$\overline{RD}$ Width	t_{RLRH}	$2t_{CLCL}-75$			ns	

Notes:

① Signal at μPD8284 or μPD8288 shown for reference only.

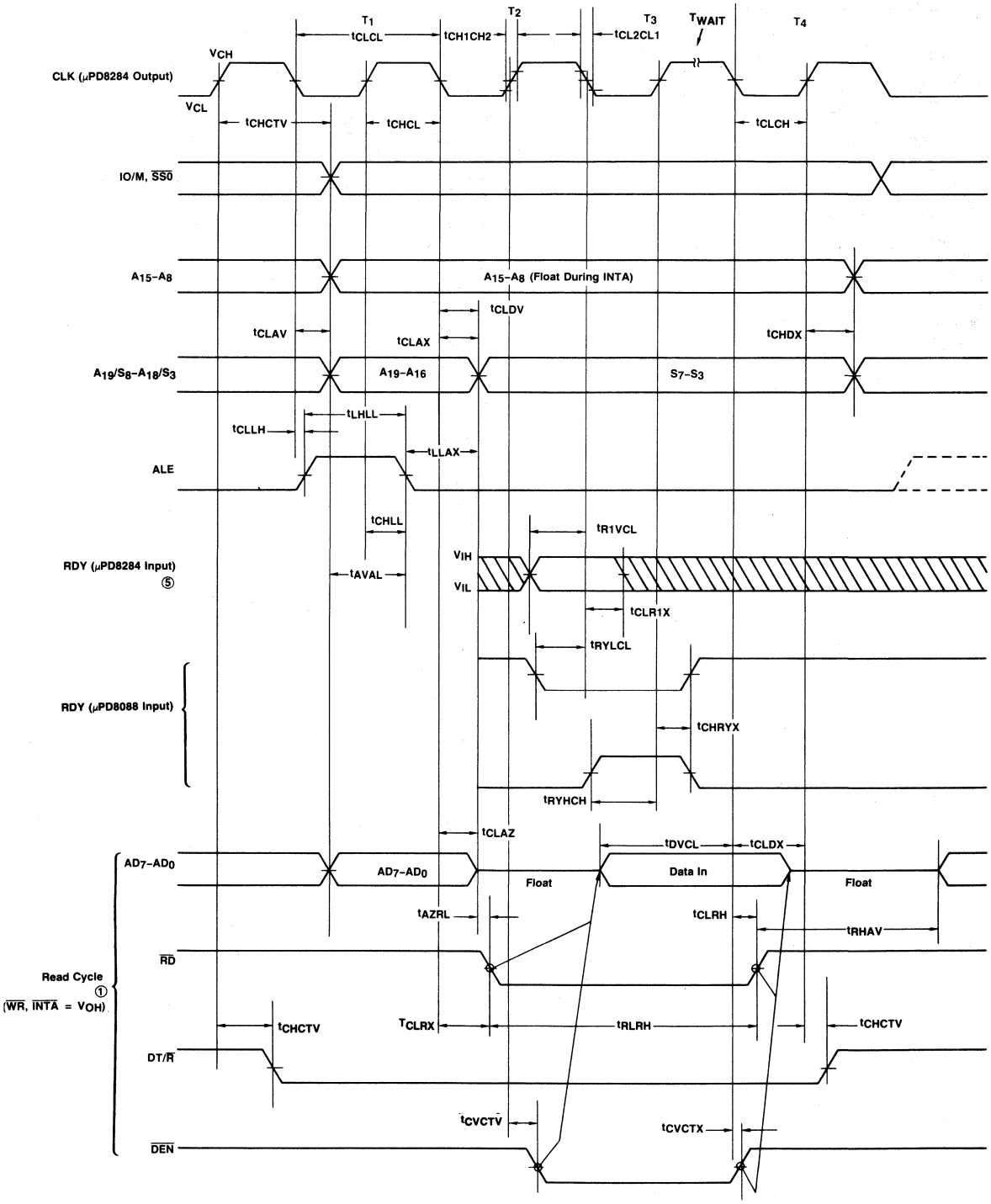
② Setup requirement for asynchronous signal guarantees recognition at next CLK.

③ Applies to T_3 and wait states.

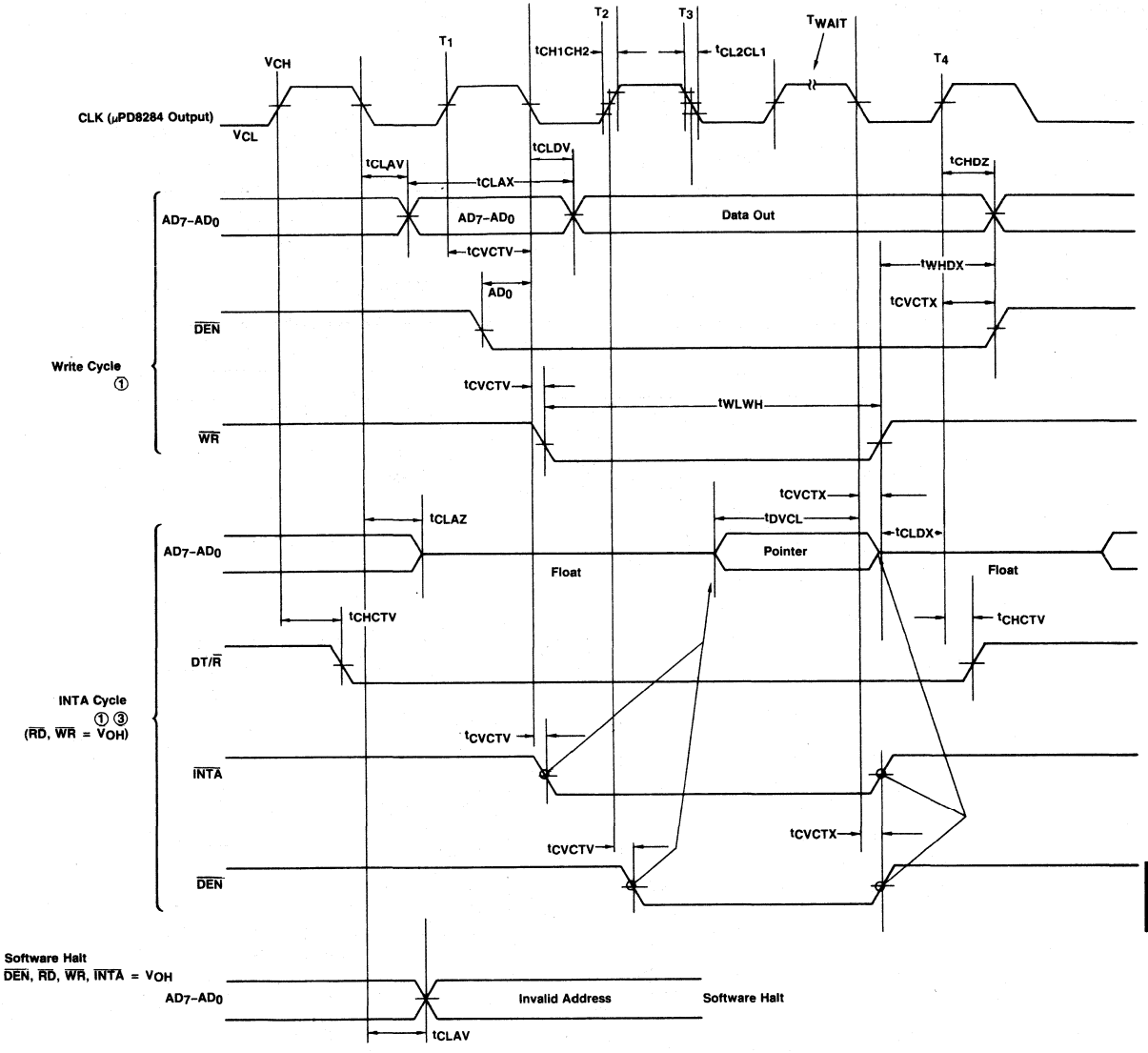
④ Applies to T_2 state (8 ns into T_3 state).

8

Timing Waveforms



Timing Waveforms (Cont.)



Notes:

① All signals switch between V_{OH} and V_{OL} unless otherwise specified.

② RDY is sampled near the end of T_2, T_3, T_{WAIT} to determine if T_{WAIT} machine states are inserted.

③ Two INTA cycles run back-to-back. The μPD8088 local Address/ Data bus floats during both INTA cycles. The control signals shown are for the second INTA cycle.

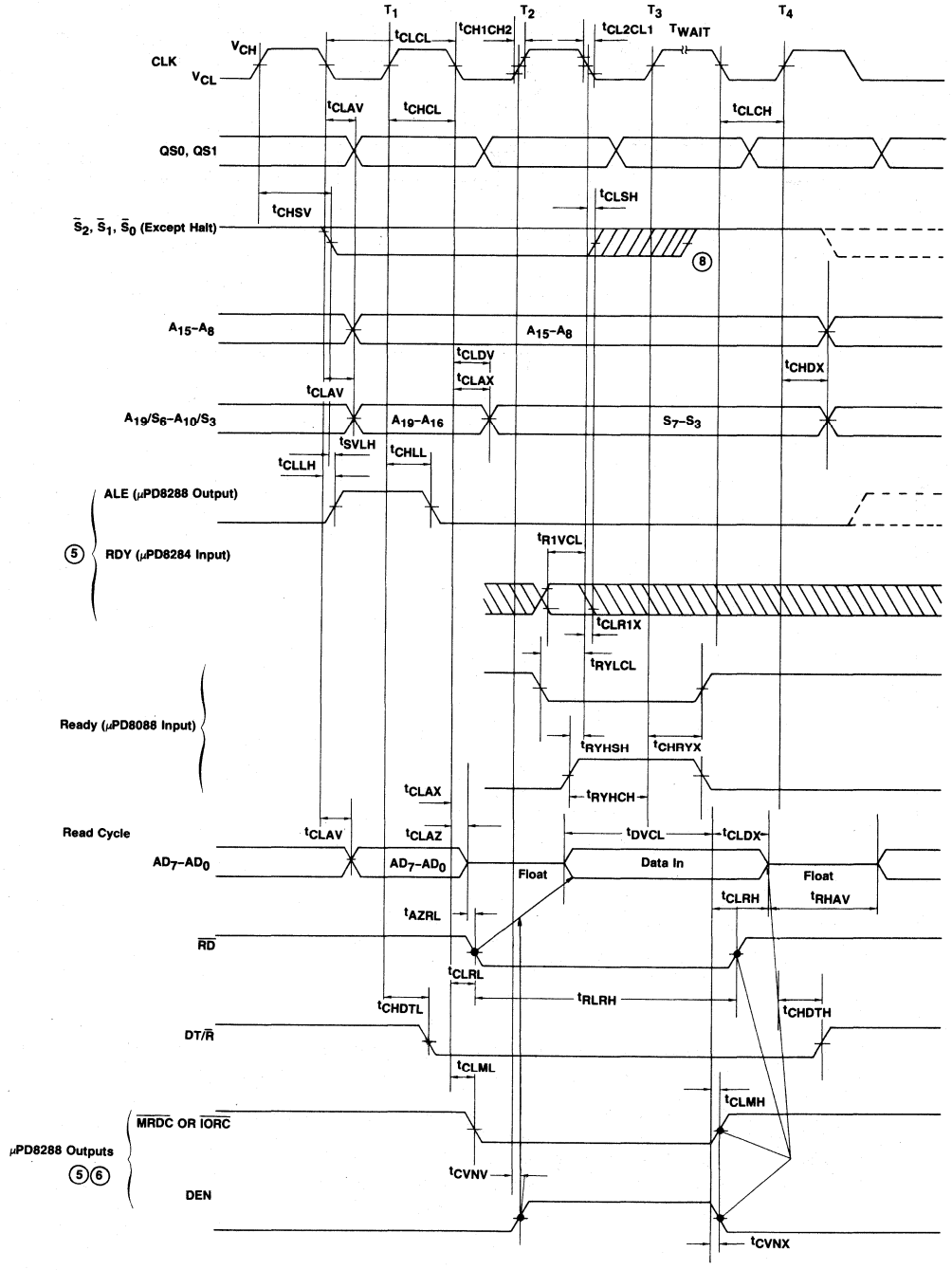
④ Signals at the μPD8284 are shown for reference.

⑤ All timing measurements are taken at 1.5V unless otherwise specified.

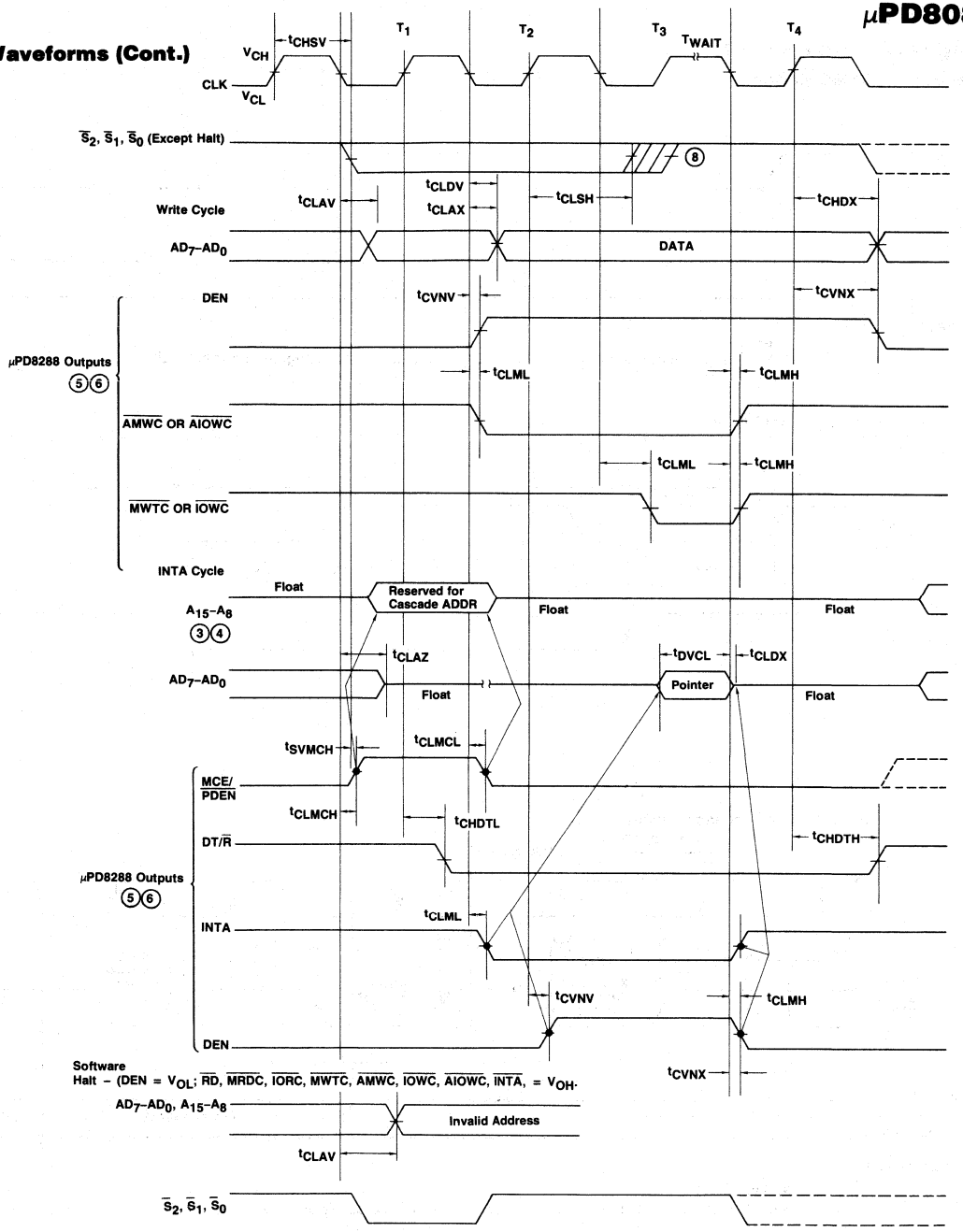
8

Timing Waveforms (Cont.)

Maximum Mode System Bus Timing (using 8288 Bus Controller)



Timing Waveforms (Cont.)

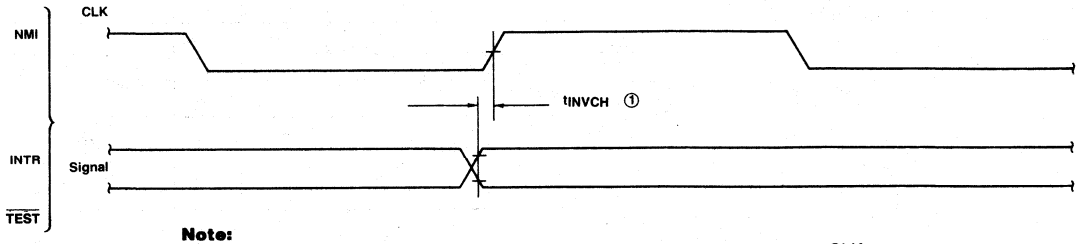


Notes:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_{WAIT} to determine if T_{WAIT} machine states are inserted.
3. The cascade address is valid between the first and second INTA cycles.
4. Two INTA cycles run back-to-back. The μPD8088 local Address/Data bus floats during both INTA cycles. The control signals shown are for the second INTA cycle.
5. Signals at the μPD8284 and μPD8288 are shown for reference.
6. The μPD8288 active-high CEN lags when the μPD8288 issues command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$, and $\overline{DEN}$).
7. All timing measurements are taken at 1.5V unless otherwise specified.
8. Status is inactive prior to T_4.

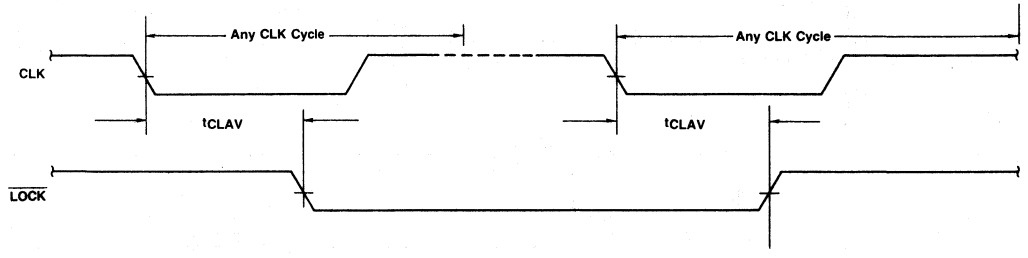
Timing Waveforms (Cont.)

Asynchronous Input Recognition

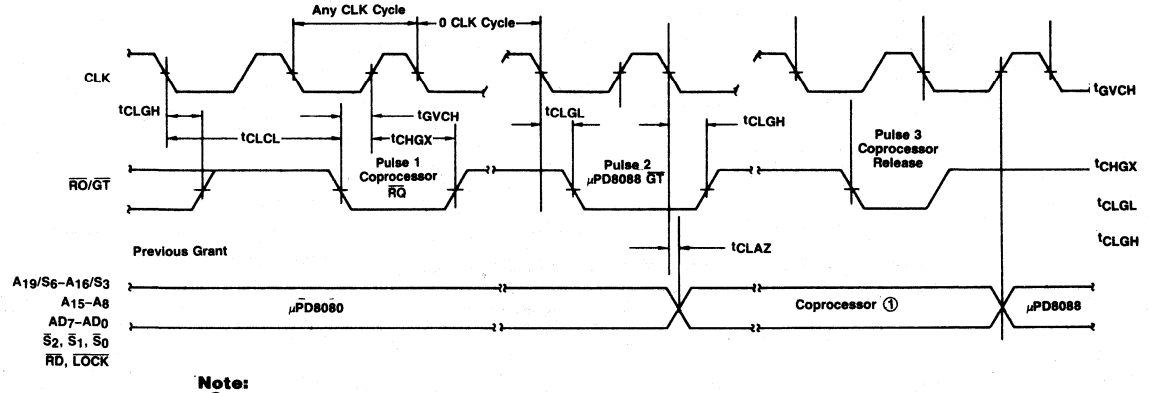


Note:
① Setup requirements for asynchronous signals guarantee recognition at next CLK.

Maximum Mode Bus Lock Signal Timing



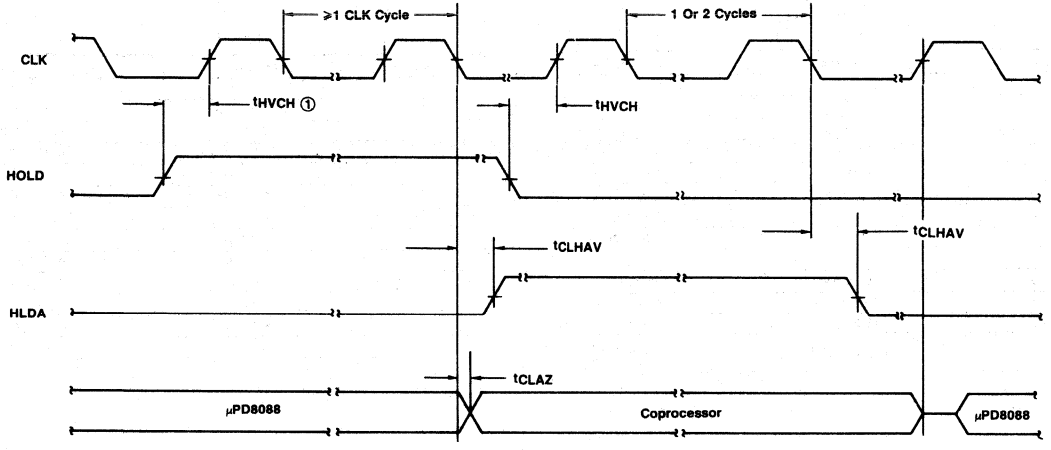
Maximum Mode Request/Grant Sequence Timing



Note:
① The coprocessor risks bus contention if it drives the buses outside the areas shown.

Timing Waveforms (Cont.)

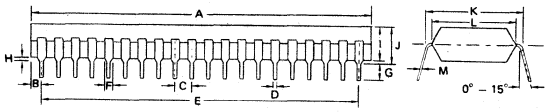
Mimimum Mode Hold Acknowledge Timing



Note:
① All signals switch between V_{OH} and V_{OL} unless otherwise specified.

Package Outlines

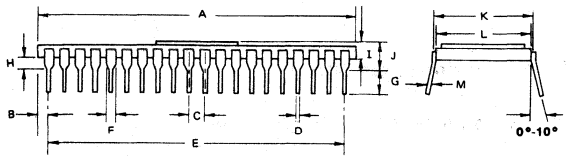
μPD8088C



Plastic

Item	Millimeters	Inches
A	51.5 Max	2.028 Max
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 Min	0.047 Min
G	2.54 Min	0.10 Min
H	0.5 Min	0.019 Min
I	5.22 Max	0.206 Max
J	5.72 Max	0.225 Max
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD8088D



Cerdip

Item	Millimeters	Inches
A	51.5 Max	2.03 Max
B	1.62 Max	0.06 Max
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ±0.1	1.9 ±0.004
F	1.02 Min	0.04 Min
G	3.2 Min	0.13 Min
H	1.0 Min	0.04 Min
I	3.5 Max	0.14 Max
J	4.5 Max	0.18 Max
K	15.24 Typ	0.6 Typ
L	14.93 Typ	0.59 Typ
M	0.25 ± 0.05	0.01 ± 0.0019

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SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD765 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The μPD765 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the μPD765 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the μPD8257. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the μPD765 and DMA controller.

There are 15 separate commands which the μPD765 will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

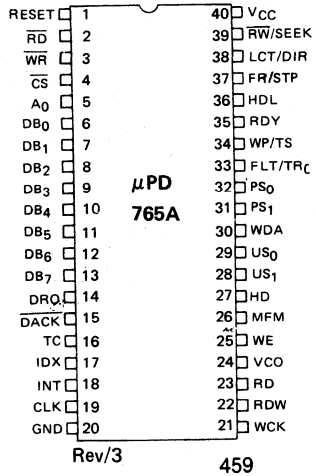
Read Data	Scan High or Equal	Write Deleted Data
Read ID	Scan Low or Equal	Seek
Read Deleted Data	Specify	Recalibrate (Restore to Track 0)
Read a Track	Write Data	Sense Interrupt Status
Scan Equal	Format a Track	Sense Drive Status

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The μPD765 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer Capability
- Drive Up to 4 Floppy Disks
- Data Scan Capability — Will Scan a Single Sector or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the Processor's Memory with Data Read from the Diskette
- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with Most Microprocessors Including 8080A, 8085A, μPD780 (Z80™)
- Single Phase 8 MHz Clock
- Single +5 Volt Power Supply
- Available in 40 Pin Plastic Dual-in-Line Package

PIN CONFIGURATION



Rev/3

TM:Z80 is a registered trademark of Zilog, Inc.

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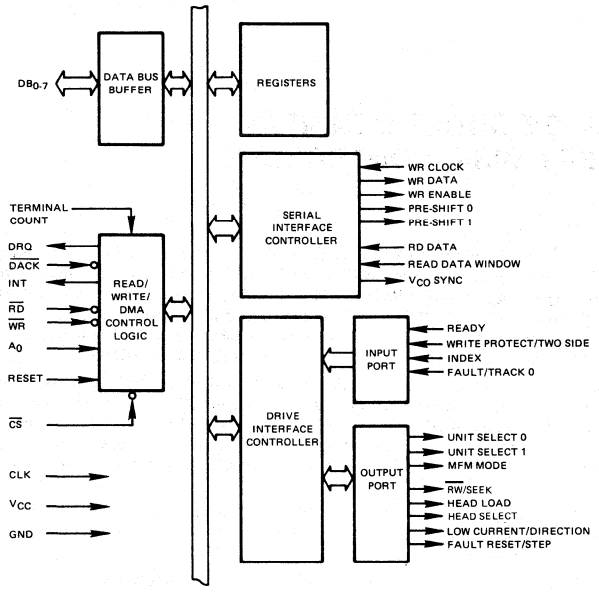
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +70°C
Storage Temperature	-55°C to +150°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltage V_{CC}	-0.5 to +7 Volts
Power Dissipation	1 Watt

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = -10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = -200 μA
Input Low Voltage (CLK + WR Clock)	$V_{IL(\Phi)}$	-0.5		0.65	V	
Input High Voltage (CLK + WR Clock)	$V_{IH(\Phi)}$	2.4		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}			150	mA	
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = V_{CC}
				-10	μA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			-10	μA	V_{OUT} = +0.45V

Note: ① Typical values for T_a = 25°C and nominal supply voltage.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION TO	FUNCTION
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1-25 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input(1)	Processor	Control signal for transfer of data from FDC to Data Bus; when "0" (low).
3	$\overline{WR}$	Write	Input(1)	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input(1)	Processor	Selects Data Reg (A_0=1) or Status Reg (A_0=0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input/(1) Output	Processor	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRQ="1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	CLK	Clock	Input		Single Phase 8 MHz Squarewave Clock.
20	GND	Ground			D.C. Power Return.
21	WCK	Write Clock	Input		Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Input	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.
23	RDD	Read Data	Input	FDD	Read data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Output	Phase Lock Loop	Inhibits VCO in PLL when "0" (low), enables VCO when "1."
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output	Phase Lock Loop	MFM mode when "1," FM mode when "0."
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high), Head 0 selected when "0" (low).
28,29	US_1,US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WDA	Write Data	Output	FDD	Serial clock and data bits to FDD.
31,32	PS_1,PS_0	Precompensation (pre-shift)	Output	FDD	Write precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/ Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode.
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Fit Reset/Step	Output	FDD	Resets fault F.F. in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			DC Power.

Note: (1) Disabled when CS = 1.

CAPACITANCE

$T_a = 25°C$; $f_c = 1$ MHz; $V_{CC} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Capacitance	$C_{IN(\Phi)}$			20	pF	All Pins Except Pin Under Test Tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP①	MAX		
Clock Period	Φ_{CY}	120	125	500	ns	
Clock Active (High, Low)	Φ_0	40			ns	
Clock Rise Time	Φ_r			20	ns	
Clock Fall Time	Φ_f			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓	T_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑	T_{RA}	0			ns	
$\overline{RD}$ Width	T_{RR}	250			ns	
Data Access Time from $\overline{RD}$ ↓	T_{RD}			200	ns	C_L = 100 pf
DB to Float Delay Time from $\overline{RD}$ ↑	T_{DF}	20		100	ns	C_L = 100 pF
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓	T_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑	T_{WA}	0			ns	
$\overline{WR}$ Width	T_{WW}	250			ns	
Data Set Up Time to $\overline{WR}$ ↑	T_{DW}	150			ns	
Data Hold Time from $\overline{WR}$ ↑	T_{WD}	5			ns	
INT Delay Time from $\overline{RD}$ ↑	T_{RI}			500	ns	
INT Delay Time from $\overline{WR}$ ↑	T_{WI}			500	ns	
DRQ Cycle Time	T_{MCY}	13			μs	
DRQ Delay Time from $\overline{DACK}$ ↓	T_{AM}			200	ns	
TC Width	T_{TC}	1			ΦCY	
Reset Width	T_{RST}	14			ΦCY	
WCK Cycle Time	T_{CY}		2 or 4② 1 or 2		μs	MFM = 0 MFM = 1
WCK Active Time (High)	T_0	80	250	350	ns	
WCK Rise Time	T_r			20	ns	
WCK Fall Time	T_f			20	ns	
Pre-Shift Delay Time from WCK ↑	T_{CP}	20		100	ns	
WDA Delay Time from WCK ↑	T_{CD}	20		100	ns	
RDD Active Time (High)	T_{RDD}	40			ns	
Window Cycle Time	T_{WCY}		2.0 1.0		μs	MFM = 0 MFM = 1
Window Hold Time to/from RDD	T_{RDW} T_{WRD}	15			ns	
$US_{0,1}$ Hold Time to $\overline{RW}$/SEEK ↑	T_{US}	12			μs	8 MHz Clock Period
SEEK/RW Hold Time to LOW CURRENT/DIRECTION ↑	T_{SD}	7			μs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑	T_{DST}	1.0			μs	
$US_{0,1}$ Hold Time from FAULT RESET/STEP ↑	T_{STU}	5.0			μs	
STEP Active Time (High)	T_{STP}	6.0	7.0		μs	
STEP Cycle Time	T_{SC}	33	③	③	μs	
FAULT RESET Active Time (High)	T_{FR}	8.0		10	μs	
Write Data Width	T_{WDD}	T_0-50			ns	
$US_{0,1}$ Hold Time After SEEK	T_{SU}	15			μs	8 MHz Clock Period
Seek Hold Time from DIR	T_{DS}	30			μs	
DIR Hold Time after STEP	T_{STD}	24			μs	
Index Pulse Width	T_{IDX}	10			ΦCY	
$\overline{RD}$ ↓ Delay from DRQ	T_{MR}	800			ns	8 MHz Clock Period
$\overline{WR}$ ↓ Delay from DRQ	T_{MW}	250			ns	
$\overline{WE}$ or $\overline{RD}$ Response Time from DRQ ↑	T_{MRW}			12	μs	

Notes: ① Typical values for T_a = 25°C and nominal supply voltage.

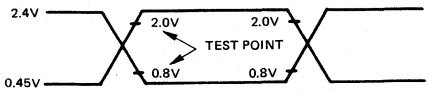
② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy.

③ Under Software Control. The range is from 1 ms to 16 ms at 8 MHz Clock Period, and 2 to 32 ms at 4 MHz Clock Period.

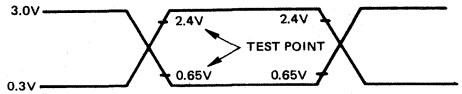
④ For mini-floppy applications, Φ_{CY} must be 4 mHz.

AC TEST CONDITION

INPUT/OUTPUT



CLOCK



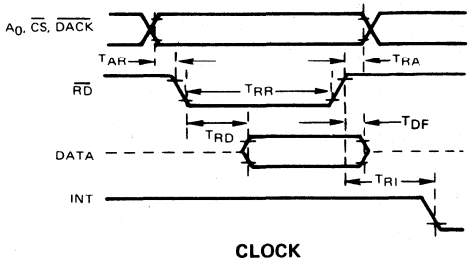
AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

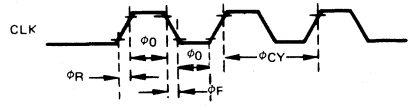
Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

TIMING WAVEFORMS

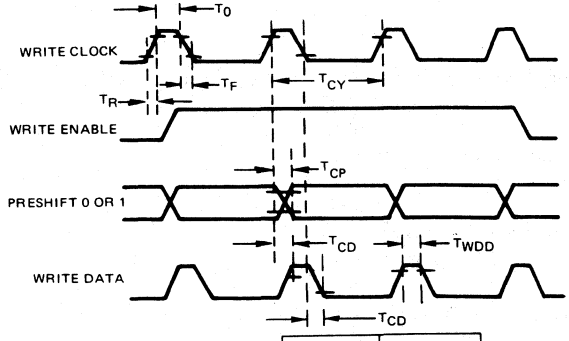
PROCESSOR READ OPERATION



CLOCK

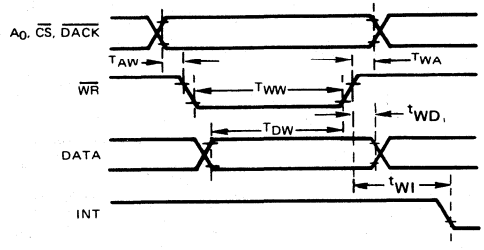


FDD WRITE OPERATION

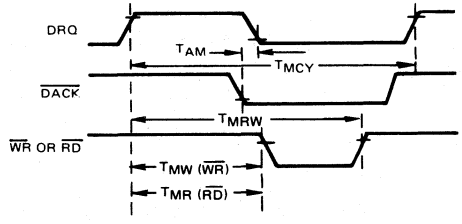


	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

PROCESSOR WRITE OPERATION



DMA OPERATION



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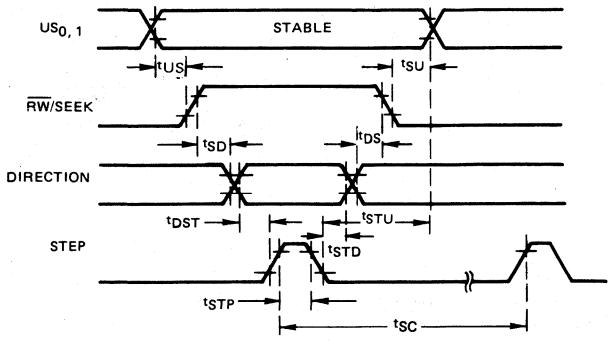
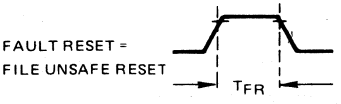
TIMING WAVEFORMS (CONT.)

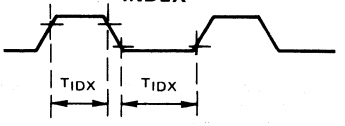
SEEK OPERATION



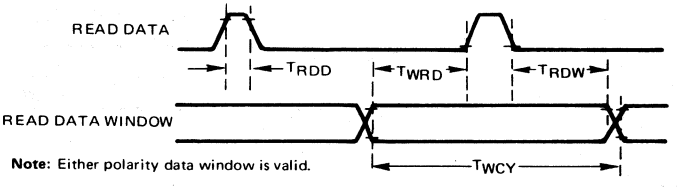
FLT RESET



INDEX

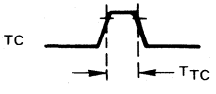


FDD READ OPERATION

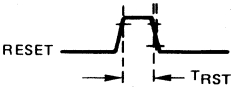


Note: Either polarity data window is valid.

TERMINAL COUNT



RESET



INTERNAL REGISTERS

The μPD765 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and μPD765.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

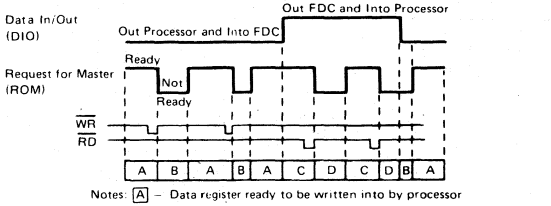
A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

INTERNAL REGISTERS (CONT.)

The bits in the Main Status Register are defined as follows:

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC Busy) goes low is 12 μs.



Notes: [A] – Data register ready to be written into by processor
[B] – Data register not ready to be written into by processor
[C] – Data register ready for next data byte to be read by the processor
[D] – Data register not ready for next data byte to be read by processor

COMMAND SEQUENCE

The μPD765 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the μPD765 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

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PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT.
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information read during Execution Phase from Floppy Disk
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: ① Symbols used in this table are described at the end of this section.

② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
SCAN HIGH OR EQUAL										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	STO								Status information at the end of seek-operation about the FDC
	R	PCN								
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT						HUT		
	W	HLT						ND		
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	ST 3								Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	NCN								
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W	Invalid Codes								Invalid Command Codes (NoOp — FDC goes into Standby State)
Result	R	ST 0								ST 0 = 80 (16)

COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1)
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop date transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.

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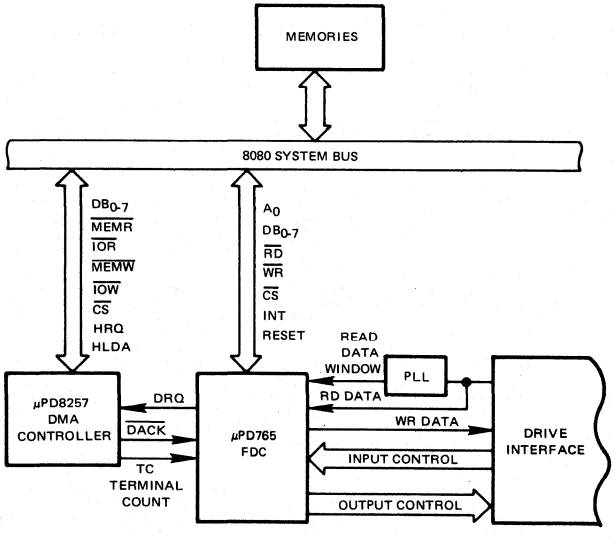
COMMAND SYMBOL DESCRIPTION (CONT.)

SYMBOL	NAME	DESCRIPTION
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

SYSTEM CONFIGURATION



PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command.

POLLING FEATURE OF THE μPD765

After the Specify command has been sent to the μPD765, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the μPD765 polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the μPD765 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the μPD765 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: 1 NC (No Change): The same value as the one at the beginning of command execution.

2 LSB (Least Significant Bit): The least significant bit of H is complemented.

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

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READ A TRACK

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

	8" STANDARD FLOPPY					5¼" MINI FLOPPY				
FORMAT	SECTOR SIZE	N	SC	GPL ①	GPL ②	SECTOR SIZE	N	SC	GPL ①	GPL ②
FM Mode	128 bytes/Sector	00	1A	07	1B	128 bytes/Sector	00	12	07	09
	256	01	0F	0E	2A	128	00	10	10	19
	512	02	08	1B	3A	256	01	08	18	30
	1024 bytes/Sector	03	04	47	8A	512	02	04	46	87
	2048	04	02	C8	FF	1024	03	02	C8	FF
	4096	05	01	C8	FF	2048	04	01	C8	FF
MFM Mode	256	01	1A	0E	36	256	01	12	0A	0C
	512	02	0F	1B	54	256	01	10	20	32\
	1024	03	08	35	74	512	02	08	2A	50
	2048	04	04	99	FF	1024	03	04	80	F0
	4096	05	02	C8	FF	2048	04	02	C8	FF
	8192	06	01	C8	FF	4096	05	01	C8	FF

Table 3

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

③ In MFM mode FDC can not perform a read/write/format operation with 128 bytes/sector. (N = 00)

④ All the values are hexidecimal.

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidicemial byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)
PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits DB_0-DB_3 in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

RECALIBRATE

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulse have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the μPD765 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the μPD765 is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find a 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

STATUS REGISTER IDENTIFICATION

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 0			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit. Number at Interrupt.
D_0	Unit Select 0	US 0	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

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STATUS REGISTER IDENTIFICATION (CONT.)

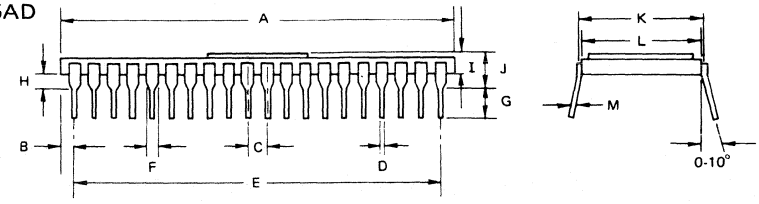
BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 1 (CONT.)			
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

It is suggested that you utilize the following applications notes:

① #8 — for an example of an actual interface, as well as a "theoretical" data separator.

② #10 — for a well documented example of a working phase lock loop.

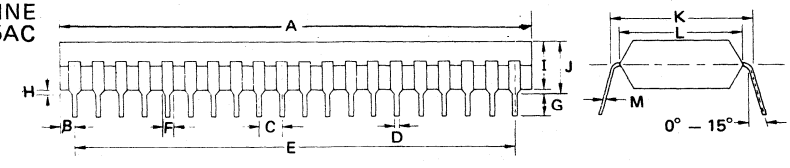
PACKAGE OUTLINE
μPD765AD



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

PACKAGE OUTLINE
μPD765AC



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

765ADS-REV3-1-82-CAT

9

8-BIT SERIAL OUTPUT A/D CONVERTER

DESCRIPTION

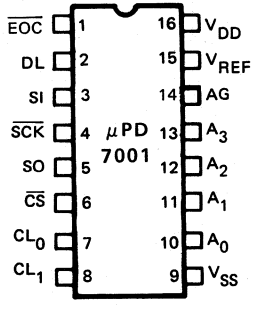
The μPD7001 is a high performance, low power 8-bit CMOS A/D converter which consists of a 4 channel analog multiplexer, and a digital interface circuit for serial data I/O. The NEC μPD7001 A/D converter uses successive approximation as a conversion technique.

An A/D conversion system can be easily designed with the μPD7001 including all circuits for A/D conversion. The μPD7001 can be directly connected to 8-bit or 4-bit microprocessors.

FEATURES

- Single chip A/D Converter
- Resolution: 8 Bit
- 4 Channel Analog Multiplexer
- Auto-Zeroscale and Auto-Fullscale Corrections without any external components
- Serial Data Transmission
- High Input Impedance: 1,000 MΩ
- Single +5V Power Supply
- Low Power Operation
- Available in 16 Pin Plastic Package
- Conversion Speed 140 μs Typ.

PIN CONFIGURATION



(TOP VIEW)

PIN NAMES

$\overline{EOC}$*	End of Conversion
DL	Analog Channel Data Load
SI	Serial Data Input
$\overline{SCK}$	Serial Data Clock
SO*	Serial Data Output
$\overline{CS}$	Chip Select
CL_0,CL_1	Successive Approximation Clock
V_{SS}	Digital Ground
A_0,A_1,A_2,A_3	Analog Inputs
AG	Analog Ground
V_{REF}	Reference Voltage Input
V_{DD}	+5V

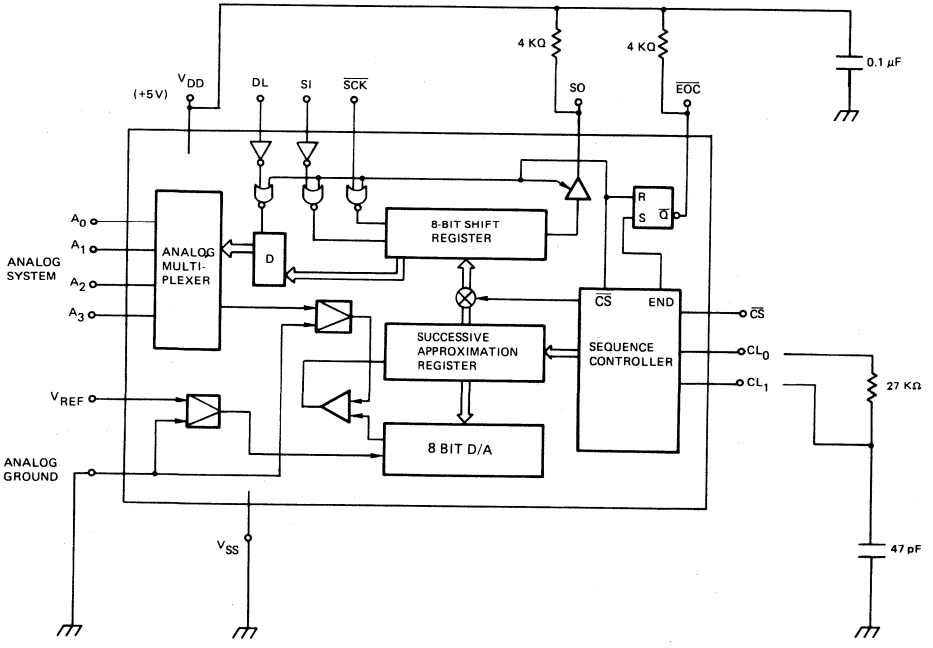
*Open Drain

9

FUNCTIONAL DESCRIPTION

The 4 channel analog inputs are selected by a 2-bit signal which is applied to a serial input and latched with a DL signal. The converted 8-bit digital signals are output from an open collector serial output (SO). The serial digital signals are synchronized with an external clock applied to a $\overline{SCK}$ terminal. The internal sequence controller controls A/D conversion by initiating a conversion cycle at a rise of the Chip Select ($\overline{CS}$). At the final step of each A/D conversion cycle the converted data is transmitted to an 8-bit shift register and immediately the next conversion cycle is started. This step results in storage of the newest data in a shift register. At the final step of the first A/D conversion cycle, an end of conversion signal ($\overline{EOC}$) is output indicating that the converted data is stored in a shift register. At a low level (active) of the chip select, the sequence controller and $\overline{EOC}$ are reset and the A/D conversion is stopped.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-0°C to +70°C
Storage Temperature	-65°C to +150°C
Analog Input Voltage	-0.3 to V_{DD} +0.3 Volts
Reference Input Voltage	-0.3 to V_{DD} +0.3 Volts
Digital Input Voltage	-0.3 to +12 Volts
Max. Pull-up Voltage	+12 Volts
Supply Voltages	-0.3 to +7 Volts
Power Dissipation	200 mW

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_a = 25 ± 2°C; f_{CK} = 400 kHz; V_{DD} = +5V; ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
$\overline{EOC}$ Hold Time	t_{HECS}	0			μs	$\overline{EOC}$ to $\overline{CS}$
$\overline{CS}$ Setup Time	t_{SCSK}	12.5			μs	$\overline{CS}$ to $\overline{SCK}$, ①
Address Data Setup Time	t_{SIK}	150			ns	
Address Data Hold Time	t_{HKI}	100			ns	
High Level Serial Clock Pulse Width	t_{WHK}	400			ns	
Low Level Serial Clock Pulse Width	t_{WLK}	400			ns	
Data Latch Hold Time	t_{HKDL}	200			ns	$\overline{SCK}$ to DL
Data Latch Pulse Width	t_{WHDL}	200			ns	
Serial Data Delay Time	t_{DKO}			500	ns	$\overline{SCK}$ to SO, R_L = 3K, ② C_L = 30 pF
Delay Time to Floating SO	t_{FCSO}			250	ns	$\overline{CS}$ to High Impedance SO
$\overline{CS}$ Hold Time	t_{HKCS}	200			ns	

Notes: ① At a low level of $\overline{CS}$ the data is exchanged with external digital circuit and at a high level of $\overline{CS}$ the μPD7001 performs A/D conversion and does not accept any external digital signal. However, 5 pulses of internal clock are needed before digital data output and then the μPD7001 remains at the previous state of high level $\overline{CS}$.

The rating corresponds to the 5 pulses of clock signal.

t_{SCSK} (Min.) = $5/f_{CK}$

② The serial data delay time depends on load capacitance and pull-up resistance.

DC CHARACTERISTICS

T_a = 25 ± 2°C; V_{DD} = +5V ± 10%; V_{REF} = 2.5V; f_{CK} = 400 kHz.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Resolution			8		Bit	V_{DD} = 5V V_{REF} = 2.25 to 2.75V
Non Linearity				0.8	%FSR	V_{DD} = 5V V_{REF} = 2.25 to 2.75V
Full-Scale Error				2	LSB	V_{DD} = 5V V_{REF} = 2.25 to 2.75V
Full-Scale Error Temp. Coefficient			30		ppm/°C	V_{DD} = 5V V_{REF} = 2.25 to 2.75V
Zero Error				2	LSB	V_{DD} = 5V V_{REF} = 2.25 to 2.75V
Zero Error Temp. Coefficient			30		ppm/°C	V_{DD} = 5V V_{REF} = 2.25 to 2.75V
Total Unadjusted Error 1	T.U.E. 1			2	LSB	V_{DD} = 5V V_{REF} = 2.25 to 2.75V
Total Unadjusted Error 2	T.U.E. 2			2	LSB	V_{DD} = 4.5 to 5.5V V_{REF} = 2.5V
Analog Input Voltage	V_I	0		V_{REF}	V	①
Analog Input Resistance	R_I		1000		MΩ	V_I = 0 to V_{DD}
Conversion Time	t_{CONV}		140		μs	②
Clock Frequency Range	f_{CK}	0.01	0.4	0.5	MHz	
Clock Frequency Distribution	Δf_{CK}		±5	±20	%	R = 27 KΩ, C = 47 pF (f_{CK} = 0.4 MHz)
Serial Clock Frequency	f_{SCK}			1	MHz	③
High Level Voltage	V_{IH}	3.6			V	
Low Level Voltage	V_{IL}			1.4	V	
Digital Input Leakage Current	I_I		1.0	10	μA	V_I = V_{SS} to +12V
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.7 mA
Output Leakage Current	I_L		1.0	10	μA	V_O = +12V
Power Dissipation	P_d		5	15	mW	

Notes: ① All digital outputs are put at a high level when $V_I > V_{REF}$.

② The A/D conversion is started with CS going to a high level and at the final step of the first A/D conversion the EOC is at a low.

The conversion time is:

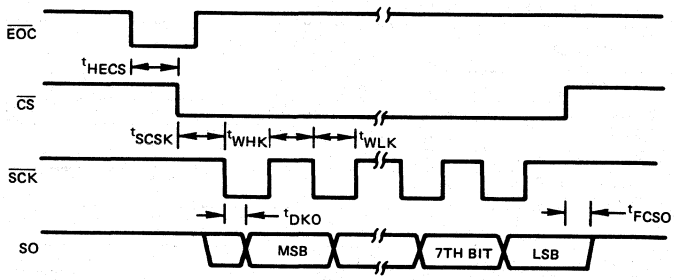
$t_{CONV} = 14 \times 4 \times 1/f_{CK}$

③ For f_{SCK} > 500 kHz, the load capacitor (stray capacitance included) and the pull-up resistor which are connected to serial output are required to be not more than 30 pF and 4 KΩ respectively.

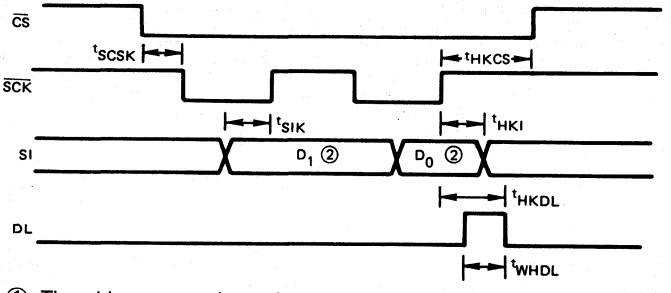
9

TIMING WAVEFORMS

DIGITAL DATA OUTPUT



ANALOG CHANNEL SELECTION



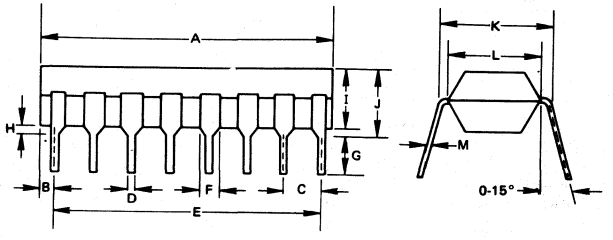
Notes: ① The address set can be performed simultaneously with the digital data outputting.

② Analog Multiplexer Channel Selections:

Analog Input Address	D_0	D_1
A_0	L	L
A_1	H	L
A_2	L	H
A_3	H	H

③ Rise and fall time of the above waveforms should not be more than 50 ns.

PACKAGE OUTLINE μPD7001C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

10-BIT BINARY A/D CONVERTER

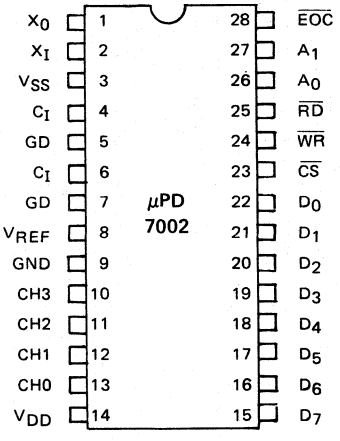
DESCRIPTION

The μPD7002 is a high performance, low power, monolithic CMOS A/D converter designed for microprocessor applications. The analog input voltage is applied to one of the four analog inputs. By loading the input register with the multiplexer channel and the desired resolution (8 or 10 bits) the integrating A/D conversion sequence is started. At the end of conversion $\overline{EOC}$ signal goes low and if connected to the interrupt line of microprocessor it will cause an interrupt. At this point the digital data can be read in two bytes from the output registers. The μPD7002 also features a status register that can be read at any time.

FEATURES

- Single Chip CMOS LSI
- Resolution: 8 or 10 Bits
- 4 Channel Analog Multiplexer
- Auto-Zeroscale and Auto-Fullscale Corrections without any External Components
- High Input Impedance: 1000MΩ
- Readout of Internal Status Register Through Data Bus
- Single +5V Power Supply
- Interfaces to Most 8-Bit Microprocessors
- Conversion Speed: 5 ms (10 Bit, f_{CK} = 2 MHz)
- Power Consumption: 15 mW
- Available in a 28 Pin Plastic Package
- 2 Performance Ranges
  Conversion Accuracy (Max) T_a = 0° to 50°C
  μPD7002C-1; 0.1% FSR
  μPD7002C ; 0.2% FSR

PIN CONFIGURATION

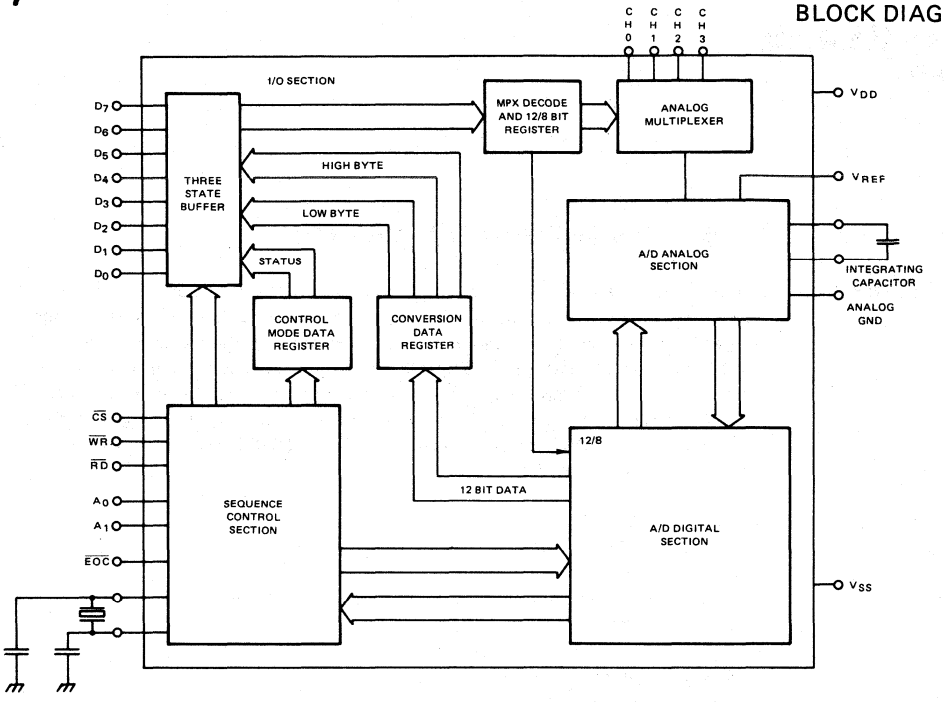


PIN NAMES

X_0,X_I	External Clock Input
V_{SS}	TTL Ground
C_I	Integrating Capacitor
GD	Guard
V_{REF}	Reference Voltage Input
GND	Analog Ground
CH3	Analog Channel 3
CH2	Analog Channel 2
CH1	Analog Channel 1
CH0	Analog Channel 0
V_{DD}	TTL Voltage (+5V)
D_0-D_7	Data Bus
$\overline{CS}$	Chip Select
$\overline{WR}$, $\overline{RD}$	Control Bus
A_0,A_1	Address Bus
$\overline{EOC}$	End of Conversion Interrupt

9

BLOCK DIAGRAM



DC CHARACTERISTICS

T_a = 0 to 50°C; V_{DD} = +5 ±0.25V, V_{REF} = +2.50V, f_{CK} = 1 MHz

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Resolution	7002C-1		10	11	12	Bits	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
	7002C		9	11	12		
Non Linearity	7002C-1			0.05	0.1	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
	7002C			0.1	0.2		
Fullscale Error	7002C-1			0.05	0.1	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
	7002C			0.1	0.2		
Zeroscale Error	7002C-1			0.05	0.1	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
	7002C			0.1	0.2		
Fullscale Temperature Coefficient				10		PPM/°C	V_{DD} = 5V
Zeroscale Temperature Coefficient				10		PPM/°C	V_{DD} = 5V
Analog Input Voltage Range		V_{IA}	0		V_{REF}	V	
Analog Input Resistance		R_{IA}		1000		MΩ	V_{IA} = V_{SS} to V_{DD}
Total Unadjusted Error 1	7002C-1	T.U.E. 1		0.05	0.1	%FSR	V_{REF} = 2.25 to 2.75V, V_{DD} = 5V
	7002C	T.U.E. 1		0.1	0.2		
Total Unadjusted Error 2	7002C-1	T.U.E. 2		0.05	0.1	%FSR	V_{REF} = 2.5V, V_{DD} = 4.75 to 5.25V
	7002C	T.U.E. 2		0.1	0.2		
Clock Input Current		I_{XI}		5	50	μA	
Clock Input High Level		V_{XIH}	V_{DD}-1.4			V	
Clock Input Low Level		V_{XIL}			V_{SS}+1.4	V	
High Level Input Voltage		V_{IH}	2.2			V	T_a = −20°C to +70°C
Low Level Input Voltage		V_{IL}			0.8	V	T_a = −20°C to +70°C
High Level Output Voltage		V_{OH}	V_{DD}-1.5			V	I_O = −1.6 mA, T_a = −20°C to +70°C
Low Level Output Voltage		V_{OL}			0.45	V	I_O = +16 mA, T_a = −20°C to +70°C
Digital Input Leakage Current		I_I		1	10	μA	V_I = V_{SS} to V_{DD}
High-Z Output Leakage Current		I_{Leak}		1	10	μA	V_O = V_{SS} to V_{DD}
Power Dissipation		Pd		15	25	mW	f_{CK} ≤ 1 MHz

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −20°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Input Voltages . . . . . −0.3 to V_{DD} + 0.3 Volts
Power Supply . . . . . −0.3 to +7 Volts
Power Dissipation . . . . . 300 mW
Analog GND Voltage . . . . . V_{SS} ± 0.3 Volts
T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

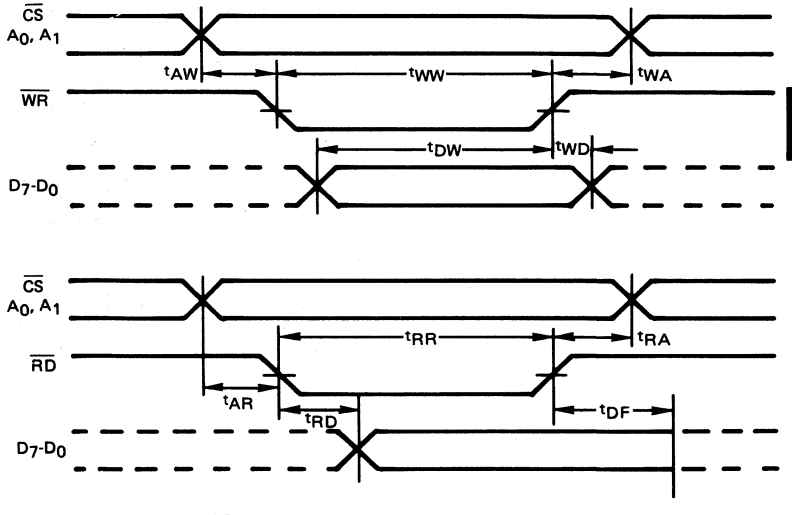
AC CHARACTERISTICS

T_a = 25° ± 2°C; V_{DD} = +5 ± 0.25V; V_{REF} = 2.5V; f_{CK} = 1 MHz; C_{INT} = 0.033 μF

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Conversion Speed (12 bit)	t_{CONV}	8.5	10	15	ms	f_{CK} = 1 MHz
Conversion Speed (8 bit)	t_{CONV}	2.4	4	5	ms	f_{CK} = 1 MHz
Clock Frequency Range	f_{CK}	0.5	1	3	MHz	
Integrating Capacitor Value	C_{INT}*	0.029			μF	V_{REF} = 2.50V, f_{CK} = 1 MHz
Address Setup Time $\overline{CS}$, A_0, A_1, to $\overline{WR}$	t_{AW}	50			ns	
Address Setup Time $\overline{CS}$, A_0, A_1, to $\overline{RD}$	t_{AR}	50			ns	
Address Hold Time $\overline{WR}$ to CS, A_0, A_1	t_{WA}	50			ns	
Address Hold Time $\overline{RD}$ to CS, A_0, A_1	t_{RA}	50			ns	
Low Level $\overline{WR}$ Pulse Width	t_{WW}	400			ns	
Low Level $\overline{RD}$ Pulse Width	t_{RR}	400			ns	
Data Setup Time Input Data to $\overline{WR}$	t_{DW}	300			ns	
Data Hold Time $\overline{WR}$ to Input Data	t_{WD}	50			ns	
Output Delay Time $\overline{RD}$ to Output Data	t_{RD}			300	ns	1TTL + 100 pF
Delay Time to High Z Output $\overline{RD}$ to Floating Output	t_{DF}			150	ns	

* $C_{INT}(\mu F)(Min) = 0.029/f_{CK}(MHz)$

TIMING WAVEFORMS



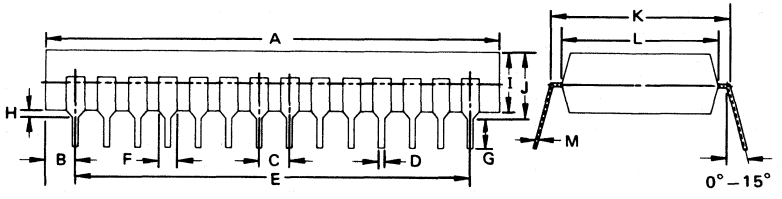
CONTROL TERMINAL FUNCTIONS

CONTROL TERMINALS					MODE	INTERNAL FUNCTION	DATA INPUT-OUTPUT TERMINALS
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0			
H	x	x	x	x	Not selected		High impedance
L	H	H	x	x	Not selected	–	
L	H	L	L	L	Write mode	Data latch A/D start	Input status, D_1, D_0 = MPX address D_3 = 8 bit/10 bit conversion designation. ① D_2 = Flag Input
L	H	L	L	H	Not selected	–	High impedance
L	H	L	H	L	Not selected	–	
L	H	L	H	H	Test mode	Test status	Input status ②
L	L	H	L	L	Read mode	Internal status	D_7 = $\overline{EOC}$, D_6 = $\overline{BUSY}$, D_5 = MSB, D_4 = 2nd MSB, D_3 = 8/10, D_2 = not used D_1 = MPX, D_0 = MPX
L	L	H	L	H	Read mode	High data byte	D_7-D_0 = MSB – 8th bit
L	L	H	H	L	Read mode	Low data byte	D_7-D_4 = 9th – 10th bit, D_3-D_0 = L
L	L	H	H	H	Read mode	Low data byte	

Notes: ① Designation of number of conversion bits: 8 bit = L; 10 bit = H.

② Test Mode: Used for inspecting the device. The data input-output terminals assume an input state and are connected to the A/D counter. Therefore, the A/D conversion data read out after this is meaningless.

PACKAGE OUTLINE μPD7002C



PLASTIC

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

MULTI-PROTOCOL SERIAL CONTROLLER

DESCRIPTION

The μPD7201 is a dual-channel multi-function peripheral controller designed to satisfy a wide variety of serial data communication requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller and within that role it is configurable by systems software so its "personality" can be optimized for a given serial data communications application.

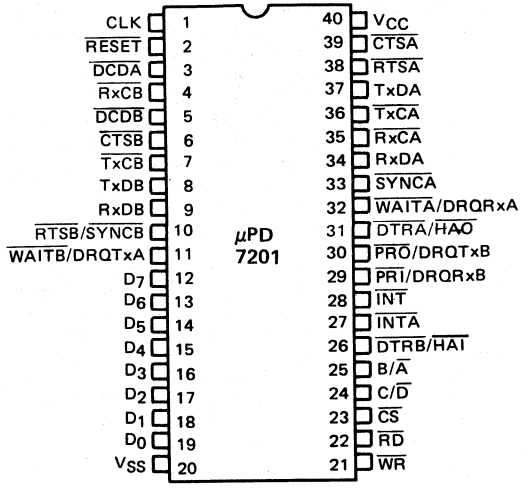
The μPD7201 is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for applications other than data communications.

The μPD7201 can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

FEATURES

- Two Fully Independent Duplex Serial Channels
- Four Independent DMA Channels for Send/Received Data for Both Serial Inputs/Outputs
- Programmable Interrupt Vectors and Interrupt Priorities
- Modem Controls Signals
- Variable, Software Programmable Data Rate, Up to 880K Baud at 4 MHz Clock
- Double Buffered Transmitter Data and Quadruply Buffered Received Data
- Programmable CRC Algorithm
- Selection of Interrupt, DMA or Polling Mode of Operation
- Asynchronous Operation:
  - Character Length: 5, 6, 7 or 8 Bits
  - Stop Bits: 1, 1-1/2, 2
  - Transmission Speed: x1, x16, x32 or x64 Clock Frequency
  - Parity: Odd, Even, or Disable
  - Break Generation and Detection
  - Interrupt on Parity, Overrun, or Framing Errors
- Monosync, Bisync, and External Sync Operations:
  - Software Selectable Sync Characters
  - Automatic Sync Insertion
  - CRC Generation and Checking
- HDLC and SDLC Operations:
  - Abort Sequence Generation and Detection
  - Automatic Zero Insertion and Detection
  - Address Field Recognition
  - CRC Generation and Checking
  - I-Field Residue Handling
- N-Channel MOS Technology
- Single +5V Power Supply; Interface to Most Microprocessors Including 8080, 8085, 8086 and Others.
- Single Phase TTL Clock
- Available in Plastic and Ceramic Dual-in-Line Packages

PIN CONFIGURATION



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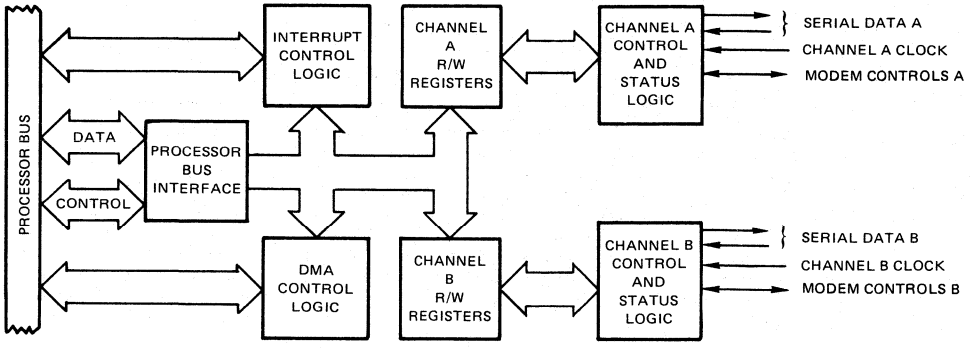
PIN DESCRIPTION

NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
12-19	D_0-D_7	System Data Bus (bidirectional, 3-state)	The system data bus transfers data and commands between the processor and the μPD7201. D_0 is the least significant bit.
25	B/$\overline{A}$	Channel A or B Select (input, High selects Channel B)	This input defines which channel is accessed during a data transfer between the processor and the μPD7201.
24	C/$\overline{D}$	Control or Data Select (input, High selects Control)	This input defines the type of information transfer performed between the processor and the μPD7201. A High at this input during a processor write to or read from the μPD7201 causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A low at C/$\overline{D}$ means that the information on the data bus is data.
23	$\overline{CS}$	Chip Select (input, active Low)	A low level at this input enables the μPD7201 to accept command or data inputs from the processor during a write cycle, or to transmit data to the processor during a read cycle.
1	CLK	System Clock (input)	The μPD7201 uses standard TTL clock.
22	$\overline{RD}$	Read (input active Low)	If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with C/$\overline{D}$, B/$\overline{A}$ and $\overline{CS}$ to transfer data from the μPD7201 to the processor or the memory.
21	$\overline{WR}$	Write (input, active Low)	The $\overline{WR}$ signal is used to control the transfer of either command or data from the processor or the memory to the μPD7201.
2	$\overline{RESET}$	Reset (input, active Low)	A low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls high and disables all interrupts. The control registers must be rewritten after the μPD7201 is reset and before data is transmitted or received. $\overline{RESET}$ must be active for a minimum of one complete CLK cycle.
10,38	$\overline{RTSA}$, $\overline{RTSB}$	Request to Send (outputs, active Low)	When the $\overline{RTS}$ bit is set, the $\overline{RTS}$ output goes Low. When the $\overline{RTS}$ bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the state of the $\overline{RTS}$ bit. Both pins can be used as general-purpose outputs.
10,33	$\overline{SYNCA}$, $\overline{SYNCB}$	Synchronization (inputs/outputs, active Low)	These pins can act either as inputs or outputs. In the Asynchronous Receive mode, they are inputs similar to $\overline{CTS}$ and $\overline{DCD}$. In this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, $\overline{SYNC}$ must be driven Low on the second rising edge of $\overline{RxC}$ after that rising edge of $\overline{RxC}$ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the $\overline{SYNC}$ input. Once $\overline{SYNC}$ is forced Low, it is wise to keep it Low until the processor informs the external sync logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of $\overline{RxC}$ that immediately precedes the falling edge of $\overline{SYNC}$ in the External Sync mode. In the Internal Synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock ($\overline{RxC}$) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.
26,31	$\overline{DTRA}$, $\overline{DTRB}$	Data Terminal Ready (outputs, active Low)	These outputs follow the state programmed into the DTR bit. They can also be programmed as general-purpose outputs.

PIN DESCRIPTION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	DESCRIPTION
27	$\overline{INTA}$	Interrupt Acknowledge (input, active Low)	This signal is generated by the processor and is sent to all peripheral devices. It serves to acknowledge the interrupt and to allow the highest priority interrupting device to put an 8-bit vector on the bus. $\overline{INT}$ and $\overline{INTA}$ are compatible with the fully nested option of the μPD8259A-5.
29	$\overline{PRI}$	Priority In (input, active Low)	These signals are daisy chained through the peripheral device controllers. The signal on these lines is intact until a device with a pending interrupt request is found on the chain. After that device, this signal holds off lower priority device interrupts. A higher priority device can interrupt the processing of an interrupt from a lower priority device, provided the processor has interrupts enabled. $\overline{PRI}$ is used with $\overline{PRO}$ to form a priority daisy chain when there is more than one interrupt-driven device. A Low on this line indicates that no other device of higher priority is being serviced by a processor interrupt service routine. $\overline{PRO}$ is Low only if $\overline{PRI}$ is Low and the processor is not servicing an interrupt from the μPD7201. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its processor interrupt service routine.
30	$\overline{PRO}$	Priority Out (output, active Low)	
11,29, 30,32	DRQTxA, DRQTxB DRQRxA, DRQRxB	DMA Request (outputs, active High)	These signals are generated by the receiver or transmitter of Channel A and Channel B. These signals can be connected to most DMA Controllers directly and are used for handshaking during DMA transfer.
26	$\overline{HAI}$	DMA Acknowledge (input, active Low)	Typically, the HLDA signal driven from the processor is input to the $\overline{HAI}$ terminal of the highest priority μPD7201, and the $\overline{HAO}$ output of that μPD7201 is daisy chained to the $\overline{HAI}$ input of the lower priority μPD7201 and propagated downstream. $\overline{HAI}$ and $\overline{HAO}$ signals provide acknowledgement for the highest priority outstanding DMA request.
31	$\overline{HAO}$	DMA Acknowledge (output, active Low)	
28	$\overline{INT}$	Interrupt Request (output, open collector, active Low)	When the μPD7201 is requesting an interrupt, it pulls $\overline{INT}$ low.
11,32	$\overline{WAITA}$, $\overline{WAITB}$	(Outputs, open drain)	Wait lines for both channels that synchronize the processor to the μPD7201 data rate. The reset state is open drain.
6,39	$\overline{CTSA}$, $\overline{CTSB}$	Clear to Send (inputs, active Low)	When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime inputs. The μPD7201 detects pulses on these inputs and interrupts the processor on both logic level transitions. The Schmitt-trigger inputs do not guarantee a specified noise-level margin.
3,5	$\overline{DCDA}$, $\overline{DCDB}$	Data Carrier Detect (inputs, active Low)	These signals are similar to the $\overline{CTS}$ inputs, except they can be used as receiver enables.
9,34	RxDA, RxDB	Receive Data (inputs, active High)	
8,37	TxDA, TxDB	Transmit Data (outputs, active High)	
4,35	$\overline{RxCA}$, $\overline{RxCB}$	Receiver Clocks (inputs)	The Receiver Clocks may be 1, 16, 32, or 64 times the data rate in asynchronous modes. Receive data is sampled on the rising edge of $\overline{RxC}$.
7,36	$\overline{TxCA}$, $\overline{TxCB}$	Transmitter Clocks (inputs)	In asynchronous modes, the Transmitter Clocks may be 1, 16, 32, or 64 times the data rate. The multiplier for the transmitter and the receiver must be the same. Both $\overline{TxC}$ and $\overline{RxC}$ inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise margin is specified). TxD changes on the falling edge of $\overline{TxC}$. Note that $\overline{TxC}$ and $\overline{RxC}$ in Channel B are on a common pin, $\overline{RxCB}/\overline{TxCB}$.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0° to +70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin . . . . . -0.5 to +7 Volts ①

Note: ① With respect to ground.

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	+0.8	V	
Input High Voltage	V_{IH}	+2.0	V_{CC}+0.5	V	
Output Low Voltage	V_{OL}		+0.45	V	I_{OL} = +2.0 mA
Output High Voltage	V_{OH}	+2.4		V	I_{OH} = -200 μA
Input Leakage Current	I_{IL}		±10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{OL}		±10	μA	V_{OUT} = V_{CC} to 0V
V_{CC} Supply Current	I_{CC}		180	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

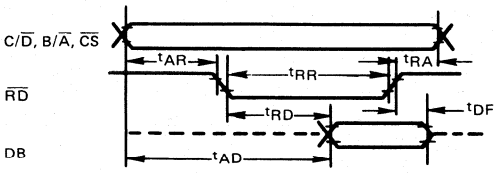
PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		10	pF	fc = 1 MHz
Output Capacitance	C_{OUT}		15	pF	Unmeasured pins Returned to GND
Input/Output Capacitance	$C_{I/O}$		20	pF	

AC CHARACTERISTICS T_a = 0°C to +70°C; V_{CC} = +5V ±10%

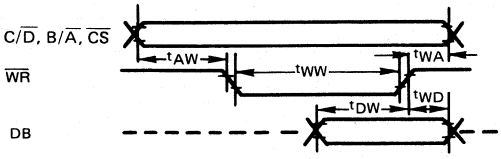
PARAMETER	SYMBOL	LIMITS		UNIT
		MIN	MAX	
Clock Cycle	t_{CY}	250	4000	ns
Clock High Width	t_{CH}	105	2000	ns
Clock Low Width	t_{CL}	105	2000	ns
Clock Rise and Fall Time	t_r, t_f	0	30	ns
Address Setup to $\overline{RD}$	t_{AR}	0		ns
Address Hold from $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ Pulse Width	t_{RR}	250		ns
Data Delay from Address	t_{AD}		200	ns
Data Delay from $\overline{RD}$	t_{RD}		200	ns
Output Float Delay	t_{DF}	10	100	ns
Address Setup to $\overline{WR}$	t_{AW}	0		ns
Address Hold from $\overline{WR}$	t_{WA}	0		ns
$\overline{WR}$ Pulse Width	t_{WW}	250		ns
Data Setup to $\overline{WR}$	t_{DW}	150		ns
Data Hold from $\overline{WR}$	t_{WD}	0		ns
$\overline{PRO}$ Delay from $\overline{INTA}$	t_{IAPO}		200	ns
$\overline{PRI}$ Setup to $\overline{INTA}$	t_{PIN}	0		ns
$\overline{PRI}$ Hold from $\overline{INTA}$	t_{IP}	0		ns
$\overline{INTA}$ Pulse Width	t_{II}	250		ns
$\overline{PRO}$ Delay from $\overline{PRI}$	t_{PIPO}		100	ns
Data Delay from $\overline{INTA}$	t_{ID}		200	ns
Request Hold from $\overline{RD}/\overline{WR}$	t_{CQ}		150	ns
$\overline{HAI}$ Setup to $\overline{RD}/\overline{WR}$	t_{LR}	300		ns
$\overline{HAI}$ Hold from $\overline{RD}/\overline{WR}$	t_{RL}	0		ns
$\overline{HAO}$ Delay from $\overline{HAI}$	t_{HIHO}		100	ns
Recovery Time Between Controls	t_{RV}	300		ns
$\overline{WAIT}$ Delay from Address	t_{CW}		120	ns
Data Clock Cycle	t_{DCY}	400		ns
Data Clock Low Width	t_{DCL}	180		ns
Data Clock High Width	t_{DCH}	180		ns
Tx Data Delay	t_{TD}		300	ns
Data Set up to $\overline{RxC}$	t_{DS}	0		ns
Data Hold from $\overline{RxC}$	t_{DH}	140		ns
$\overline{INT}$ Delay Time from $\overline{TxC}$	t_{ITD}		4 ~ 6	t_{CY}
$\overline{INT}$ Delay Time from $\overline{RxC}$	t_{IRD}		7 ~ 11	t_{CY}
Low Pulse Width	t_{PL}	200		ns
High Pulse Width	t_{PH}	200		ns
External $\overline{INT}$ from $\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$	t_{IPD}		500	ns
Delay from $\overline{RxC}$ to $\overline{SYNC}$	t_{DRxC}		100	ns

TIMING WAVEFORMS

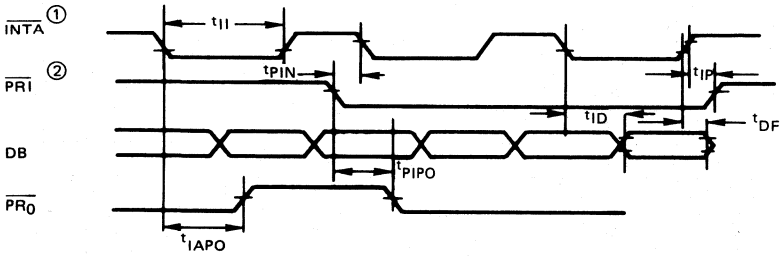
READ CYCLE



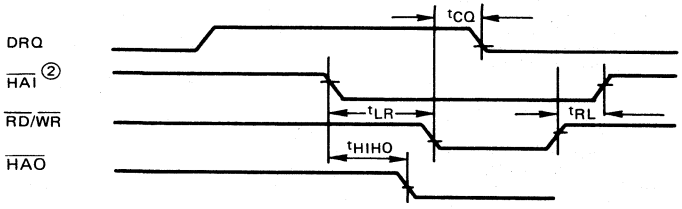
WRITE CYCLE



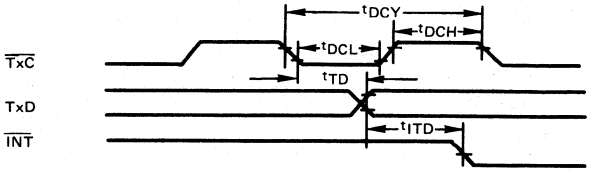
INTA CYCLE



DMA CYCLE



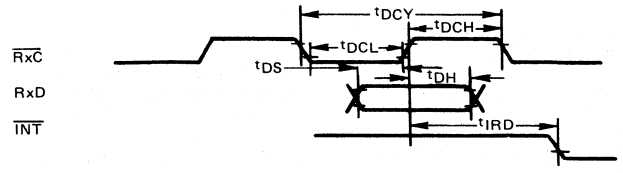
TRANSMIT DATA CYCLE



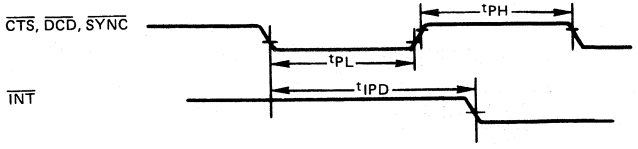
Notes: ① INTA signal acts as RD signal.
② PRI and HAI signals act as CS signal.

TIMING WAVEFORMS
(CONT.)

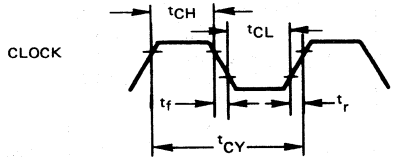
RECEIVE DATA CYCLE



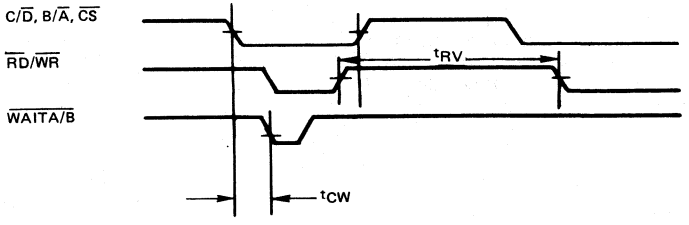
OTHER TIMING



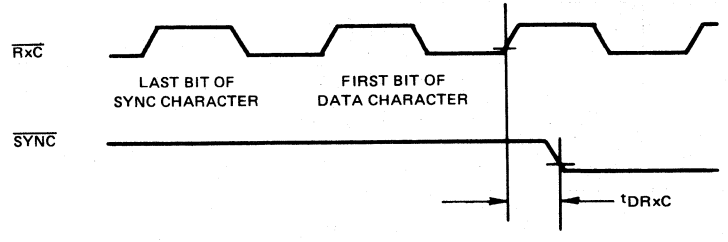
CLOCK



READ/WRITE CYCLE
(SOFTWARE BLOCK TRANSFER MODE)



SYNC PULSE GENERATION
(EXTERNAL SYNC MODE)



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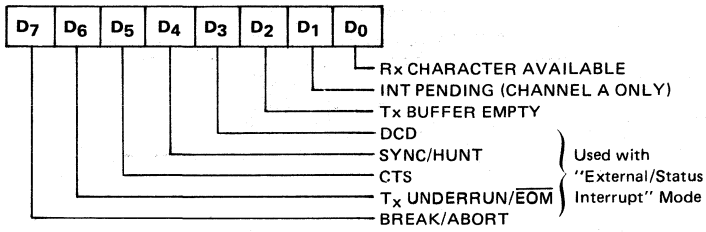
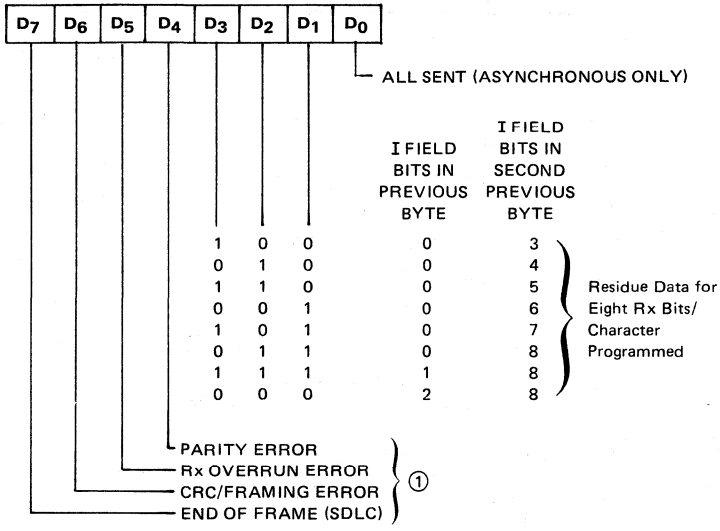
READ REGISTER
BIT FUNCTIONS

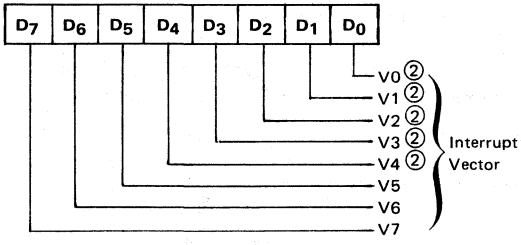
READ REGISTER 0



READ REGISTER 1 ①



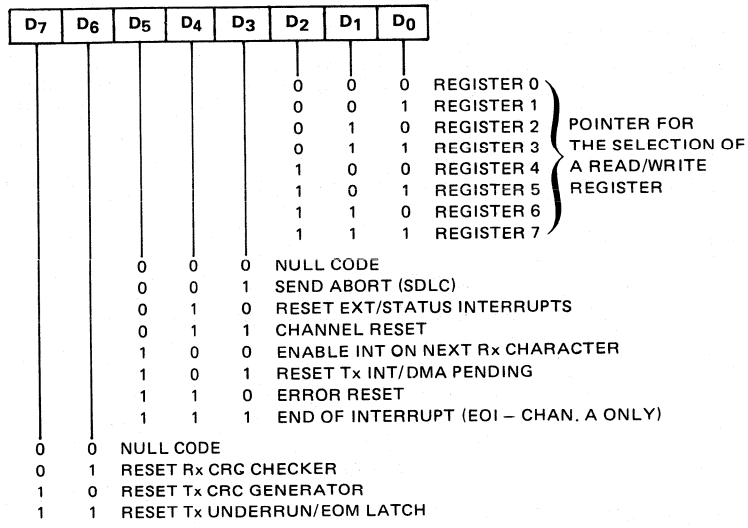
READ REGISTER 2



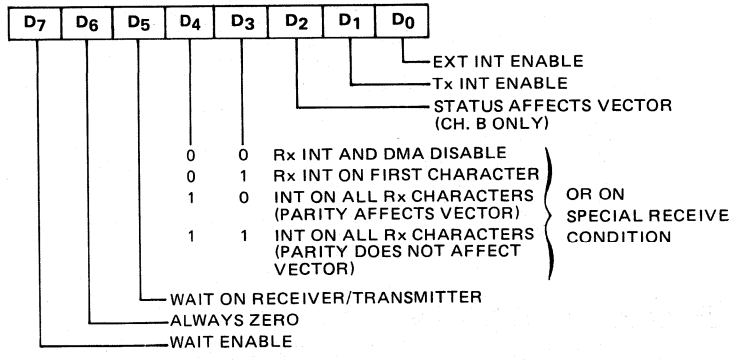
Notes: ① Used with Special Receive Condition Mode.
② Variable if "Status Affects Vector" is programmed.

WRITE REGISTER BIT FUNCTIONS

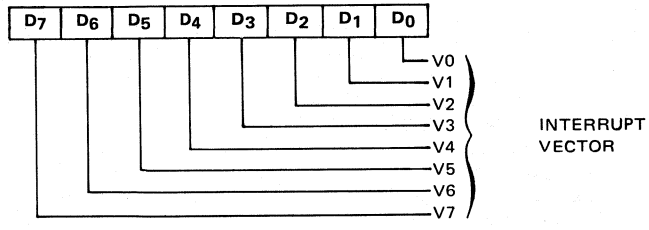
WRITE REGISTER 0



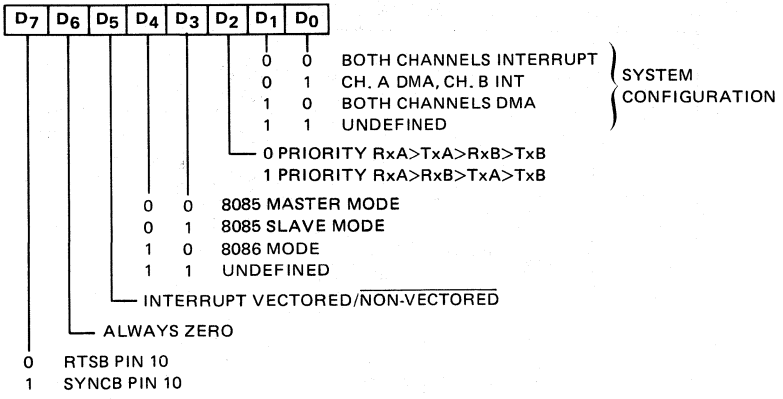
WRITE REGISTER 1



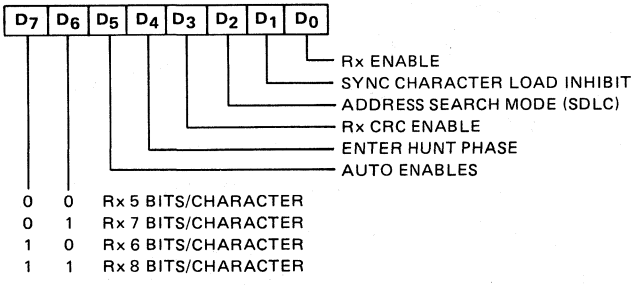
WRITE REGISTER 2 (CHANNEL B)



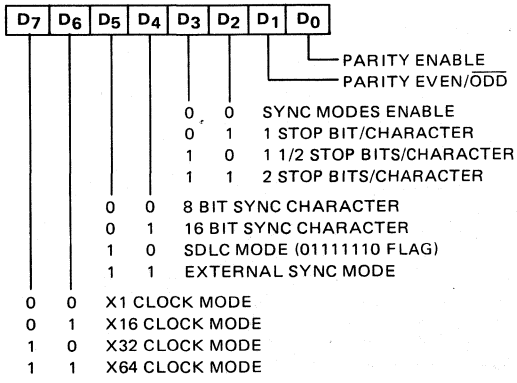
WRITE REGISTER 2 (CHANNEL A)



WRITE REGISTER 3

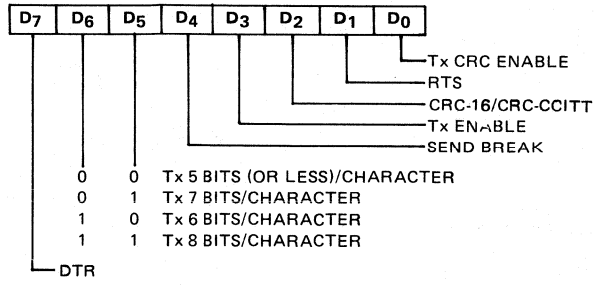


WRITE REGISTER 4

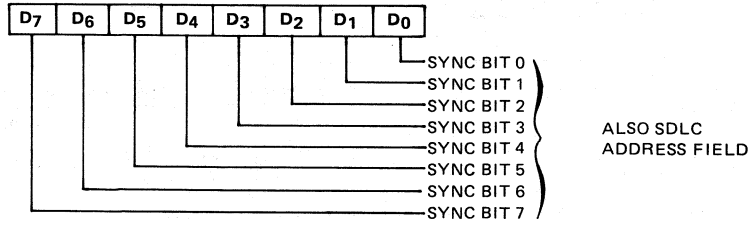


WRITE REGISTER BIT FUNCTIONS (CONT.)

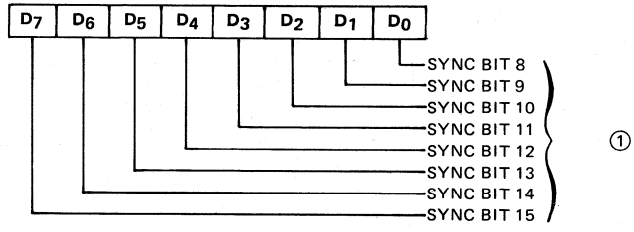
WRITE REGISTER 5



WRITE REGISTER 6



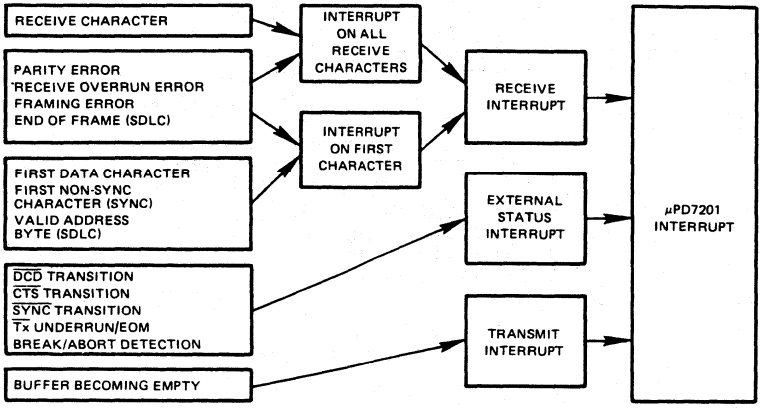
WRITE REGISTER 7



Note: ① For SDLC it must be programmed to "01111110" for flag recognition.

9

INTERRUPT STRUCTURE



WR2s BITS IN CH. A			PRIN	MODE	CONTENTS ON DATA BUS DRIVEN BY THE μPD7201 AT EACH INTA SEQUENCE																			
					1st $\overline{INTA}$								2nd $\overline{INTA}$								3rd $\overline{INTA}$ (*)							
D_5	D_4	D_3			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	x	x	x	Non-vectored	High-Z								High-Z								High-Z							
1	0	0	0	8085 Master	(Call) 1	1	0	0	1	1	0	1	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	0	0	0	0	0	0	0	0
1	0	0	1	8085 Master	1	1	0	0	1	1	0	1	High-Z								High-Z							
1	0	1	0	8085 Slave	High-Z								V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0	0	0	0	0	0	0	0	0
1	0	1	1	8085 Slave	High-Z								High-Z								High-Z							
1	1	0	0	8086	High-Z								V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0								
1	1	0	1	8086	High-Z								High-Z															

(*) 3rd $\overline{INTA}$ is 8085 Mode

Condition Affects Vector Modifications

8085 Modes / 8086 Modes	D_4 / D_2	D_3 / D_1	D_2 / D_0	CONDITION
	1	1	1	No Interrupt Pending
	0	0	0	Channel B Transmitter Buffer Empty
	0	0	1	Channel B External/Status Change
	0	1	0	Channel B Received Character Available
	0	1	1	Channel B Special Receive Condition
	1	0	0	Channel A Transmitter Buffer Empty
	1	0	1	Channel A External/Status Change
	1	1	0	Channel A Received Character Available
	1	1	1	Channel A Special Receive Condition

INTELLIGENT GPIB INTERFACE CONTROLLER

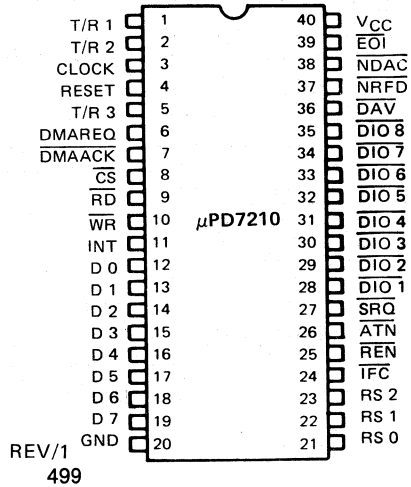
DESCRIPTION

The μPD7210 TLC is an intelligent GPIB Interface Controller designed to meet all of the functional requirements for Talkers, Listeners, and Controllers as specified by the IEEE Standard 488-1978. Connected between a processor bus and the GPIB, the TLC provides high level management of the GPIB to unburden the processor and to simplify both hardware and software design. Fully compatible with most processor architectures, Bus Driver/Receivers are the only additional components required to implement any type of GPIB interface.

FEATURES

- All Functional Interface Capability Meeting IEEE Standard 488-1978
  - SH1 (Source Handshake)
  - AH1 (Acceptor Handshake)
  - T5 or TE5 (Talker or Extended Talker)
  - L3 or LE3 (Listener or Extended Listener)
  - SR1 (Service Request)
  - RL1 (Remote Local)
  - PP1 or PP2 ((Parallel Poll) (Remote or Local Configuration))
  - DC1 (Device Clear)
  - DT1 (Device Trigger)
  - C1-5 ((Controller) (All Functions))
- Programmable Data Transfer Rate
- 16 MPU Accessible Registers – 8 Read/8 Write
- 2 Address Registers
  - Detection of MTA, MLA, MSA (My Talk/Listen/Secondary Address)
  - 2 Device Addresses
- EOS Message Automatic Detection
- Command (IEEE Standard 488-78) Automatic Processing and Undefined Command Read Capability
- DMA Capability
- Programmable Bus Transceiver I/O Specification (Works with T.I./Motorola/Intel)
- 1 to 8 MHz Clock Range
- TTL Compatible
- N Channel MOS
- +5V Single Power Supply
- 40-Pin Plastic DIP
- 8080/85/86 Compatible

PIN CONFIGURATION

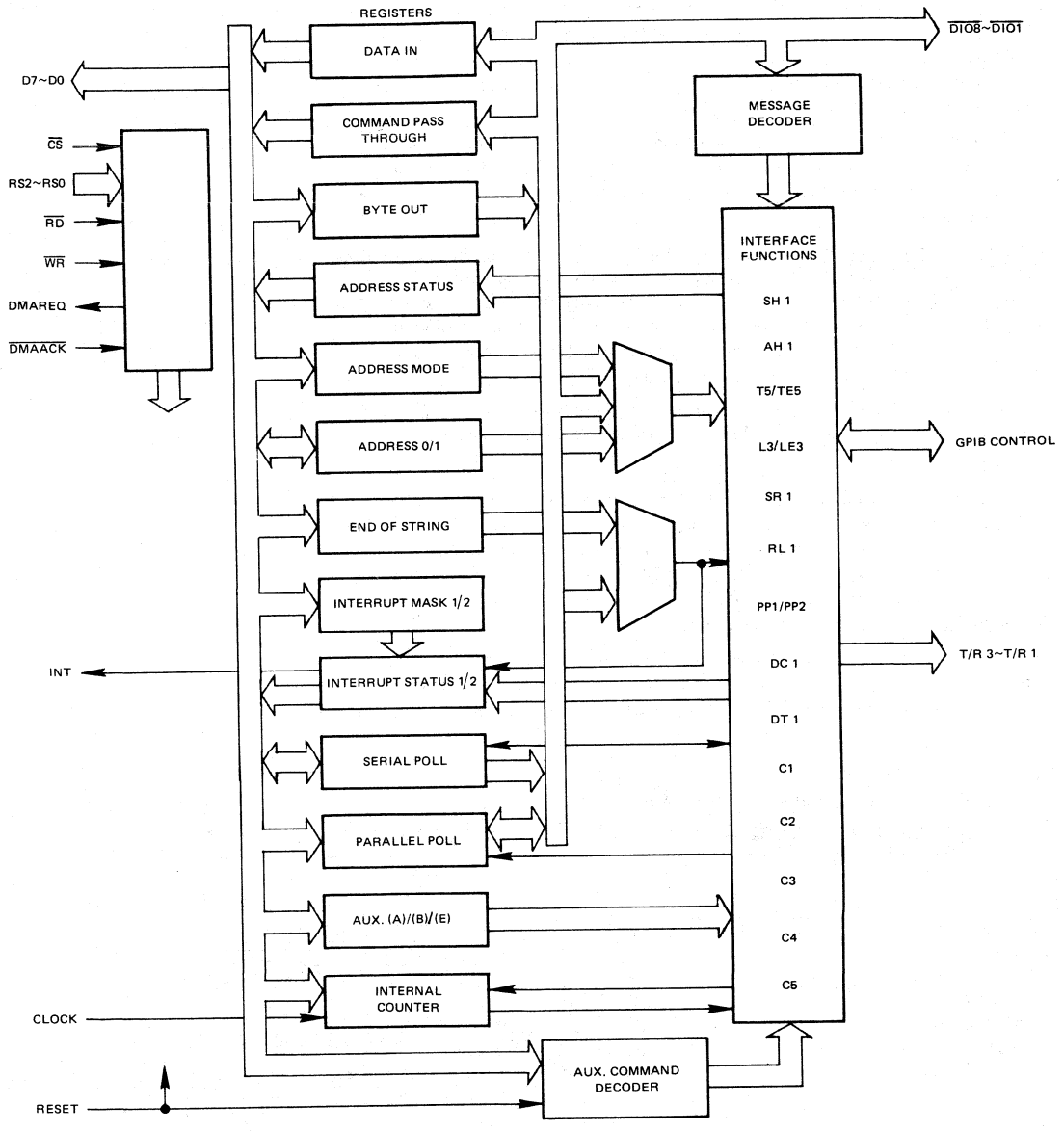


9

PIN IDENTIFICATION

PIN	NAME	I/O	DESCRIPTION
1	T/R1	O	Transmit/Receive Control – Input/Output Control Signal for the GPIB Bus Transceivers.
2	T/R2	O	Transmit/Receive Control – The functions of T/R2, T/R3 are determined by the values of TRM1, TRM0 of the address mode register.
3	CLK	I	Clock – (1-8 MHz) Reference Clock for generating the state change prohibit times T1, T6, T7, T9 specified in IEEE Standard 488-1978.
4	RST	I	Reset – Resets 7210 to an idle state when high (active high).
5	T/R3	O	Transmit/Receive Control – Function determined by TRM1 and TRM0 of address mode register (See T/R2).
6	DRQ	O	DMA Request – 7210 requests data transfer to the computer system, becomes low on input of DMA acknowledge signal $\overline{DACK}$.
7	$\overline{DACK}$	I	DMA Acknowledge – (Active Low) Signal connects the computer system data bus to the data register of the 7210.
8	$\overline{CS}$	I	Chip Select – (Active Low) Enables access to the register selected by RS0-2 (read or write operation).
9	$\overline{RD}$	I	Read – (Active Low) Places contents of read register specified by RS0-2 – on D0-7 (Computer Bus).
10	$\overline{WR}$	I	Write – (Active Low) writes data on D0-7 into the write register specified by RS0-2.
11	INT / $\overline{INT}$	O	Interrupt Request – (Active High/Low) Becomes active due to any 1 of 13 internal interrupt factors (unmasked) active state software configurable, active high on chip reset.
12-19	D0-7	I/O	Data Bus – 8-bit bidirectional data bus, for interface to computer system.
20	GND		Ground.
21-23	RS0-2	I	Register Select – These lines select one of eight read (write) registers during a read (write) operation.
24	$\overline{IFC}$	I/O	Interface Clear – Control line used for clearing the interface functions.
25	$\overline{REN}$	I/O	Remote Enable – Control line used to select remote or local control of the devices.
26	$\overline{ATN}$	I/O	Attention – Control line which indicates whether data on DIO lines is an interface message or device dependent message.
27	$\overline{SRQ}$	I/O	Service Request – Control line used to request the controller for service.
28-35	$\overline{DIO1\text{-}8}$	I/O	Data Input/Output – 8-bit bidirectional bus for transfer of message on the GPIB.
36	$\overline{DAV}$	I/O	Data Valid – Handshake line indicating that data on DIO lines is valid.
37	$\overline{NRFD}$	I/O	Ready for Data – Handshake line indicating that device is ready for data.
38	$\overline{NDAC}$	I/O	Data Accepted – Handshake line indicating completion of message reception.
39	$\overline{EOI}$	I/O	End or Identify – Control line used to indicate the end of multiple byte transfer sequence or to execute a parallel polling in conjunction with ATN.
40	V_{CC}		+5V DC – Technical Specifications: +5V; NMOS; 500 MW; 40 Pins; TTL Compatible; 1-8 MHz.

BLOCK DIAGRAM



INTRODUCTION

The IEEE Standard 488 describes a "Standard Digital Interface for Programmable Instrumentation" which, since its introduction in 1975, has become the most popular means of interconnecting instruments and controllers in laboratory, automatic test and even industrial applications. Refined over several years, the 488-1978 Standard, also known as the General Purpose Interface Bus (GPIB), is a highly sophisticated standard providing a high degree of flexibility to meet virtually most all instrumentation requirements. The μPD7210 TLC implements all of the functions that are required to interface to the GPIB. While it is beyond the scope of this document to provide a complete explanation of the IEEE 488 Standard, a basic description follows:

The GPIB interconnects up to 15 devices over a common set of data control lines. Three types of devices are defined by the standard: Talkers, Listeners, and Controllers, although some devices may combine functions such as Talker/Listener or Talker/Controller.

Data on the GPIB is transferred in a bit parallel, byte serial fashion over 8 Data I/O lines (D101 – D108). A 3 wire handshake is used to ensure synchronization of transmission and reception. In order to permit more than one device to receive data at the same time, these control lines are "Open Collector" so that the slowest device controls the data rate. A number of other control lines perform a variety of functions such as device addressing, interrupt generation, etc.

The μPD7210 TLC implements all functional aspects of Talker, Listener and Controller functions as defined by the 488-1978 Standard, and on a single chip.

GENERAL

The μPD7210 TLC is an intelligent controller designed to provide high level protocol management of the GPIB, freeing the host processor for other tasks. Control of the TLC is accomplished via 16 internal registers. Data may be transferred either under program control or via DMA using the TLC's DMA control facilities to further reduce processor overhead. The processor interface of the TLC is general in nature and may be readily interfaced to most processor lines.

In addition to providing all control and data lines necessary for a complete GPIB implementation, the TLC also provides a unique set of bus transceiver controls permitting the use of a variety of different transceiver configurations for maximum flexibility.

INTERNAL REGISTERS

The TLC has 16 registers, 8 of which are read and 8 write.

REGISTER NAME	ADDRESSING						SPECIFICATION							
	R S 2	R S 1	R S 0	$\overline{W}$ R	$\overline{R}$ D	$\overline{C}$ S								
Data In [0R]	0	0	0	1	0	0	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Interrupt Status 1 [1R]	0	0	1	1	0	0	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Status 2 [2R]	0	1	0	1	0	0	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC
Serial Poll Status [3R]	0	1	1	1	0	0	S8	PEND	S6	S5	S4	S3	S2	S1
Address Status [4R]	1	0	0	1	0	0	CIC	ATN	SPMS	LPAS	TPAS	LA	TA	MJMN
Command Pass Through [5R]	1	0	1	1	0	0	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0
Address 0 [6R]	1	1	0	1	0	0	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
Address 1 [7R]	1	1	1	1	0	0	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
Byte Out [0W]	0	0	0	0	1	0	BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0
Interrupt Mask 1 [1W]	0	0	1	0	1	0	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Mask 2 [2W]	0	1	0	0	1	0	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC
Serial Poll Mode [3W]	0	1	1	0	1	0	S8	rsv	S6	S5	S4	S3	S2	S1
Address Mode [4W]	1	0	0	0	1	0	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0
Auxiliary Mode [5W]	1	0	1	0	1	0	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0
Address 0/1 [6W]	1	1	0	0	1	0	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
End of String [7W]	1	1	1	0	1	0	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

DATA REGISTERS

The data registers are used for data and command transfers between the GPIB and the microcomputer system.

DATA IN (0R)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Holds data sent from the GPIB to the computer

BYTE OUT (0W)

BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0

Holds information written into it for transfer to the GPIB

INTERRUPT REGISTERS

The interrupt registers are composed of interrupt status bits, interrupt mask bits, and some other noninterrupt related bits.

READ

INTERRUPT STATUS 1 [1R]	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT STATUS 2 [2R]	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC

WRITE

INTERRUPT MASK 1 [1W]	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT MASK 2 [2W]	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC

There are thirteen factors which can generate an interrupt from the μPD7210, each with their own status bit and mask bit.

The interrupt status bits are always set to one if the interrupt condition is met. The interrupt mask bits decide whether the INT bit and the interrupt pin will be active for that condition.

Interrupt Status Bits

INT	OR of All Unmasked Interrupt Status Bits
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger
END	End (END or EOS Message Received)
DEC	Device Clear
ERR	Error
DO	Data Out
DI	Data In
SRQI	Service Request Input
LOKC	Lockout Change
REMC	Remote Change
ADSC	Address Status Change
CO	Command Output

Noninterrupt Related Bits

LOK	Lockout
REM	Remote/Local
DMAO	Enable/Disable DMA Out
DMAI	Enable/Disable DMA In

SERIAL POLL REGISTERS

READ

SERIAL POLL STATUS [3R]	S8	PEND	S6	S5	S4	S3	S2	S1

WRITE

SERIAL POLL MODE [3W]	S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll Mode register holds the STB (status byte: S8, S6-S1) sent over the GPIB and the local message rsv (request service). The Serial Poll Mode register may be read through the Serial Poll Status register. The PEND is set by rsv = 1, and cleared by NPRS • $\overline{rsv}$ = 1 (NPRS = Negative Poll Response State).

ADDRESS MODE/STATUS REGISTERS

ADDRESS STATUS [4R]	CIC	$\overline{ATN}$	SPMS	LPAS	TPAS	LA	TA	MJMN
ADDRESS MODE [4W]	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0

The Address Mode register selects the address mode of the device and also sets the mode for T/R3 and T/R2 the transceiver control lines.

The functions of T/R2, T/R3 terminals (2 and 5) are determined as below by the TRM1, TRM0 values of the address mode register.

T/R2	T/R3	TRM1	TRM0
EOIOE	TRIG	0	0
CIC	TRIG	0	1
CIC	EOIOE	1	0
CIC	PE	1	1

EOIOE = TACS + SPAS + CIC · $\overline{CSBS}$

This denotes the input/output of $\overline{EOI}$ terminal.

When "1": Output
When "0": Input

CIC = $\overline{CIDS + CADS}$

This denotes if the controller inteface function is active or not.

When "1": $\overline{ATN}$ = output, $\overline{SRQ}$ = input
When "0": $\overline{ATN}$ = input, $\overline{SRQ}$ = output

PE = CIC + $\overline{PPAS}$

This indicates the type of bus driver connected to DI08 to DI01 and DAV lines.

When "1": 3 state type
When "0": Open collector type

TRIG: When DTAS state is initiated or when a trigger auxiliary command is issued, a high pulse is generated.

Upon RESET, TRM0 and TRM1 become "0" (TRM0 = TRM1 = 0) and local message port is provided, so that T/R2 and T/R3 both become "LOW."

ADDRESS MODES

ton	lon	ADM1	ADM0	ADDRESS MODE	CONTENTS OF ADDRESS (0) REGISTER	CONTENTS OF ADDRESS (1) REGISTER
1	0	0	0	Talk only mode	Address Identification Not Necessary (No controller on the GPIB)	
0	1	0	0	Listen only mode	Not Used	
0	0	0	1	Address mode 1 (A1)	Major talk address or Major listen address	Minor talk address or Minor listen address
0	0	1	0	Address mode 2 (A2)	Primary address (talk or listen)	Secondary address (talk or listen)
0	0	1	1	Address mode 3 (A3)	Primary address (major talk or major listen)	Primary address (minor talk or minor listen)
Combinations other than above indicated Prohibited.						

Notes: (A1)– Either MTA or MLA reception is indicated by coincidence of either address with the received address. Interface function T or L.

(A2)– Address register 0 = primary, Address register 1 = secondary, interface function TE or LE.

(A3)– CPU must read secondary address via Command Pass Through Register interface function (TE or LE).

ADDRESS STATUS BITS

$\overline{ATN}$	Data Transfer Cycle (device in CSBS)
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
CIC	Controller Active
LA	Listener Addressed
TA	Talker Addressed
MJMN	Sets minor T/L address Reset = Major T/L address
SPMS	Serial Poll Mode State

ADDRESS REGISTERS

ADDRESS 0 [6R]	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
ADDRESS 1 [7R]	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
ADDRESS 0/1 [6W]	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

The TLC is able to automatically detect two types of addresses which are held in address registers 0 and 1. The addressing modes are outlined below.

Address settings are made by writing into the address 0/1 register. The function of each bit is described below.

9

ADDRESS 0/1 REGISTER BIT SELECTIONS

ARS – Selects which address register 0 or 1
DT – Permits or Prohibits address to be detected as Talk
DL – Permits or Prohibits address to be detected as Listen
AD5 – AD1 – Device address value
EOI – Holds the value of EOI line when data is received

COMMAND PASS THROUGH REGISTER

COMMAND PASS THROUGH [5R]	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

The CPT register is used such that the CPU may read the DIO lines in the cases of undefined command, secondary address, or parallel poll response.

END OF STRING REGISTER

END OF STRING [7W]

EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

This register holds either a 7- or 8-bit EOS message byte used in the GPIB system to detect the end of a data block. Aux Mode Register A controls the specific use of this register.

AUXILIARY MODE REGISTER

AUXILIARY MODE [5W]

CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

This is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits.

CNT 2	1	0	COM 4	3	2	1	0	OPERATION
0	0	0	C_4	C_3	C_2	C_1	C_0	Issues an auxiliary command specified by C_4 to C_0.
0	0	1	0	F_3	F_2	F_1	F_0	The reference clock frequency is specified and T_1, T_6, T_7, T_9 are determined as a result.
0	1	1	U	S	P_3	P_2	P_1	Makes write operation to the parallel poll register.
1	0	0	A_4	A_3	A_2	A_1	A_0	Makes write operation to the aux. (A) register.
1	0	1	B_4	B_3	B_2	B_1	B_0	Makes write operation to the aux. (B) register.
1	1	0	0	0	0	E_1	E_0	Makes write operation to the aux. (E) register.

AUXILIARY COMMANDS 0 0 0 C_4 C_3 C_2 C_1 C_0

COM 43210			
00000	iepon	—	Immediate Execute pon — Generate local pon Message
00010	crst	—	Chip Reset — Same as External Reset
00011	rrfd	—	Release RFD
00100	trig	—	Trigger
00101	rtl	—	Return to Local Message Generation
00110	seoi	—	Send EOI Message
00111	nvld	—	Non Valid (OSA reception) — Release DAC Holdoff
01111	vld	—	Valid (MSA reception, CPT, DEC, DET) — Release DAC Holdoff
0X001	sppf	—	Set/Reset Parallel Poll Flag
10000	gts	—	Go To Standby
10001	tca	—	Take Control Asynchronously
10010	tcs	—	Take Control Synchronously
11010	tcse	—	Take Control Synchronously on End
10011	ltn	—	Listen
11011	ltnc	—	Listen with Continuous Mode
11100	lun	—	Local Unlisten
11101	epp	—	Execute Parallel Poll
1X110	sifc	—	Set/Reset IFC
1X111	sren	—	Set/Reset REN
10100	dsc	—	Disable System Control

INTERNAL COUNTER 0 0 1 0 F_3 F_2 F_1 F_0

The internal counter generates the state change prohibit times (T_1, T_6, T_7, T_9) specified in the IEEE std 488-1978 with reference to the clock frequency.

AUXILIARY A REGISTER 1 0 0 A_4 A_3 A_2 A_1 A_0

Of the 5 bits that may be specified as part of its access word, 2 bits control the GPIB data receiving modes of the 7210 and 3 bits control how the EOS message is used.

A_1	A_0	DATA RECEIVING MODE
0	0	Normal Handshake Mode
0	1	RFD Holdoff on all Data Modes
1	0	RFD Holdoff on End Mode
1	1	Continuous Mode

BIT NAME			FUNCTION
A_2	0	Prohibit	Permits (prohibits) the setting of the END bit by reception of the EOS message.
	1	Permit	
A_3	0	Prohibit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message TACS.
	1	Permit	
A_4	0	7 bit EOS	Makes the 8 bits/7 bits of EOS register the valid EOS message.
	1	8 bit EOS	

AUXILIARY B REGISTER 1 0 1 B_4 B_3 B_2 B_1 B_0

The Auxiliary B Register is much like the A Register in that it controls the special operating features of the device.

BIT NAME			FUNCTION
B_0	1	Permit	Permits (prohibits) the detection of undefined command. In other words, it permits (prohibits) the setting of the CPT bit on reception of an undefined command.
	0	Prohibit	
B_1	1	Permit	Permits (prohibits) the transmission of the END message when in serial poll active state (SPAS).
	0	Prohibit	
B_2	1	T_1 (high-speed)	T_1 (high speed) as T_1 of handshake after transmission of 2nd byte following data transmission.
	0	T_1 (low-speed)	
B_3	1	$\overline{INT}$	Specifies the active level of $\overline{INT}$ pin.
	0	INT	
B_4	1	ist = SRQS	SRQS indicates the value of ist level local message (the value of the parallel poll flag is ignored). SRQS = 1 . . . ist = 1. SRQS = 0 . . . ist = 0.
	0	ist = Parallel Poll Flag	The value of the parallel poll flag is taken as the ist local message.

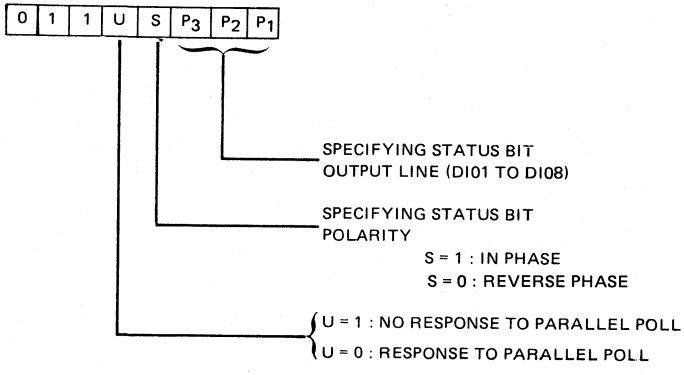
AUXILIARY E REGISTER 1 1 0 0 0 0 E_1 E_0

This register controls the Data Acceptance Modes of the TLC.

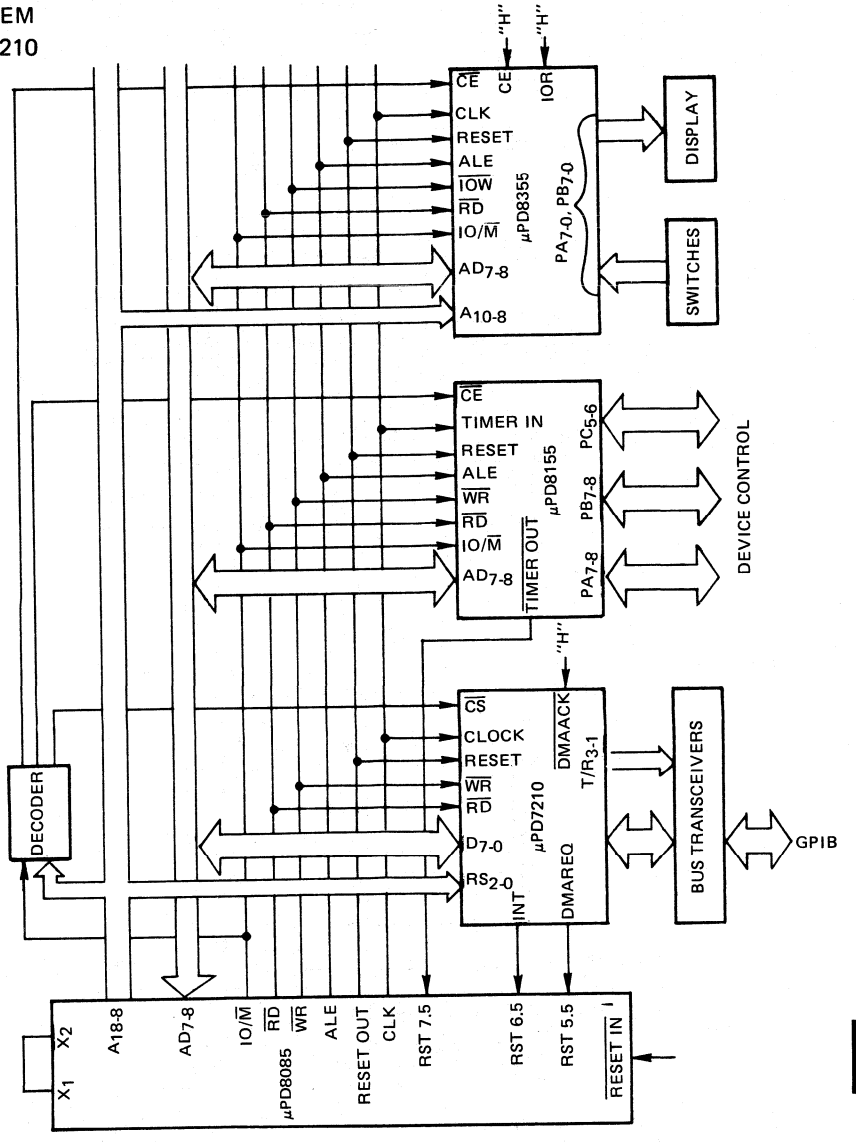
BIT	FUNCTION		
E_0	1	Enable	DAC Holdoff by initiation of DCAS
	0	Disable	
E_1	1	Enable	DAC Holdoff by initiation of DTAS
	0	Disable	

Parallel Poll Register 0 1 1 U S P_3 P_2 P_1

The Parallel Poll Register defines the parallel poll response of the μPD7210.



MINIMUM 8085 SYSTEM
WITH μPD7210



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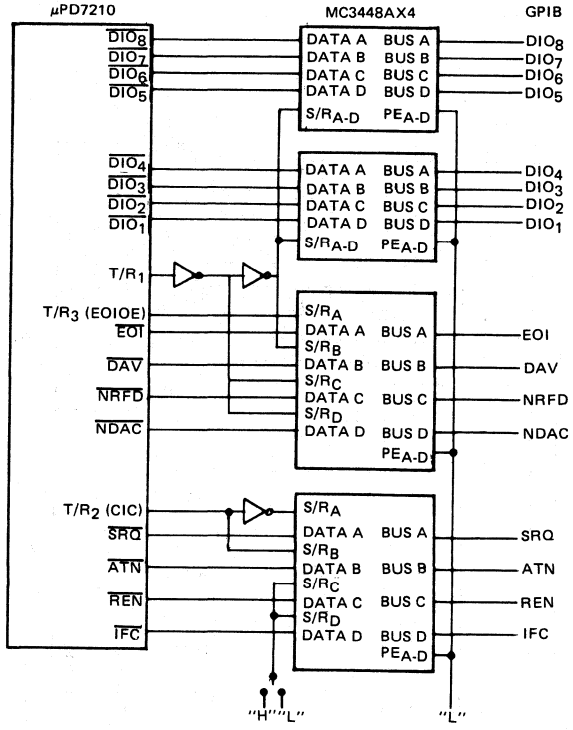
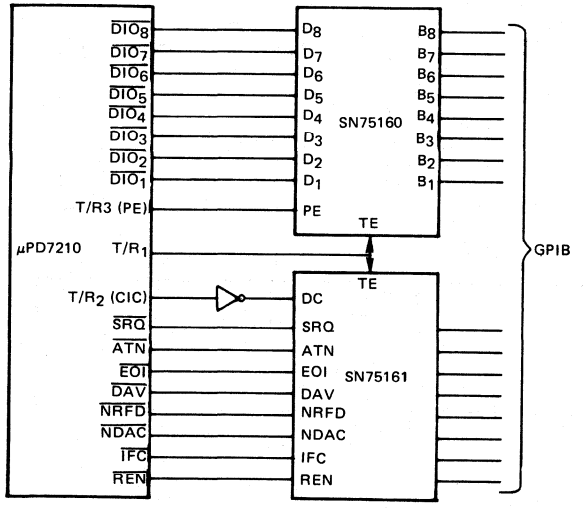
MINIMUM 8085 SYSTEM
WITH μPD7210 (CONT.)



Note: In this example, high-speed data transfer cannot be made since the bus transceiver is of the open collector type (Set $B_2 = 0$).



Note: In the case of low-speed data transfer ($B_2 = 0$), the T/R_3 pin can be used as a TRIG output. The PE input of SN75160 should be cleared to "0." Using this connection, pass-control operation cannot be used.

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

Parameter	Symbol	Test Conditions	Ratings	Unit
Supply Voltage	V_{CC}		−0.5 ~ + 7.0	V
Input Voltage	V_I		−0.5 ~ +7.0	V
Output Voltage	V_O		−0.5 ~ +7.0	V
Operating Temperature	T_{opt}		0 ~ +70	°C
Storage Temperature	T_{stg}		−65 ~ +125	°C

DC CHARACTERISTICS

(T_a = 0 ~ +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
Input Low Voltage	V_{IL}		−0.5		+0.8	V
Input High Voltage	V_{IH}		+2.0		V_{CC} + 0.5	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2 mA (4 mA : T/R1 Pin)			+0.45	V
High Level Output Voltage	V_{OH1}	I_{OH} = −400 μA (Except INT)	+2.4			V
High Level Output Voltage (INT Pin)	V_{OH2}	I_{OH} = −400 μA I_{OH} = −50 μA	+2.4 +3.5			V
Input Leakage Current	I_{IL}	V_{IN} = 0V ~ V_{CC}	−10		+10	μA
Output Leakage Current	I_{OL}	V_{OUT} = 0.45V ~ V_{CC}	−10		+10	μA
Supply Current	I_{CC}				+180	mA

CAPACITANCE

(T_a = 25°C, V_{CC} = GND = 0V)

Parameter	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
Input Capacitance	C_{IN}	f = 1 MHz			10	pF
Output Capacitance	C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground			15	pF
I/O Capacitance	$C_{I/O}$				20	pF

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AC CHARACTERISTICS

(T_a = 0 ~ 70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Conditions	Limits		Unit
			Min.	Max	
$\overline{EOI}\downarrow \rightarrow \overline{DIO}$	t_{EODI}	PPSS → PPAS, ATN = True		250	ns
$\overline{EOI}\downarrow \rightarrow$ T/R1↑	t_{EOT11}	PPSS → PPAS, ATN = True		155	ns
$\overline{EOI}\uparrow \rightarrow$ T/R1↓	t_{EOT12}	PPAS → PPSS, ATN = False		200	ns
$\overline{ATN}\downarrow \rightarrow \overline{NDAC}\downarrow$	t_{ATND}	AIDS → ANRS, LIDS		155	ns
$\overline{ATN}\downarrow \rightarrow$ T/R1↓	t_{ATT1}	TACS + SPAS → TADS, CIDS		155	ns
$\overline{ATN}\downarrow \rightarrow$ T/R2↓	t_{ATT2}	TACS + SPAS → TADS, CIDS		200	ns
$\overline{DAV}\downarrow \rightarrow$ DMAREQ	t_{DVRQ}	ACRS → ACDS, LACS		600	ns
$\overline{DAV}\downarrow \rightarrow \overline{NRFD}\downarrow$	t_{DVNR1}	ACRS → ACDS		350	ns
$\overline{DAV}\downarrow \rightarrow \overline{NDAC}\uparrow$	t_{DVND1}	ACRS → ACDS → AWNS		650	ns
$\overline{DAV}\uparrow \rightarrow \overline{NDAC}\downarrow$	t_{DVND2}	AWNS → ANRS		350	ns
$\overline{DAV}\uparrow \rightarrow \overline{NRFD}\uparrow$	t_{DVNR2}	AWNS → ANRS → ACRS		350	ns
$\overline{RD}\downarrow \rightarrow \overline{NRFD}\uparrow$	t_{RNR}	ANRS → ACRS LACS, DI reg. selected		500	ns
$\overline{NDAC}\uparrow \rightarrow$ DMAREQ↑	t_{NDRQ}	STRS → SWNS → SGNS, TACS		400	ns
$\overline{NDAC}\uparrow \rightarrow \overline{DAV}\uparrow$	t_{NDDV}	STRS → SWNS → SGNS		350	ns
$\overline{WR}\uparrow \rightarrow \overline{DIO}$	t_{WDI}	SGNS → SDYS, BO reg. selected		250	ns
$\overline{NRFD}\uparrow \rightarrow \overline{DAV}\downarrow$	t_{NRDV}	SDYS → STRS, T_1 = True		350	ns
$\overline{WR}\uparrow \rightarrow \overline{DAV}\downarrow$	t_{WDV}	SGNS → SDYS → STRS BO reg. selected, RFD = True N_F = fc = 8 MHz, T_1 (High Speed)		830 +t_{SYNC}	ns
TRIG Pulse Width	t_{TRIG}		50		ns

AC CHARACTERISTICS (CONT.)

(T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Limits Min	Limits Max	Unit
Address Setup to $\overline{RD}$	t_{AR}	RS0 ~ RS2	85		ns
		$\overline{CS}$	0		ns
Address Hold from $\overline{RD}$	t_{RA}		0		ns
$\overline{RD}$ Pulse Width	t_{RR}		170		ns
Data Delay from Address	t_{AD}			250	ns
Data Delay from $\overline{RD}$↓	t_{RD}			150	ns
Output Float Delay from $\overline{RD}$↑	t_{DF}		0	80	ns
$\overline{RD}$ Recovery Time	t_{RV}		250		ns

Address Setup to $\overline{WR}$	t_{AW}		0		ns
Address Hold from $\overline{WR}$	t_{WA}		0		ns
$\overline{WR}$ Pulse Width	t_{WW}		170		ns
Data Setup to $\overline{WR}$	t_{DW}		150		ns
Data Hold from $\overline{WR}$	t_{WD}		0		ns
$\overline{WR}$ Recovery Time	t_{RV}		250		ns

DMAREQ↓ Delay from $\overline{DMAACK}$	t_{AKRQ}			130	ns
Data Delay from $\overline{DMAACK}$	t_{AKD}			200	ns

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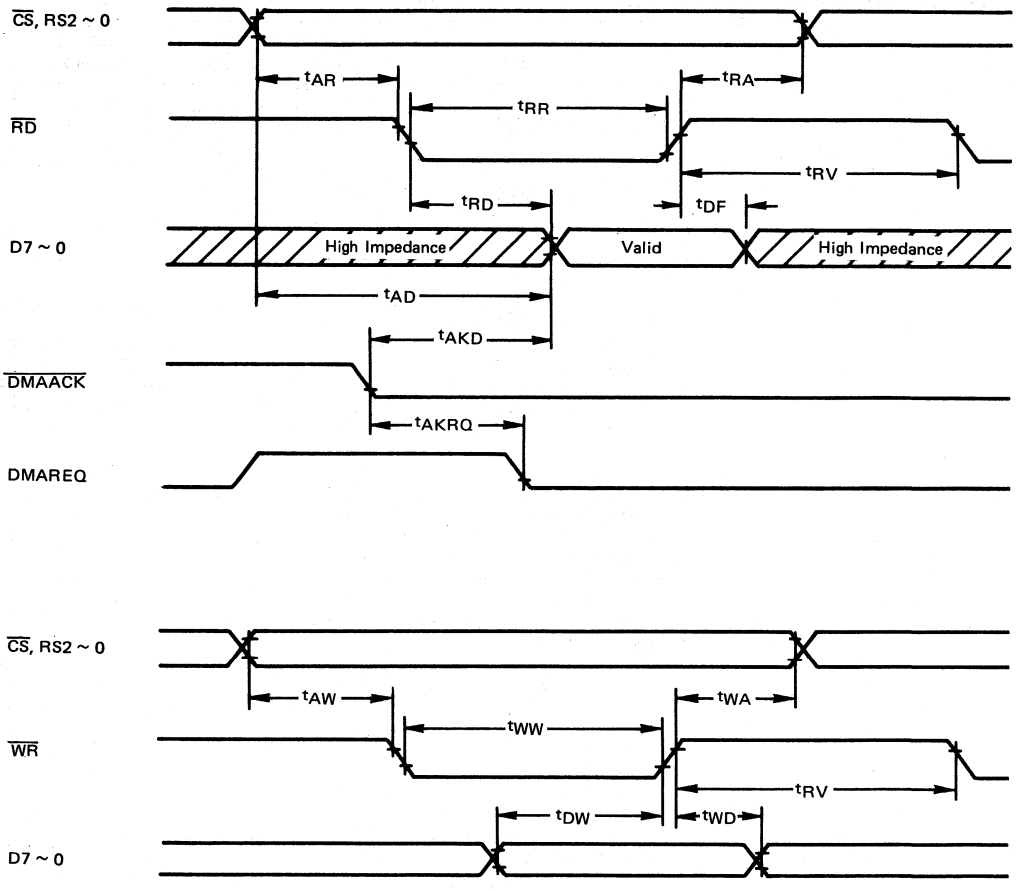
TIMING WAVEFORMS



PRELIMINARY

μPD7220/GDC
GRAPHICS DISPLAY CONTROLLER

Description

The μPD7220 Graphics Display Controller (GDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the GDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the GDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the GDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the GDC is ideal for advanced computer graphics applications.

Features

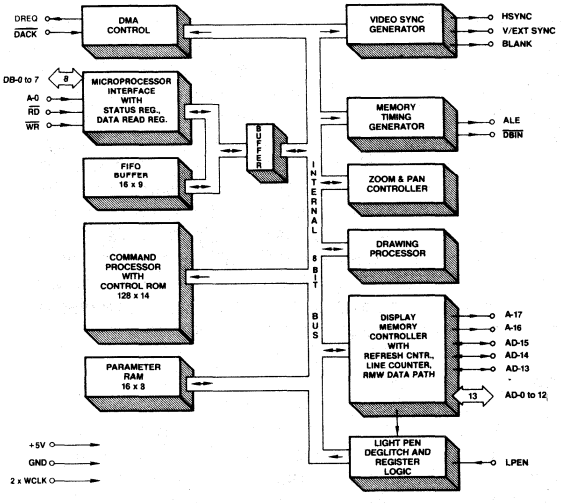
- ☐ Microprocessor Interface
  - DMA transfers with 8257- or 8237-type controllers
  - FIFO Command Buffering
- ☐ Display Memory Interface
  - Up to 256K words of 16 bits
  - Read-Modify-Write (RMW) Display Memory cycles in under 800ns
  - Dynamic RAM reresh cycles for nonaccessed memory
- ☐ Light Pen Input
- ☐ External video synchronization mode
- ☐ Graphics Mode:
  - Four megabit, bit-mapped display memory
- ☐ Character Mode:
  - 8K character code and attributes display memory
- ☐ Mixed Graphics and Characters Mode
  - 64K if all characters
  - 1 megapixel if all graphics
- ☐ Graphics Capabilities:
  - Figure drawing of lines, arc/circles, rectangles, and graphics character in 800ns per pixel
  - Display 1024-by-1024 pixels with 4 planes of color or grayscale.
  - Two independently scrollable areas
- ☐ Character Capabilities:
  - Auto cursor advance
  - Four independently scrollable areas
  - Programmable cursor height
  - Characters per row: up to 256
  - Character rows per screen: up to 100
- ☐ Video Display Format
  - Zoom magnification factors of 1 to 16
  - Panning
  - Command-settable video raster parameters
- ☐ Technology
  - Single +5 volt, NMOS, 40-pin DIP
- ☐ DMA Capability:
  - Bytes or word transfers
  - 4 clock periods per byte transferred

System Considerations

The GDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the GDC's design, each of the system components is used to the maximum extent through six-level hierarchy of simultaneous tasks. At the lowest level, the GDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the GDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the GDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the GDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

GDC Components

The GDC block diagram illustrates how these tasks are accomplished.



Microprocessor Bus Interface

Control of the GDC by the system microprocessor is achieved through an 8-bit bidirectional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal GDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

Command Processor

The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destina-

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tions within the GDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

DMA Control

The DMA control circuitry in the GDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a μPD8257 or μPD8237 DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

Parameter RAM

The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

Video Sync Generator

Based on the clock input, the sync logic generates the raster timing signals for almost any interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple GDCs.

Memory Timing Generator

The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the GDC's ALE and $\overline{DBIN}$ outputs.

Zoom & Pan Controller

Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independent of the other display areas.

Drawing Processor

The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing processor needs no further assistance to complete the figure drawing.

Display Memory Controller

The display memory controller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMs. The memory controller apportions the video field time between the various types of cycles.

Light Pen Deglitcher

Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address.

Programmer's View of GDC

The GDC occupies two addresses on the system microprocessor bus through which the GDC's status register and FIFO are accessed. Commands and parameters are written into the GDC's FIFO and are differentiated based on address bit A0. The status register or the FIFO can be read as selected by the address line.

A0	READ	WRITE
0	STATUS REGISTER	PARAMETER INTO FIFO
1	FIFO READ	COMMAND INTO FIFO

GDC Microprocessor Bus Interface Registers

Commands to the GDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacts the parameters, loads them into the appropriate registers within the GDC, and initiates the required operations.

The commands available in the GDC can be organized into five categories as described in the following section.

GDC Command Summary

Video Control Commands

1. RESET: Resets the GDC to its idle state.
2. SYNC: Specifies the video display format.
3. VSYNC: Selects master or slave video synchronization mode.
4. CCHAR: Specifies the cursor and character row heights.

Display Control Commands

1. START: Ends Idle mode and unblanks the display.
2. BCTRL: Controls the blanking and unblanking of the display.
3. ZOOM: Specifies zoom factors for the display and graphics characters writing.
4. CURS: Sets the position of the cursor in display memory.
5. PRAM: Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
6. PITCH: Specifies the width of the X dimension of display memory.

Drawing Control Commands

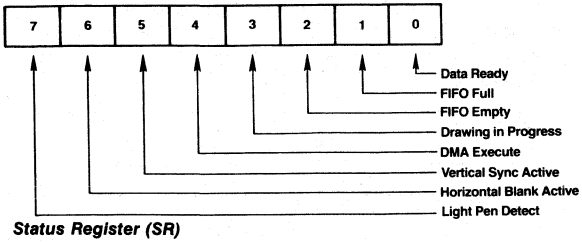
1. WDAT: Writes data words or bytes into display memory.
2. MASK: Sets the mask register contents.
3. FIGS: Specifies the parameters for the drawing processor.
4. FIGD: Draws the figure as specified above.
5. GCHRD: Draws the graphics character into display memory.

Data Read Commands

1. RDAT: Reads data words or bytes from display memory.
2. CURD: Reads the cursor position.
3. LPRD: Reads the light pen address.

DMA Control Commands

1. DMAR: Requests a DMA read transfer.
2. DMAW: Requests a DMA write transfer.



Status Register (SR)

Status Register Flags

SR-7: Light Pen Detect
When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

SR-6: Horizontal Blanking Active
A 1 value for this flag signifies that horizontal retrace blanking is currently underway.

SR-5: Vertical Sync
Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

SR-4: DMA Execute
This bit is a 1 during DMA data transfers.

SR-3: Drawing in Progress
While the GDC is drawing a graphics figure, this status bit is a 1.

SR-2: FIFO Empty
This bit and the FIFO Full flag coordinate system microprocessor accesses with the GDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the GDC have been processed.

SR-1: FIFO Full
A 1 at this flag indicates a full FIFO in the GDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked before each write into the GDC.

SR-0: Data Ready
When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

FIFO Operation & Command Protocol

The first-in, first-out buffer (FIFO) in the GDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the GDC's command set. The microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the GDC requires the differentiation of the first byte of a command sequence from the succeeding bytes. This first byte contains the operation code and the remaining bytes carry parameters. Writing into the GDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the GDC tests this bit as it interprets the entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the GDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the GDC always put the FIFO into write mode if it wasn't in it already. If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require a GDC response, such as RDAT, CURD and LPRD, put the FIFO into read mode after the command is interpreted by the GDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

Read-Modify-Write Cycle

Data transfers between the GDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four clock period timing of the RMW cycle is used to: 1) output the address, 2) read data from the memory, 3) modify the data, and 4) write the modified data back into the initially selected memory address. This type of memory cycle is used for all interactions with display memory including DMA transfers, except for the two clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the GDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic Unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT command or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic Unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic Unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with 1s in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a four-bit dAD field to specify the dot address. The command processor converts this parameter into the one-of-16 format used in the Mask register for figure drawing. A full 16 bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

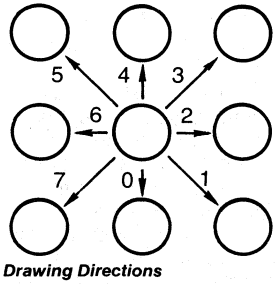
The Logic Unit combines the data read from display memory, the Pattern Register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the modify data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

Figure Drawing

The GDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 5MHz, this is equal to 800ns. During the RMW cycle the GDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the GDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the GDC's internal RMW logic.

During the drawing process, the GDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The GDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counterclockwise.



Drawing Directions

Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer register to the right or left.

The table below summarizes these operations for each direction.

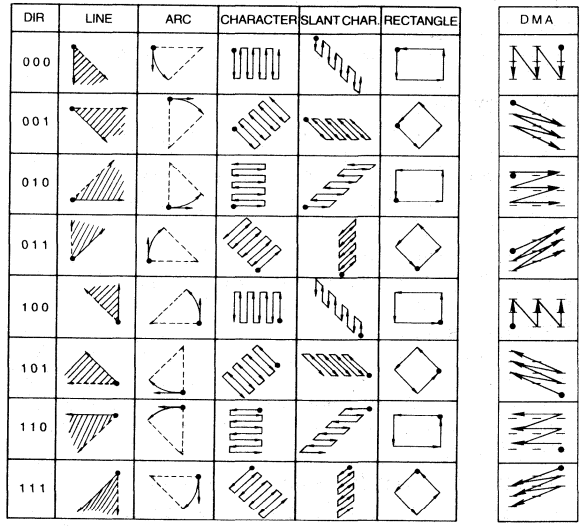
Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the

DIR	OPERATIONS TO ADDRESS THE NEXT PIXEL
000	EAD + P → EAD
001	EAD + P → EAD dAD (MSB) = 1 : EAD + 1 → EAD dAD → LR
010	dAD (MSB) = 1 : EAD + 1 → EAD dAD → LR
011	EAD − P → EAD dAD (MSB) = 1 : EAD + 1 → EAD dAD → LR
100	EAD − P → EAD
101	EAD − P → EAD dAD (LSB) = 1 : EAD − 1 → EAD dAD → RR
110	dAD (LSB) = 1 : EAD + 1 → EAD dAD → RR
111	EAD + P → EAD dAD (LSB) = 1 : EAD + 1 → EAD dAD → RR

Where P = Pitch, LR = Left Rotate, RR = Right Rotate
EAD = Execute Word Address
dAD = Dot Address stored in the Mask Register

dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to effect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:



Note that during line drawing, the angle of the line may be anywhere within the shaded octant defined by the DIR value. Arc drawing starts in the direction initially specified by the DIR value and veers into an arc as drawing proceeds. An arc may be up to 45 degrees in length. DMA transfers are done on word boundaries only, and follow the arrows indicated in the table to find successive word addresses. The slanted paths for DMA transfers indicate the GDC changing both the X and Y components of the word address when moving to the next word. It does not follow a 45 degree diagonal path by pixels.

Drawing Parameters

In preparation for graphics figure drawing, the GDC's Drawing Processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the GDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The GDC Drawing Processor coordinates the RMW circuitry and address registers to draw the specified figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specific details about the figure to be drawn are reduced by the microprocessor to a form conducive to high-speed address calculations within the GDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

DRAWING TYPE	DC	D	D2	D1	DM
Initial Value*	0	8	8	-1	-1
Line	|ΔI|	2|ΔD| - |ΔI|	2(|ΔD| - |ΔI|)	2|ΔD|	—
Arc**	r sin 0↑	r-1	2(r-1)	-1	rsin θ↓
Rectangle	3	A-1	B-1	-1	A-1
Area Fill	B-1	A	A	—	—
Graphic Character***	B-1	A	A	—	—
Read & Write Data	W-1	—	—	—	—
DMAW	D-1	C-1	—	—	—
DMAR	D-1	C-1	(C-1)/2+	—	—

* Initial values for the various parameters are loaded during the handling of the FIGS op code byte.

** Circles are drawn with 8 arcs, each of which span 45°, so that sin 0 = 1/√2 and sin θ = 0.

*** Graphic characters are a special case of bit-map area filling in which B and A ⩽ 8. If A = 8 there is no need to load D and D2.

Where:

-1 = all ONES value.

All numbers are shown in base 10 for convenience. The GDC accepts base 2 numbers (2s complement notation where appropriate).

- — = No parameter bytes sent to GDC for this parameter.
- ΔI = The larger at Δx or Δy.
- ΔD = The smaller at Δx or Δy.
- r = Radius at curvature, in pixels.
- ϕ = Angle from major axis to end at the arc. ϕ ⩽ 45°.
- θ = Angle from major axis to start at the arc. θ ⩽ 45°.
- ↑ = Round up to the next higher integer.
- ↓ = Round down to the next lower integer.
- A = Number of pixels in the initially specified direction.
- B = Number of pixels in the direction at right angles to the initially specified direction.
- W = Number of words to be accessed.
- C = Number of bytes to be transferred in the initially specified direction. (Two bytes per word if word transfer mode is selected).
- D = Number of words to be accessed in the direction at right angles to the initially specified direction.
- DC = Drawing count parameter which is one less than the number of RMW cycles to be executed.
- DM = Dots masked from drawing during arc drawing.
- \+ = Needed only for word reads.

Graphics Character Drawing

Graphics characters can be drawn into display memory pixel-by-pixel. The up to 8-by-8 character is loaded into the GDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

Once the parameter RAM has been loaded with up to eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the zoom command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor.

The movement of these PRAM bytes to the display memory is controlled by the parameters of the FIGS command. Based on the specified height and width of the area to be drawn, the parameter RAM is scanned to fill the required area.

For an 8-by-8 graphics character, the first pixel drawn uses the LSB of RA-15, the second pixel uses bit 1 of RA-15, and so on, until the MSB of RA-15 is reached.

The GDC jumps to the corresponding bit in RA-14 to continue the drawing. The progression then advances toward the LSB of RA-14. This snaking sequence is continued for the other 6 PRAM bytes. This progression matches the sequence of display memory addresses calculated by the drawing processor as shown above. If the area is narrower than 8 pixels wide, the snaking will advance to the next PRAM byte before the MSB is reached. If the area is less than 8 lines high, fewer bytes in the parameter RAM will be scanned. If the area is larger than 8 by 8, the GDC will repeat the contents of the parameter RAM in two dimensions, as required to fill the area with the 8-by-8 mozaic. (Fractions of the 8-by-8 pattern will be used to fill areas which are not multiples of 8 by 8.)

Parameter RAM Contents: RAM Address RA 0 to 15

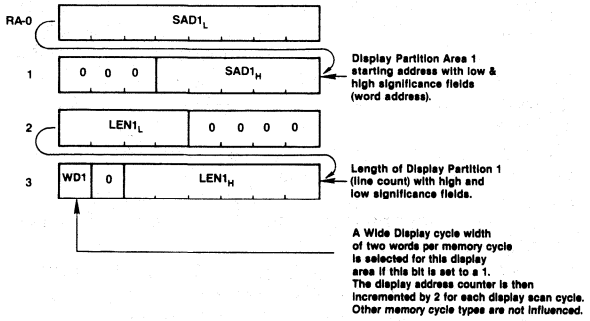
The parameters stored in the parameter RAM, PRAM, are available for the GDC to refer to repeatedly during figure drawing and raster-scanning. In each mode of operation the values in the PRAM are interpreted by the GDC in a predetermined fashion. The host microprocessor must load the appropriate parameters into the proper PRAM locations. PRAM loading command allows the host to write into any location of the PRAM and transfer as many bytes as desired. In this way any stored parameter byte or bytes may be changed without influencing the other bytes.

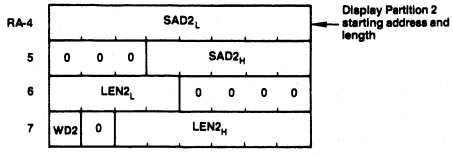
The PRAM stores two types of information. For specifying the details of the display area partitions, blocks of four bytes are used. The four parameters stored in each block include the starting address in display memory of each display area, and its length. In addition, there are two mode bits for each area which specify whether the area is a bit-mapped graphics area or a coded character area, and whether a 16-bit or a 32-bit wide display cycle is to be used for that area.

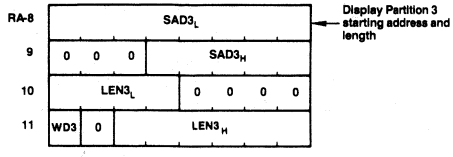
The other use for the PRAM contents is to supply the pattern for figure drawing when in a bit-mapped graphics area or mode. In these situations, PRAM bytes 8 through 16 are reserved for this patterning information. For line, arc, and rectangle drawing (linear figures) locations 8 and 9 are loaded into the Pattern Register to allow the GDC to draw dotted, dashed, etc. lines. For area filling and graphics bit-mapped character drawing locations 8 through 15 are referenced for the pattern or character to be drawn.

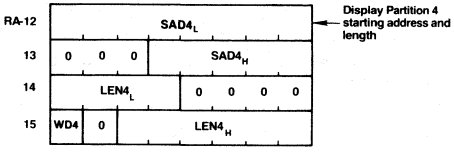
Details of the bit assignments are shown on the following pages for the various modes of operation.

Character Mode

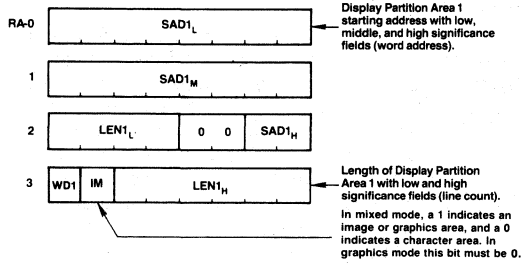


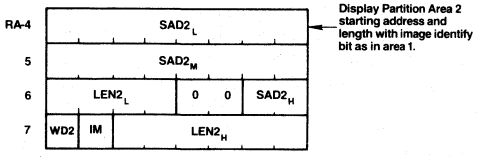


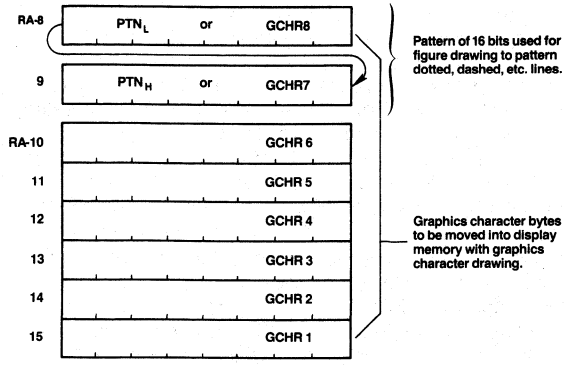




Graphics and Mixed Graphics and Character Modes





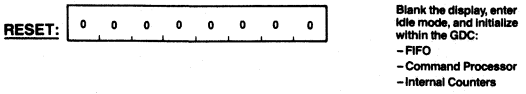


Command Bytes Summary

RESET:	0	0	0	0	0	0	0	0
SYNC:	0	0	0	0	1	1	1	DE
VSYNC:	0	1	1	0	1	1	1	M
CCHAR:	0	1	0	0	1	0	1	1
START:	0	1	1	0	1	0	1	1
BCTRL:	0	0	0	0	1	1	0	DE
ZOOM:	0	1	0	0	0	1	1	0
CURS:	0	1	0	0	1	0	0	1
PRAM:	0	1	1	1	SA			
PITCH:	0	1	0	0	0	1	1	1
WDAT:	0	0	1	TYPE		0	MOD	
MASK:	0	1	0	0	1	0	1	0
FIGS:	0	1	0	0	1	1	0	0
FIGD:	0	1	1	0	1	1	0	0
GCHRD:	0	1	1	0	1	0	0	0
RDAT:	1	0	1	TYPE		0	MOD	
CURD:	1	1	1	0	0	0	0	0
LPRD:	1	1	0	0	0	0	0	0
DMAR:	1	0	1	TYPE		1	MOD	
DMAW:	0	0	1	TYPE		1	MOD	

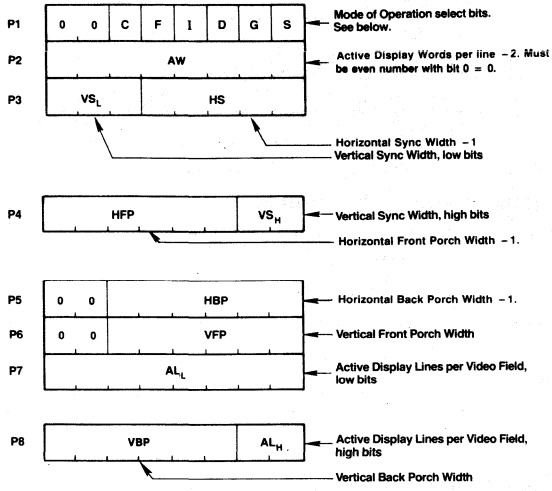
Video Control Commands

Reset



This command can be executed at any time and does not modify any of the parameters already loaded into the GDC.

If followed by parameter bytes, this command also sets the sync generator parameters as described below.
Idle mode is exited with the START command.



In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any.
The number of active words per line must be an even number from 2 to 256.
An all-zero parameter value selects a count equal to 2^n where n = number of bits in the parameter field for vertical parameters.
All horizontal widths are counted in display words.
All vertical intervals are counted in lines.

SYNC Generator Period Constraints

Horizontal Back Porch Constraints

1. In general:
   HBP ≥ 3 Display Word Cycles (6 clock cycles).
2. If the IMAGE or WD modes change within one video field:
   HBP ≥ 5 Display Word Cycles (10 clock cycles).

Horizontal Front Porch Constraints

1. If the display ZOOM function is used at other than 1X:
   HFP ≥ 2 Display Word Cycles (4 clock cycles).
2. If the GDC is used in the video sync Slave mode:
   HFP ≥ 4 Display Word Cycles (8 clock cycles).
3. If the Light Pen is used:
   HFP ≥ 6 Display Word Cycles (12 clock cycles).

Horizontal SYNC Constraints

1. If Interlaced display mode is used:
   HS ≥ 3 Display Word Cycles (6 clock cycles).

Modes of Operation Bits

C	G	Display Mode
0	0	Mixed Graphics & Character
0	1	Graphics Mode
1	0	Character Mode
1	1	Invalid

I	S	Video Framing
0	0	Noninterlaced
0	1	Invalid
1	0	Interlaced Repeat Field for Character Displays
1	1	Interlaced

Repeat Field Framing: 2 Field Sequence with ½ line offset between otherwise identical fields.
Interlaced Framing: 2 Field Sequence with ½ line offset. Each field displays alternate lines.
Noninterlaced Framing: 1 field brings all of the information to the screen.

Total scanned lines in interlace mode is odd. The sum of VFP + VS + VBP + AL should equal one less than the desired odd number of lines.

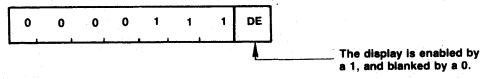
D	Dynamic RAM Refresh Cycles Enable
0	No Refresh — STATIC RAM
1	Refresh — Dynamic RAM

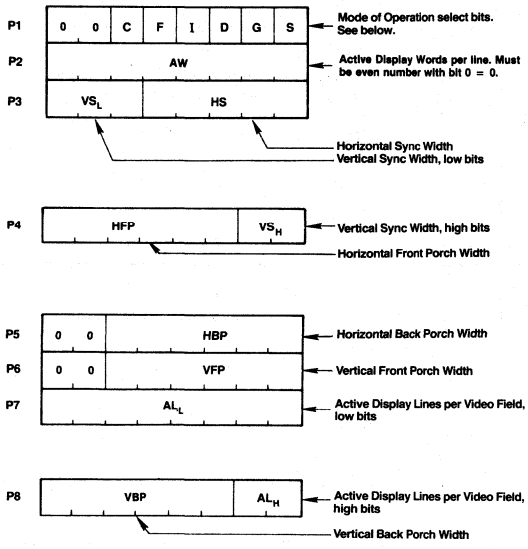
Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

F	Drawing Time Window
0	Drawing during active display time and retrace blanking
1	Drawing only during retrace blanking

Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.

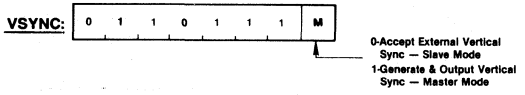
SYNC Format Specify





This command also loads parameters into the sync generator. The various parameter fields and bits are identical to those at the RESET command. The GDC is not reset nor does it enter idle mode.

Vertical Sync Mode



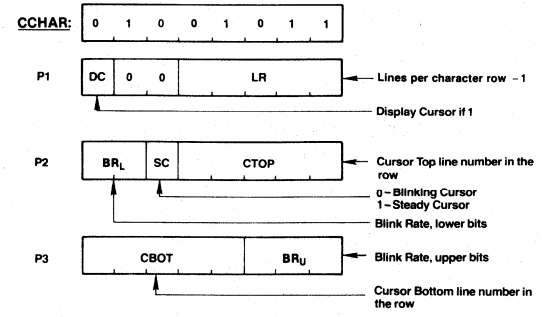
When using two or more GDCs to contribute to one image, one GDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all GDCs are connected together.

Slave Mode Operation

A few considerations should be observed when synchronizing two or more GDCs to generate overlayed video via the VSYNC INPUT/OUTPUT pin. As mentioned above, the Horizontal Front Porch (HFP) must be 4 or more display cycles wide. This is equivalent to eight or more clock cycles. This gives the slave GDCs time to initialize their internal video sync generators to the proper point in the video field to match the incoming vertical sync pulse (VSYNC). This resetting of the generator occurs just after the end of the incoming VSYNC pulse, during the HFP interval. Enough time during HFP is required to allow the slave GDC to complete the operation before the start of the HSYNC interval.

Once the GDCs are initialized and set up as Master and Slaves, they must be given time to synchronize. It is a good idea to watch the VSYNC status bit of the Master GDC and wait until after one or more VSYNC pulses have been generated before the display process is started. The START command will begin the active display of data and will end the video synchronization process, so be sure there has been at least one VSYNC pulse generated for the Slaves to synchronize to.

Cursor & Character Characteristics

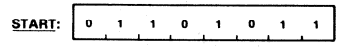


In graphics mode, LR should be set to 0.

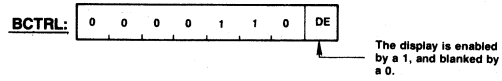
The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always ½ the cursor rate but with a ¾ on-¼ off duty cycle.

Display Control Commands

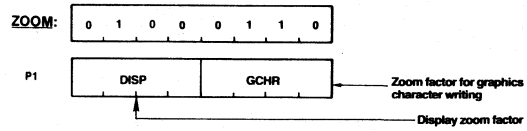
Start Display & End Idle Mode



Display Blanking Control

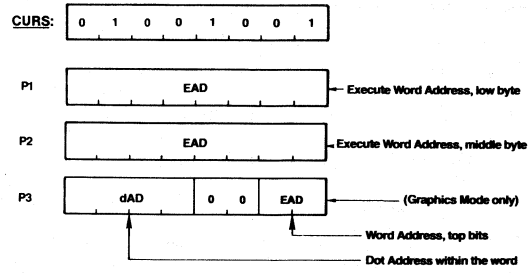


Zoom Factors Specify



Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.

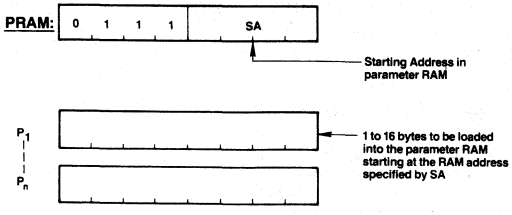
Cursor Position Specify



In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address.

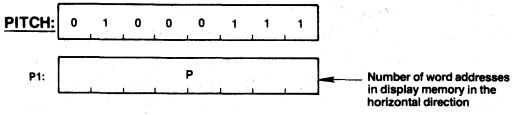
In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.

Parameter RAM Load



From the starting address, SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is terminated by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.

Pitch Specification

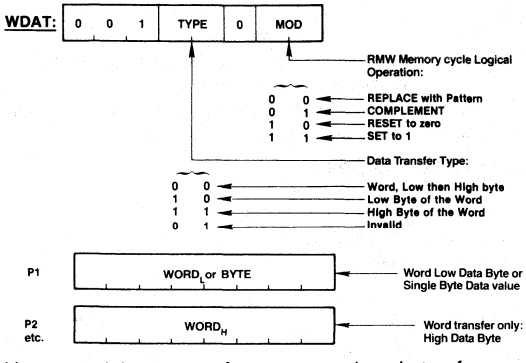


This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

The Pitch parameter (width of display memory) is set by two different commands. In addition to the PITCH command, the RESET (or SYNC) command also sets the pitch value. The "active words per line" parameter, which specifies the width of the raster-scan display, also sets the Pitch of the display memory. In situations in which these two values are equal there is no need to execute a PITCH command.

Drawing Control Commands

Write Data into Display Memory



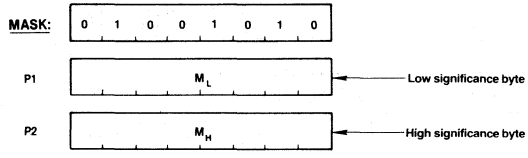
Upon receiving a set of parameters (two bytes for a word transfer, one for a byte transfer), one RMW cycle into Video Memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.

For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

In graphics bit-map situations, only the LSB of the WDAT parameter bytes is used as the pattern in the RMW operations. Therefore it is possible to have only an all ones or all zeros pattern. In coded character applications all the bits of the WDAT parameters are used to establish the drawing pattern.

The WDAT command operates differently from the other commands which initiate RMW cycle activity. It requires parameters to set up the Pattern register while the other commands use the stored values in the parameter RAM. Like all of these commands, the WDAT command must be preceeded by a FIGS command and its parameters. Only the first three parameters need be given following the FIGS opcode, to set up the type of drawing, the DIR direction, and the DC value. The DC parameter + 1 will be the number of RMW cycles done by the GDC with the first set of WDAT parameters. Additional sets of WDAT parameters will see a DC value of 0 which will cause only one RMW cycle to be executed.

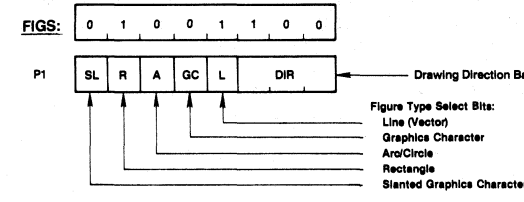
Mask Register Load

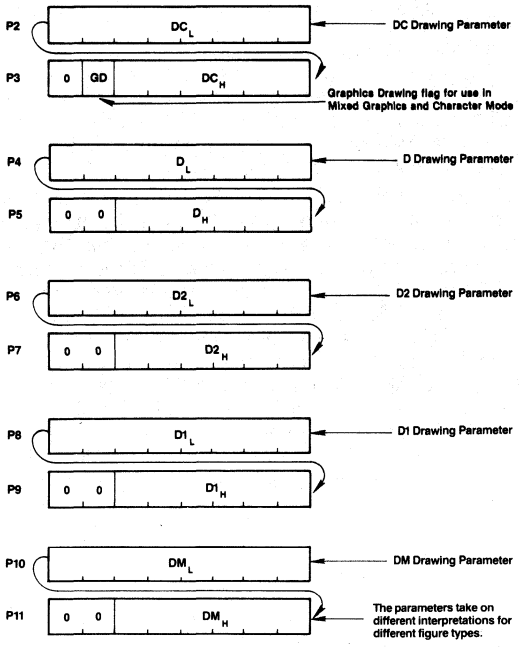


This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

The Mask register is loaded both by the MASK command and the third parameter byte of the CURS command. The MASK command accepts two parameter bytes to load a 16-bit value into the Mask register. All 16 bits can be individually one or zero, under program control. The CURS command on the other hand, puts a "1 of 16" pattern into the Mask register based on the value of the Dot Address value, dAD. If normal single-pixel-at-a-time graphics figure drawing is desired, there is no need to do a MASK command at all since the CURS command will set up the proper pattern to address the proper pixels as drawing progresses. For coded character DMA, and screen setting and clearing opertions using the WDAT command, the MASK command should be used after the CURS command if its third parameter byte has been output.

Figure Drawing Parameters Specify





Valid Figure Type Select Combinations

SL	R	A	GC	L	Operation
0	0	0	0	0	Character Display Mode Drawing, Individual Dot Drawing, DMA, WDAT, and RDAT
0	0	0	0	1	Straight Line Drawing
0	0	0	1	0	Graphics Character Drawing and Area filling with graphics character pattern
0	0	1	0	0	Arc and Circle Drawing
0	1	0	0	0	Rectangle Drawing
1	0	0	1	0	Slanted graphics character drawing and slanted area filling

Only these bit combinations assure correct drawing operation.

Figure Draw Start

FIGD: 0 1 1 0 1 1 0 0

On execution of this instruction, the GDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.

Graphics Character Draw and Area Filling Start

GCHRD: 0 1 1 0 1 0 0 0

Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in Parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

Data Read Commands

Read Data from Display Memory

RDAT: 1 0 1 | TYPE | 0 | MOD

Data Transfer Type:
- 0 0 — Word, low then high byte
- 1 0 — Low Byte of the Word only
- 1 1 — High Byte of the Word only
- 0 1 — Invalid

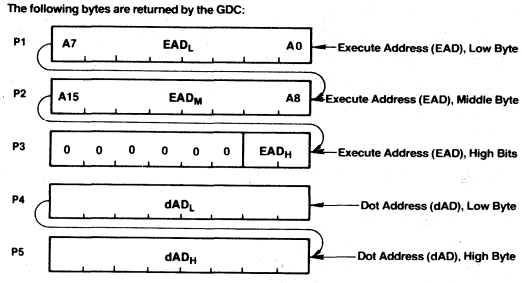
Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes).

As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the GDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost. MOD should be set to 00 if no modification to video buffer is desired.

Cursor Address Read

CURD: 1 1 1 0 0 0 0 0

The following bytes are returned by the GDC:



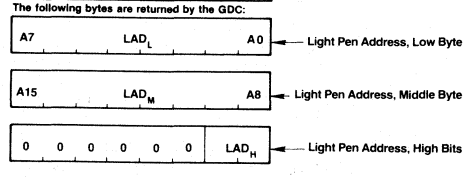
The Execute Address, EAD, points to the display memory word containing the pixel to be addressed.

The Dot Address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

Light Pen Address Read

LPRD: 1 1 0 0 0 0 0 0

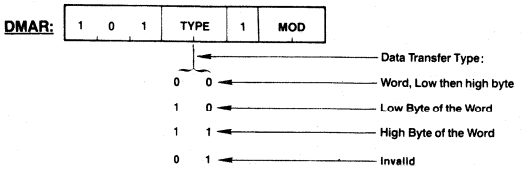
The following bytes are returned by the GDC:



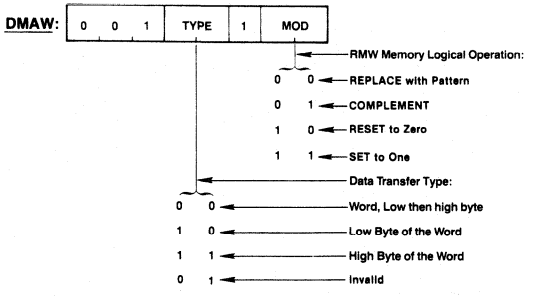
The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.

The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

DMA Read Request



DMA Write Request



Absolute Maximum Ratings* (Tentative)

Ambient Temperature under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on any Pin with respect to Ground	−0.5V to +7V
Power Dissipation	1.5 Watt

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

t_a = 0°C to 70°C; V_{CC} = 5V ± 10%; GND = 0V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5	0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −400 μA
Input Low Leak Current	I_{IL}		−10	μA	V_I = 0V
Input High Leak Current	I_{IH}		+10	μA	V_I = V_{CC}
Output Low Leak Current	I_{OL}		−10	μA	V_O = 0V
Output High Leak Current	I_{OH}		+10	μA	V_O = V_{CC}
Clock Input Low Voltage	V_{CL}	−0.5	0.6	V	
Clock Input High Voltage	V_{CH}	3.9	V_{CC} + 1.0	V	
V_{CC} Supply Current	I_{CC}		270		

Capacitance

t_a = 25°C; V_{CC} = GND = 0V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input Capacitance	C_{IN}		10	pF	fc = 1 MHz
I/O Capacitance	C_{VO}		20	pF	V_I (unmeasured) = 0V
Output Capacitance	C_{OUT}		20	pF	
Clock Input Capacitance	C_ϕ		20	pF	

AC Characteristics

t_A = 0°C to 70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Read Cycle (GDC ↔ CPU)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{AR}	Address Setup to $\overline{RD}$↓	0		ns	
t_{RA}	Address Hold from $\overline{RD}$↑	0		ns	
t_{RR1}	$\overline{PD}$ Pulse Width	t_{RD1} + 20	80	ns	
t_{RD1}	Data Delay from $\overline{RD}$↓		80	ns	C_L = 50 pF
t_{DF}	Data Floating from $\overline{RD}$↑	0	100	ns	
t_{RCY}	$\overline{RD}$ Pulse Cycle	4 t_{CLK}		ns	

Write Cycle (GDC ↔ CPU)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{AW}	Address Setup to $\overline{WR}$↓	0		ns	
t_{WA}	Address Hold from $\overline{WR}$↑	0		ns	
t_{WW}	$\overline{WR}$ Pulse Width	100		ns	
t_{DW}	Data Setup to $\overline{WR}$↑	80		ns	
t_{WD}	Data Hold from $\overline{WR}$↑	0		ns	
t_{WCY}	$\overline{WR}$ Pulse Cycle	4 t_{CLK}		ns	

DMA Read Cycle (GDC ↔ CPU)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{KR}	$\overline{DACK}$ Setup to $\overline{RD}$↓	0		ns	
t_{RK}	$\overline{DACK}$ Hold from $\overline{RD}$↑	0		ns	
t_{RR2}	$\overline{RD}$ Pulse Width	t_{RD2} + 20		ns	
t_{RD2}	Data Delay from $\overline{RD}$↓		1.5 t_{CLK} + 80	ns	C_L = 50 pF
t_{REQ}	DREQ Delay from 2XCCLK↑		120	ns	C_L = 50 pF
t_{QK}	DREQ Setup to $\overline{DACK}$↓	0		ns	
t_{DK}	$\overline{DACK}$ High Level Width	t_{CLK}		ns	
t_E	$\overline{DACK}$ Pulse Cycle	4 t_{CLK}		ns	
$t_{KQ(R)}$	DREQ ↓ Delay from $\overline{DACK}$↓		2 t_{CLK} + 120	ns	C_L = 50 pF

DMA Write Cycle (GDC ↔ CPU)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{KW}	$\overline{DACK}$ Setup to $\overline{WR}$↓	0		ns	
t_{WK}	$\overline{DACK}$ Hold from $\overline{WR}$↑	0		ns	
$t_{KQ(R)}$	DREQ ↓ Delay from $\overline{DACK}$↓		t_{CLK} + 120	ns	C_L = 50 pF

R/M/W Cycle (GDC ↔ Display Memory)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{AD}	Address/Data Delay from 2XCCLK↑		130	ns	C_L = 50 pF
t_{OFF}	Address/Data Floating from 2XCCLK↑	10	130	ns	C_L = 50 pF
t_{DIS}	Input Data Setup to 2XCCLK↓	40		ns	
t_{DIH}	Input Data Hold from 2XCCLK↓	0		ns	
t_{DBI}	DBIN Delay from 2XCCLK↓		90	ns	C_L = 50 pF
t_{RR}	ALE↑ Delay from 2XCCLK↑	30	110	ns	C_L = 50pF
t_{RF}	ALE↓ Delay from 2XCCLK↓	20	90	ns	C_L = 50 pF
t_{RW}	ALE Width	1/3 t_{CLK}		ns	C_L = 50 pF

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Display Cycle (GDC ↔ Display Memory)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{VD}	Video Signal Delay from 2XCCLK↑		120	ns	C_L = 50 pF

Input Cycle (GDC ↔ Display Memory)

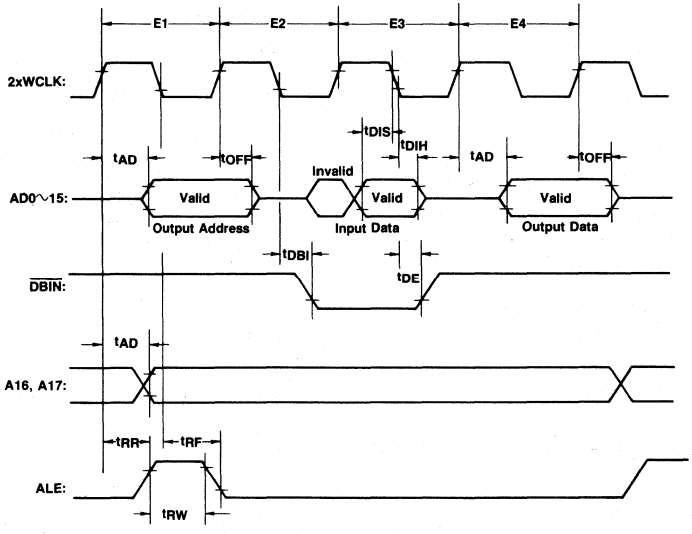
Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{PS}	Input Signal Setup to 2XCCLK↑	20		ns	
t_{PW}	Input Signal Width	t_{CLK}		ns	

Clock

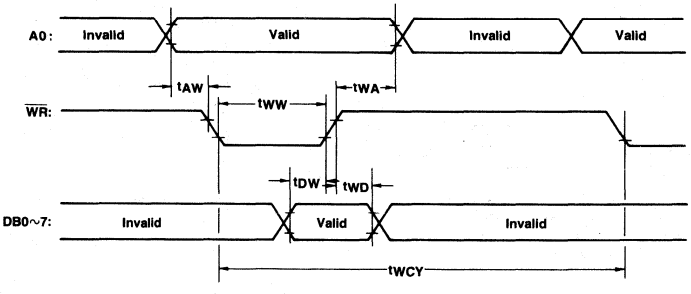
Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
t_{CR}	Clock Rise Time		10	ns	
t_{CF}	Clock Fall Time		10	ns	
t_{CH}	Clock High Pulse Width	95		ns	
t_{CL}	Clock Low Pulse Width	95		ns	
t_{CLK}	Clock Cycle	200	2000	ns	

Timing Waveforms

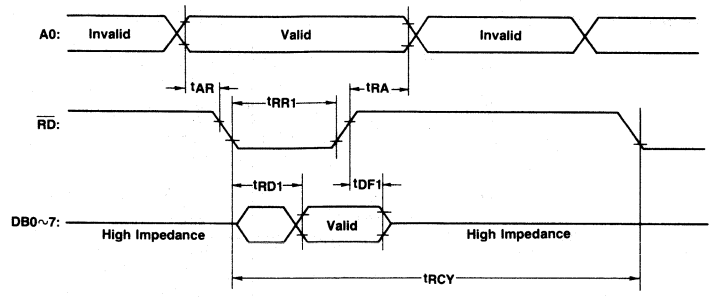
Display Memory RMW Timing



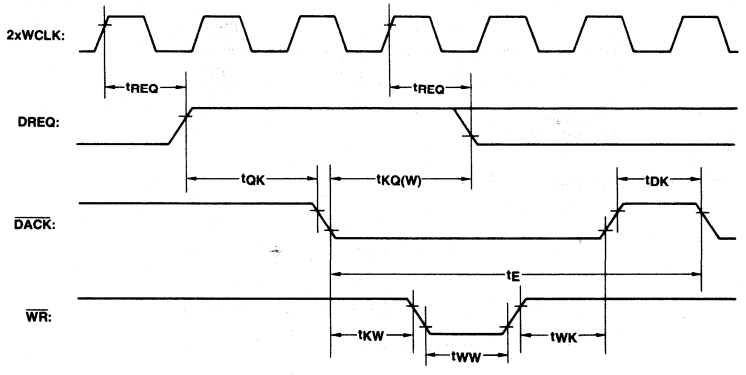
Microprocessor Interface Write Timing



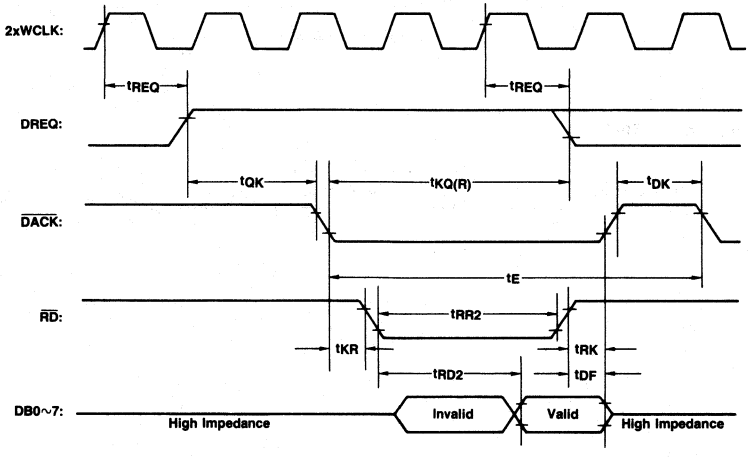
Microprocessor Interface Read Timing



Microprocessor Interface DMA Write Timing



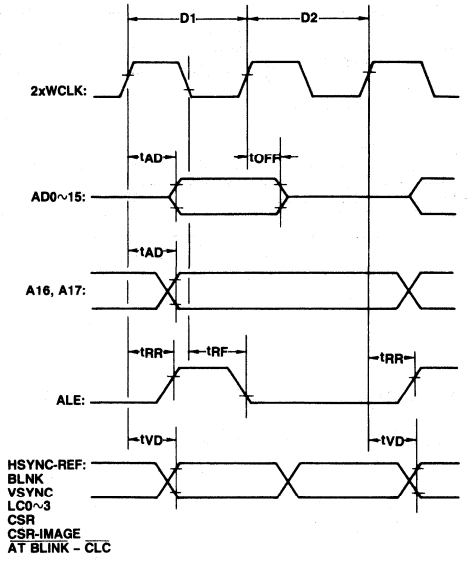
Microprocessor Interface DMA Read Timing



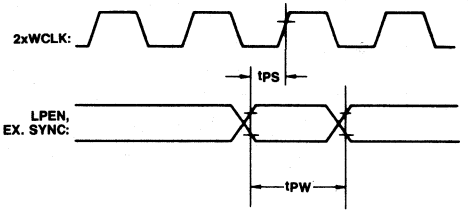
9

Timing Waveforms (Cont.)

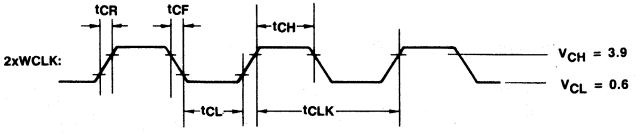
Display Memory Display Cycle Timing



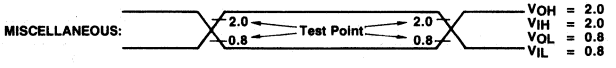
Light Pen and External Sync Input Timing



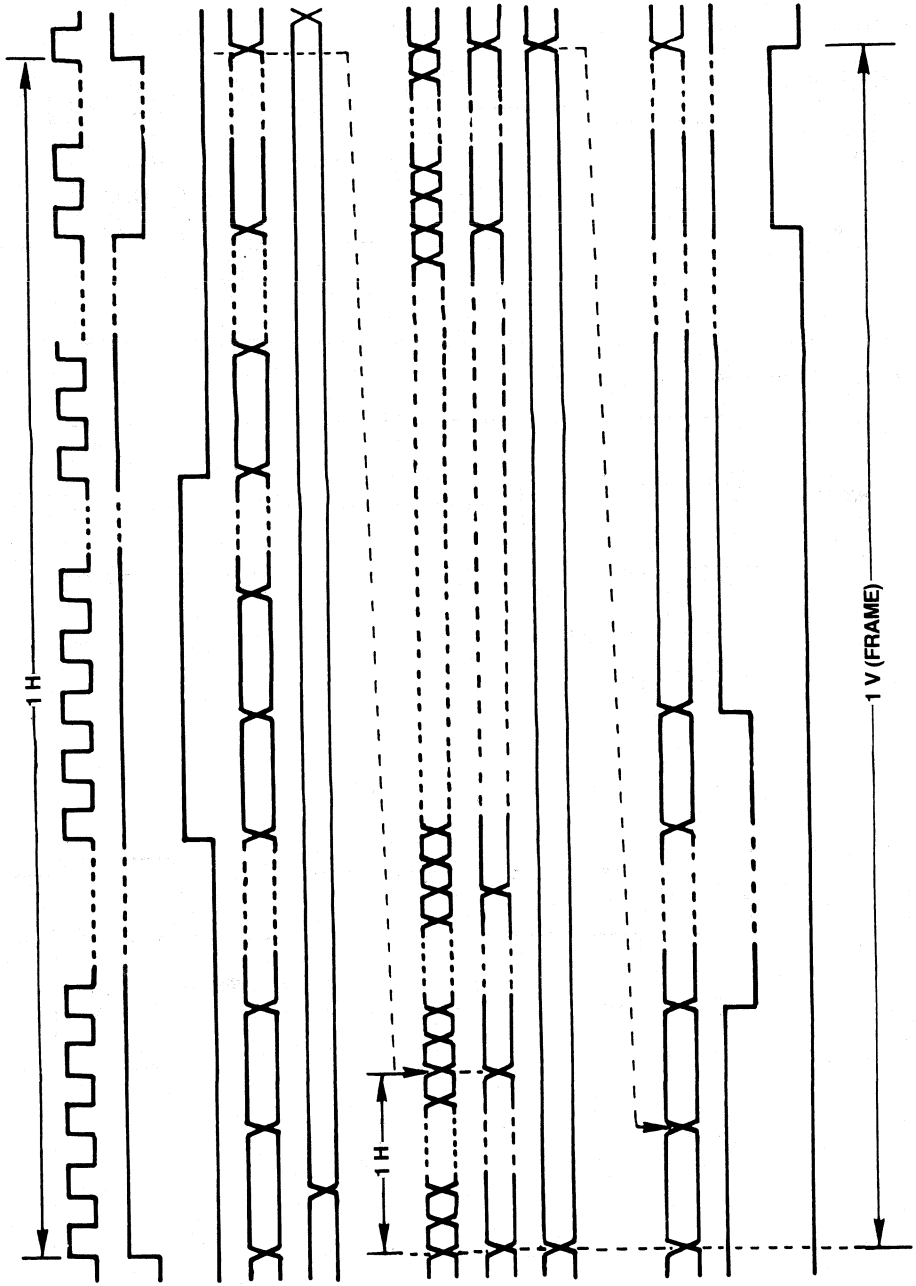
Clock Timing



Test Level (for AC Tests)



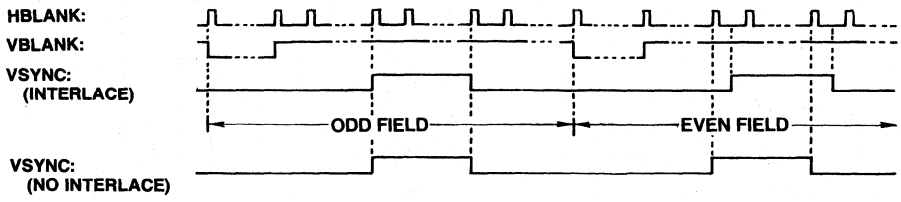
Timing Waveforms (Cont.)



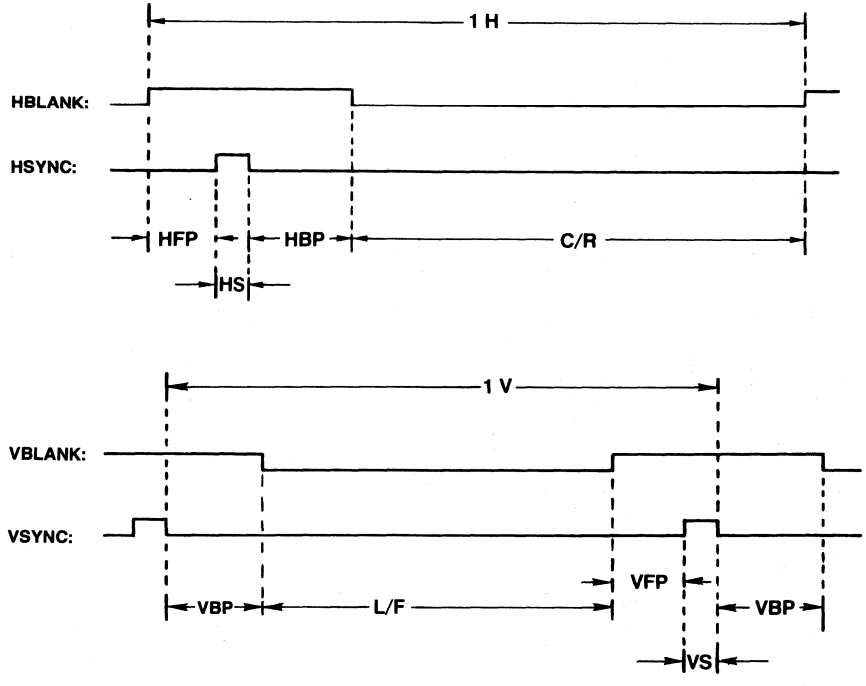
Video Sync Signals Timing

Timing Waveforms (Cont.)

Interlaced Video Timing

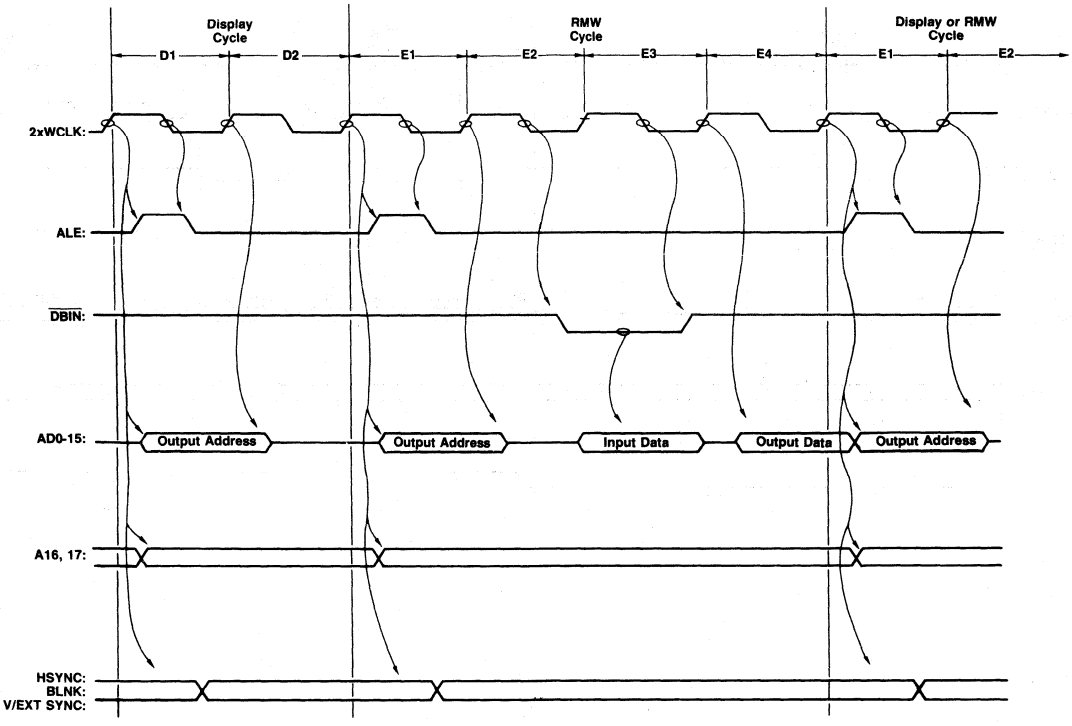


Video Sync Generator Parameters

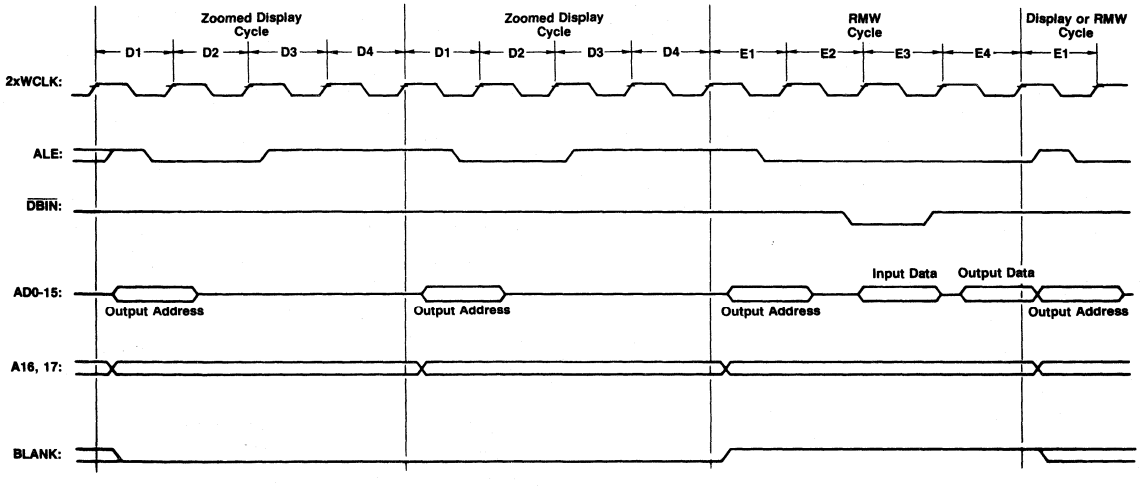


Timing Waveforms (Cont.)

Display and RMW Cycles (1x Zoom)



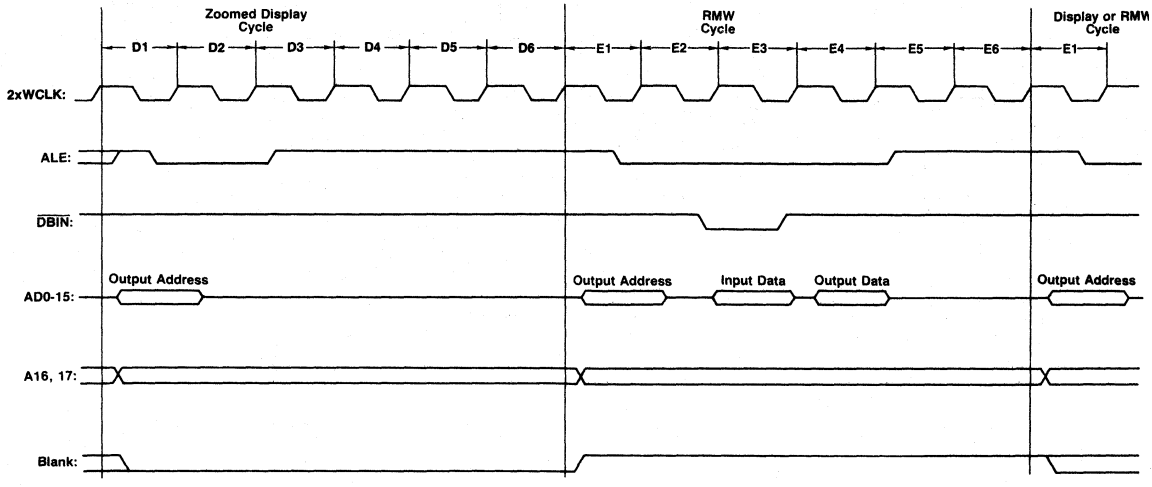
Display and RMW Cycles (2x Zoom)



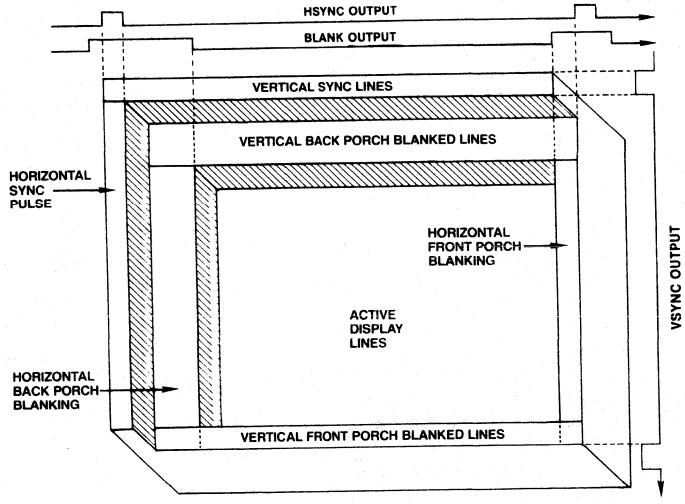
9

Timing Waveforms (Cont.)

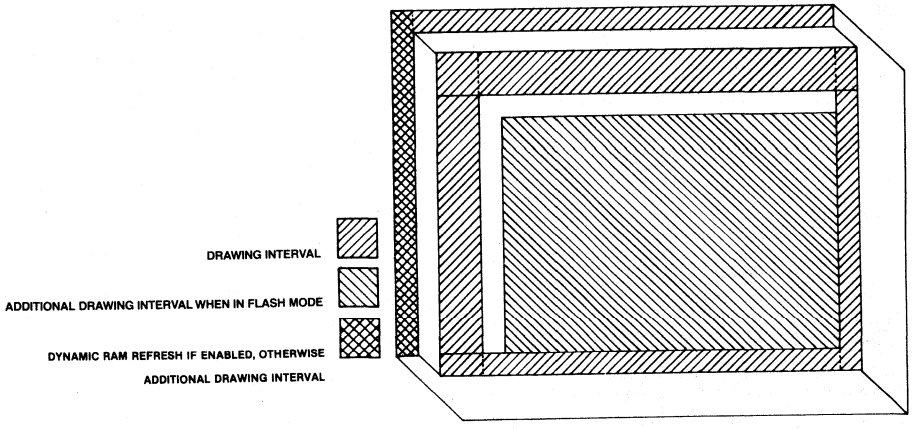
Zoomed Display Operation with RMW Cycle (3x Zoom)



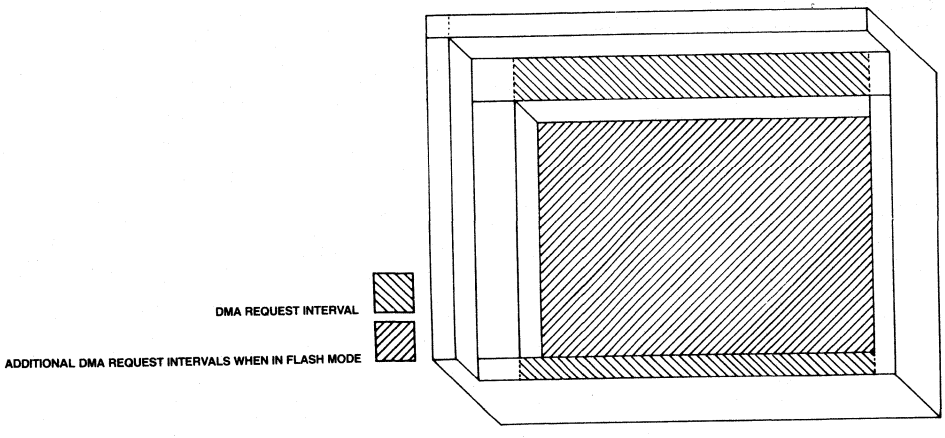
Video Field Timing



Drawing Intervals



DMA Request Intervals

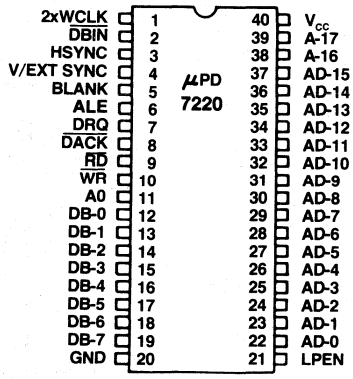


9

Pin Identification

Pin No.	Symbol	Direction	Function
1	2xWCLK	IN	Clock Input
2	$\overline{DBIN}$	OUT	Display Memory Read Input Flag
3	HSYNC	OUT	Horizontal Video Sync Output
4	V/EXT SYNC	IN/OUT	Vertical Video Sync Output or External VSYNC Input
5	BLANK	OUT	CRT Blanking Output
6	ALE ($\overline{RAS}$)	OUT	Address Latch Enable Output
7	DRQ	OUT	DMA Request Output
8	$\overline{DACK}$	IN	DMA Acknowledge Input
9	$\overline{RD}$	IN	Read Strobe Input for Microprocessor Interface
10	$\overline{WR}$	IN	Write Strobe Input for Microprocessor Interface
11	A0	IN	Address Select Input for Microprocessor Interface
12–19	DB0 to 7	IN/OUT	Bidirectional Data Bus to Host Microprocessor
20	GND	—	Ground
21	LPEN	IN	Light Pen Detect Input
22–34	AD0 to 12	IN/OUT	Address and Data Lines to Display Memory
35–37	AD13 to 15	IN/OUT	Utilization Varies with Mode of Operation
38	A16	OUT	Utilization Varies with Mode of Operation
39	A17	OUT	Utilization Varies with Mode of Operation
40	V_{CC}	—	+5V ± 10%

Pin Configuration



Character Mode Pin Utilization

Pin No.	Name	Direction	Function
35–37	AD13 to 15	OUT	Line Counter Bits 0 to 2 Outputs
38	A16	OUT	Line Counter Bit 3 Output
39	A17	OUT	Cursor Output

Mixed Mode Pin Utilization

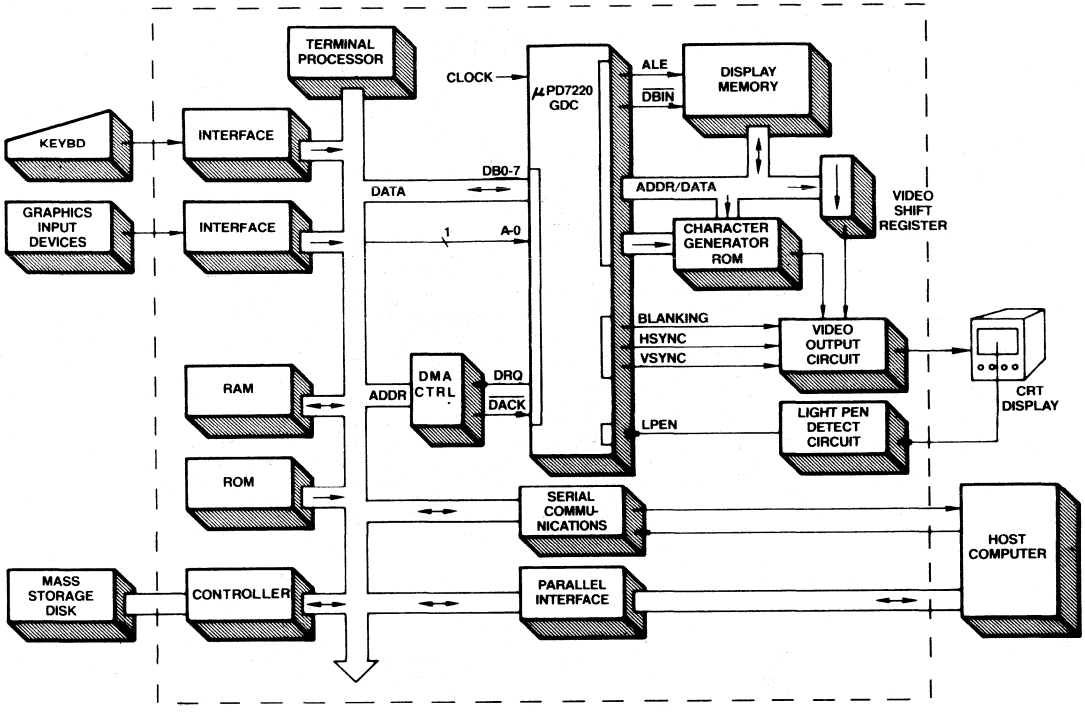
Pin No.	Name	Direction	Function
35–37	AD13 to 15	IN/OUT	Address and Data Bits 13 to 15
38	A16	OUT	Attribute Blink and Clear Line Counter* Output
39	A17	OUT	Cursor and Bit-Map Area* Flag Output

* = Output during the HSYNC interval. Use the trailing edge at HSYNC to clock this value into a flop for reference during the rest of the video line.

Graphics Mode Pin Utilization

Pin No.	Name	Direction	Function
35–37	AD13 to 15	IN/OUT	Address and Data Bits 13 to 15
38	A16	OUT	Address Bit 16 Output
39	A17	OUT	Address Bit 17 Output

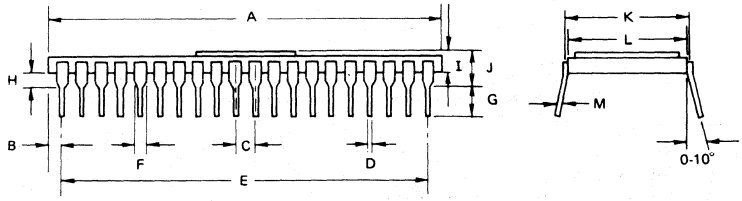
Block Diagram of a Graphics Terminal



9

Package Outlines

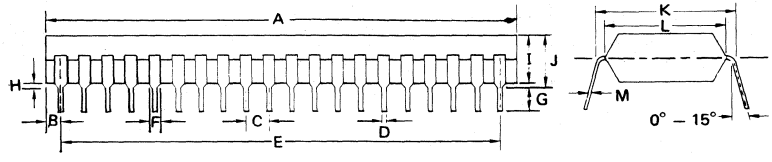
μPD7220D



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

μPD7220C



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD7225
INTELLIGENT ALPHANUMERIC LCD CONTROLLER/DRIVER

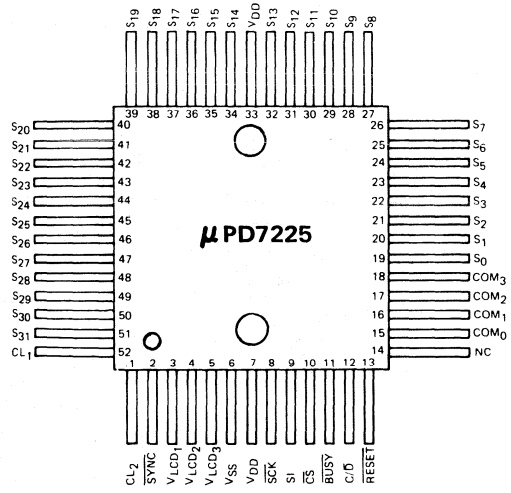
Description

The μPD7225 is an intelligent peripheral device designed to interface most microprocessors with a wide variety of alphanumeric LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 32 segments and is easily cascaded for larger LCD applications. The μPD7225 communicates with a host microprocessor through an 8-bit serial interface. It includes a 7-segment numeric and a 14-segment alphanumeric segment decoder to reduce system software requirements. The μPD7225 is manufactured with low power consumptiom CMOS process allowing use of a single power supply between 2.7V and 5.5V and is available in a space-saving 52-pin flat plastic package.

Features

- ☐ Single-chip LCD Controller with Direct LCD Drive
- ☐ Low-cost Serial Interface to most Microprocessors
- ☐ Compatible with:
  - 7-Segment Numeric LCD Configurations—up to 16 Digits
  - 14-Segment Alphanumeric LCD Configurations—up to 8 Characters
- ☐ Selectable LCD Drive Configuration: Static, Biplexed, Triplexed, or Quadriplexed
- ☐ 32-Segment Drivers
- ☐ Cascadable for Larger LCD Applications
- ☐ Selectable LCD Bias Voltage Configuration: Static, 1/2, or 1/3
- ☐ Hardware Logic Blocks Reduce System Software Requirements
  - — 8-Bit Serial Interface
  - — Two 32 x 4-Bit Static RAMs for Display Data and Blinking Data Storage
  - — Programmable Segment Decoding Capability
    - 16-Character, 7-Segment Numeric Decoder
    - 64-Character, 14-Segment USASCII Alphanumeric Decoder
  - — Programmable Segment Blinking Capability
  - — Automatic Synchronization of Segment Drivers with Sequentially Multiplexed Backplane Drivers
- ☐ Single Power Supply, Variable from 2.7V to 5.5V
- ☐ Low Power Consumption CMOS Technology
- ☐ Extended −40°C to +85°C Temperature Range Available
- ☐ Space-saving 52-Pin Flat Plastic Package

Pin Configuration



Pin Description

Pin No.	Pin Symbol	Function
1	CL_2	System clock output (active high). Connect to CL_1 with 180kΩ resistor, or leave open.
2	$\overline{SYNC}$	Synchronization port (active low). For multichip operation tie all $\overline{SYNC}$ lines together.
3–5	V_{LCD_1}, V_{LCD_2}, V_{LCD_3}	LCD bias voltage supply inputs to LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.
6	V_{SS}	Ground.
7, 33	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
8	$\overline{SCK}$	Serial clock input (active low). Synchronizes 8-bit serial data transfer from microprocessor to μPD7225.
9	SI	Serial input (active high). Data input from microprocessor.
10	$\overline{CS}$	Chip select input (active low). Enables μPD7225 for data input from microprocessor. Display can also be updated when μPD7225 is deselected.
11	$\overline{BUSY}$	Busy output (active low). Handshake line indicates that μPD7225 is ready to receive next data byte.
12	$C/\overline{D}$	Command/data select input (active both high and low). Distinguishes serially input data byte as a command or as display data.
13	$\overline{RESET}$	Reset input (active low). R/C circuit or pulse initializes μPD7225 after power-up.
14	NC	No connection.
15–18	COM_0–COM_3	LCD Backplane Driver Outputs.
19–32, 34–51	S_0–S_{31}	LCD Segment Driver Outputs.
52	CL_1	System clock input (active high). Connect to CL_2 with 180kΩ resistor, or to external clock source.

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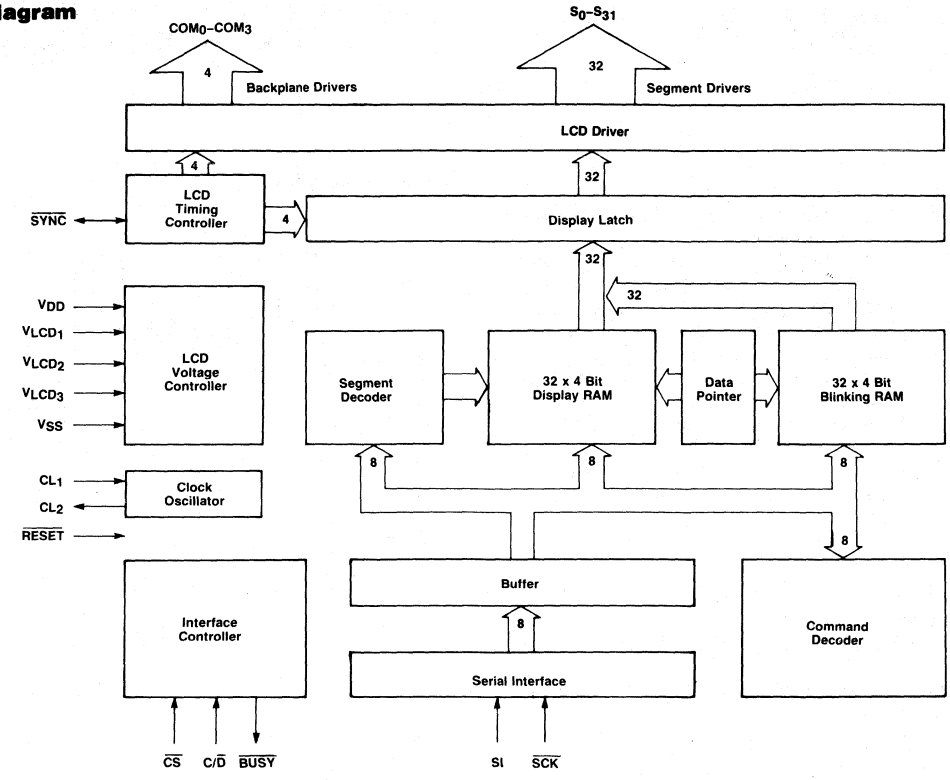
Block Diagram



Command Summary

Command	Description	Instruction Code Binary D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
1. MODE SET	Initialize the μPD7225, including selection of: 1) LCD Drive Configuration 2) LCD Bias Voltage Configuration 3) LCD Frame Frequency	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
2. UNSYNCHRONOUS DATA TRANSFER	Synchronize Display RAM data transfer to Display Latch with $\overline{CS}$	0	0	1	1	0	0	0	0	30
3. SYNCHRONOUS DATA TRANSFER	Synchronize Display RAM data transfer to Display Latch with LCD Drive Cycle	0	0	1	1	0	0	0	1	31
4. INTERRUPT DATA TRANSFER	Interrupt Display RAM data transfer to Display Latch	0	0	1	1	1	0	0	0	38
5. LOAD DATA POINTER	Load Data Pointer with 5 bits of Immediate Data	1	1	1	D_4	D_3	D_2	D_1	D_0	E0-FF
6. CLEAR DISPLAY RAM	Clear the Display RAM and reset the Data Pointer	0	0	1	0	0	0	0	0	20
7. WRITE DISPLAY RAM	Write 4 bits of Immediate Data to the Display RAM location addressed by the Data Pointer; Increment Data Pointer	1	1	0	1	D_3	D_2	D_1	D_0	D0-DF
8. AND DISPLAY RAM	Perform a Logical AND between the Display RAM data addressed by the Data Pointer and 4 bits of Immediate Data; Write result to same Display RAM location. Increment Data Pointer	1	0	0	1	D_3	D_2	D_1	D_0	90-9F

Command	Description	Instruction Code Binary D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
9. OR DISPLAY RAM	Perform a Logical OR between the Display RAM data addressed by the Data Pointer and 4 bits of Immediate Data; Write result to same Display RAM location; Increment Data Pointer	1	0	1	1	D_3	D_2	D_1	D_0	B0-BF
10. ENABLE SEGMENT DECODER	Start use of the Segment Decoder	0	0	0	1	0	1	0	1	15
11. DISABLE SEGMENT DECODER	Stop use of the Segment Decoder	0	0	0	1	0	1	0	0	14
12. ENABLE DISPLAY	Turn on the LCD	0	0	0	1	0	0	0	1	11
13. DISABLE DISPLAY	Turn off the LCD	0	0	0	1	0	0	0	0	10
14. CLEAR BLINKING RAM	Clear the Blinking RAM and reset the Data Pointer	0	0	0	0	0	0	0	0	00
15. WRITE BLINKING RAM	Write 4 bits of Immediate Data to the Blinking RAM location addressed by the Data Pointer; Increment Data Pointer	1	1	0	0	D_3	D_2	D_1	D_0	C0-CF
16. AND BLINKING RAM	Perform a Logical AND between Blinking RAM data addressed by the Data Pointer and 4 bits of Immediate Data; Write result to same Blinking RAM Location; Increment Data Pointer	1	0	0	0	D_3	D_2	D_1	D_0	80-8F
17. OR BLINKING RAM	Perform a Logical OR between Blinking RAM data addressed by the Data Pointer and 4 bits of Immediate Data; Write result to same Blinking Location; Increment Data Pointer	1	0	1	0	D_3	D_2	D_1	D_0	A0-AF
18. ENABLE BLINKING	Start Segment Blinking at the Frequency Specified by 1 bit of Immediate Data	0	0	0	1	1	0	1	D_0	1A-1B
19. DISABLE BLINKING	Stop Segment Blinking	0	0	0	1	1	0	0	0	18

Details of operation and application examples can be found in the "μPD7225 Intelligent Alphanumeric LCD Controller/Driver Technical Manual."

Absolute Maximum Ratings*

T_a = 25°C

Supply Voltage, V_{DD}	−0.3V to +7.0V
All Inputs and Outputs with Respect to V_{SS}	−0.3V to V_{DD} +0.3V
Storage Temperature	−65°C to +150°C
Operating Temperature	−10°C to +70°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C to +70°C; V_{DD} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	
Input Leakage Current High	I_{LIH}			2	μA	V_{IH} = V_{DD}
Input Leakage Current Low	I_{LIL}			−2	μA	V_{IL} = 0V
Output Voltage High	V_{OH}	V_{DD} −0.5			V	$\overline{BUSY}$, $\overline{SYNC}$, I_{OH} = −10 μA
Output Voltage Low	V_{OL_1}			0.5	V	$\overline{BUSY}$, I_{OL} = 100 μA
	V_{OL_2}			1.0	V	$\overline{SYNC}$, I_{OL} = 900 μA
Output Leakage Current Low	I_{LOH}			2	μA	V_{OH} = V_{DD}
	I_{LOL}			−2	μA	V_{OL} = 0V
Output Short Circuit Current	I_{OS}			−300	μA	$\overline{SYNC}$, V_{OS} = 1.0V
Backplane Driver Output Impedance	R_{COM}		5	7	kΩ	COM_0–COM_3, $V_{DD} \geq V_{LCD}$. Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes
Segment Driver Output Impedance	R_{SEG}		7	14	kΩ	S_0–S_{31}, $V_{DD} \geq V_{LCD}$. Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes
Supply Current	I_{DD}		100	250	μA	CL_1 external clock, f_ϕ = 200 KHz

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DC Characteristics (Cont.)

T_a = 0°C to +70°C; V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Voltage High	V_{IH_1}	0.7 V_{DD}		V_{DD}	V	Except $\overline{SCK}$
	V_{IH_2}	0.8 V_{DD}		V_{DD}	V	$\overline{SCK}$
Input Voltage Low	V_{IL_1}	0		0.3 V_{DD}	V	Except $\overline{SCK}$
	V_{IL_2}	0		0.2 V_{DD}	V	$\overline{SCK}$
Input Leakage Current High	I_{LIH}			2	μA	$V_{IH} = V_{DD}$
Input Leakage Current Low	I_{LIL}			−2	μA	V_{IL} = 0V
Output Voltage High	V_{OH}	V_{DD} − 0.75			V	$\overline{BUSY}$, $\overline{SYNC}$, I_{OH} = −7 μA
Output Voltage Low	V_{OL_1}			0.5	V	$\overline{BUSY}$, I_{OL} = 100 μA
	V_{OL_2}			0.5	V	$\overline{SYNC}$, I_{OL} = 400 μA
Output Leakage Current Low	I_{LOH}			2	μA	$V_{OH} = V_{DD}$
	I_{LOL}			−2	μA	V_{OL} = 0V
Output Short Circuit Current	I_{OS}			−200	μA	$\overline{SYNC}$, V_{OS} = 0.5V
Backplane Driver Output Impedance	R_{COM}		6		kΩ	COM_0–COM_3, $V_{DD} \geq V_{LCD}$. Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes
Segment Driver Output Impedance	R_{SEG}		12		kΩ	S_0–S_{31}, $V_{DD} \geq V_{LCD}$. Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes
Supply Current	I_{DD}		30	100	μA	CL_1 external clock, V_{DD} = 3.0V ± 10%, f_ϕ = 140 KHz

AC Characteristics

T_a = −10°C to +70°C; V_{DD} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock Frequency	f_ϕ	50		200	KHz	
	f_{OSC}	85	130	175	KHz	R = 180 kΩ + 5%
Clock Pulse Width High	$t_{\phi W_H}$	2		16	μs	CL_1, external clock
Clock Pulse Width Low	$t_{\phi W_L}$	2		16	μs	CL_1, external clock
$\overline{SCK}$ Cycle	t_{CY_K}	900			ns	
$\overline{SCK}$ Pulse Width High	t_{KW_H}	400			ns	
$\overline{SCK}$ Pulse Width Low	t_{KW_L}	400			ns	
$\overline{BUSY}$↑ to $\overline{SCK}$↓ Hold Time	t_{BH_K}	0			ns	
SI Setup Time to $\overline{SCK}$↑	t_{IS_K}	100			ns	
SI Hold Time After $\overline{SCK}$↑	t_{IH_K}	200			ns	
8th $\overline{SCK}$↑ to $\overline{BUSY}$↓ Delay Time	t_{KD_B}			3	μs	C_{LOAD} = 50 pF
$\overline{CS}$↓ to $\overline{BUSY}$↓ Delay Time	t_{CD_B}			1.5	μs	C_{LOAD} = 50 pF
C/$\overline{D}$ Setup Time to 8th $\overline{SCK}$↑	t_{DS_K}	9			μs	
C/$\overline{D}$ Hold Time After 8th $\overline{SCK}$↑	t_{DH_K}	1			μs	
$\overline{CS}$ Hold Time After 8th $\overline{SCK}$↑	t_{CH_K}	1			μs	
$\overline{CS}$ Pulse Width High	t_{CW_H}	$8/f_\phi$			μs	
$\overline{CS}$ Pulse Width Low	t_{CW_L}	$8/f_\phi$			μs	

AC Characteristics (Cont.)

T_a = 0°C to +70°C; V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock Frequency	f_ϕ	50		140	KHz	
	f_{OSC}	50	100	140	KHz	R = 180 kΩ + 5%, V_{DD} = 3.0V ± 10%
Clock Pulse Width High	$t_{\phi W_H}$	3		16	μs	CL_1, external clock
Clock Pulse Width Low	$t_{\phi W_L}$	3		16	μs	CL_1, external clock
$\overline{SCK}$ Cycle	t_{CY_K}	4			μs	
$\overline{SCK}$ Pulse Width High	t_{KW_H}	1.8			μs	
$\overline{SCK}$ Pulse Width Low	t_{KW_L}	1.8			μs	
$\overline{BUSY}$↑ to $\overline{SCK}$↓ Hold Time	t_{BH_K}	0			ns	
SI Setup Time to $\overline{SCK}$↑	t_{IS_K}	1			μs	
SI Hold Time After $\overline{SCK}$↑	t_{IH_K}	1			μs	
8th $\overline{SCK}$↑ to $\overline{BUSY}$↓ Delay Time	t_{KD_B}			5	μs	C_{LOAD} = 50 pF
$\overline{CS}$↓ to $\overline{BUSY}$↓ Delay Time	t_{CD_B}			5	μs	C_{LOAD} = 50 pF
C/$\overline{D}$ Setup Time to 8th $\overline{SCK}$↑	t_{DS_K}	18			μs	
C/$\overline{D}$ Hold Time After 8th $\overline{SCK}$↑	t_{DH_K}	1			μs	
$\overline{CS}$ Hold Time After 8th $\overline{SCK}$↑	t_{CH_K}	1			μs	
$\overline{CS}$ Pulse Width High	t_{CW_H}	$8/f_\phi$			μs	
$\overline{CS}$ Pulse Width Low	t_{CW_L}	$8/f_\phi$			μs	
$\overline{SYNC}$ Load Capacitance	C_{LOAD}			50	pF	f_ϕ = 200 KHz

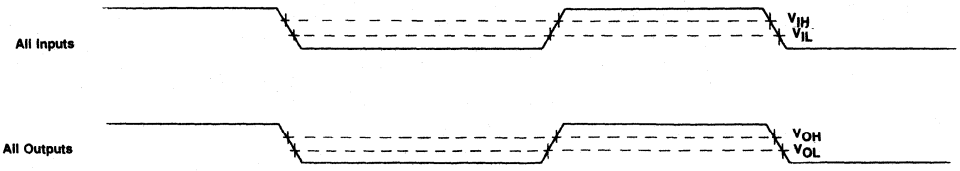
Capacitance

T_a = 25°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10	pF	
Output Capacitance	C_{O_1}			20	pF	Except $\overline{BUSY}$
	C_{O_2}			15	pF	$\overline{BUSY}$
Input/Output Capacitance	C_{IO}			15	pF	$\overline{SYNC}$
Clock Capacitance	C_ϕ			30	pF	CL_1 Input

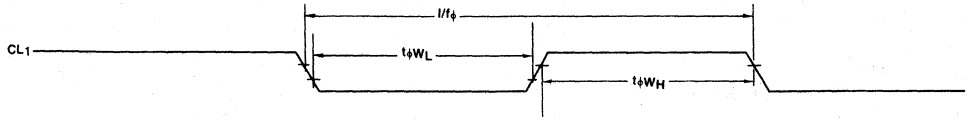
f_ϕ = 1 MHz. Unmeasured pins return to 0V.

AC Timing Characteristics

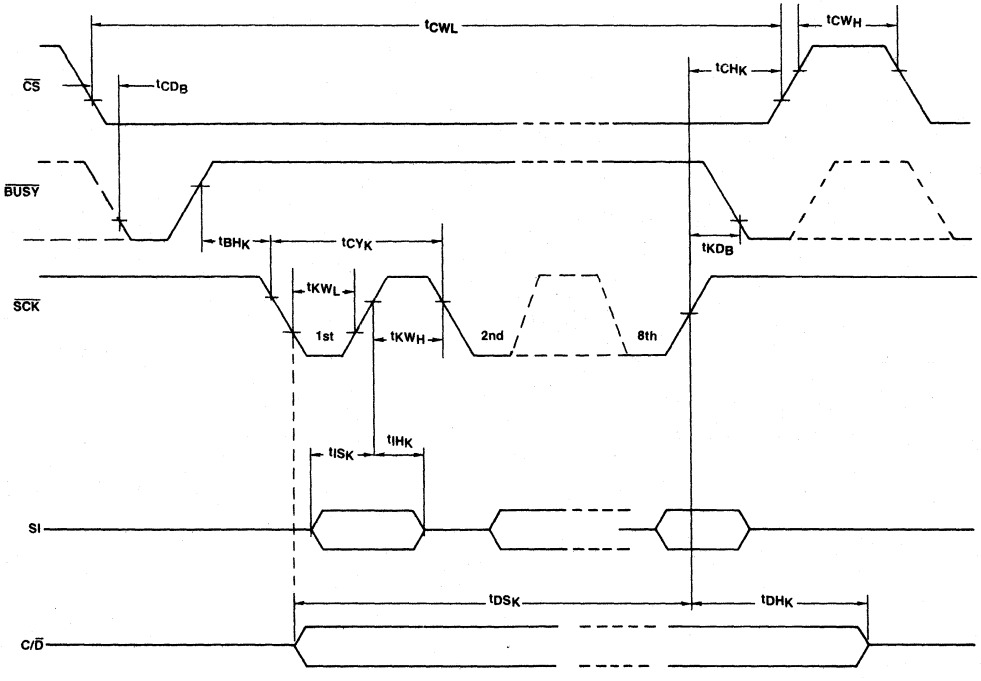


Timing Waveforms

Clock



Serial Interface



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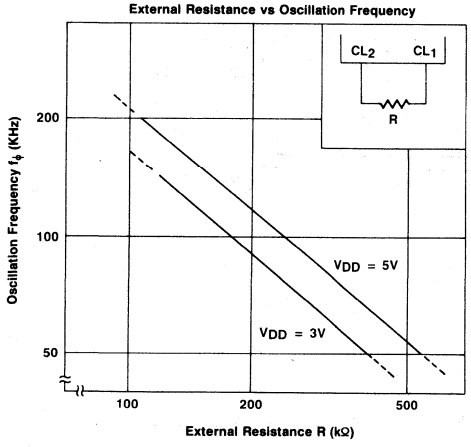
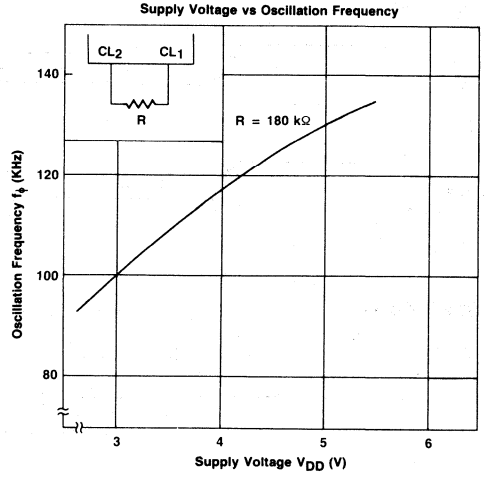
Characteristics Curves

T_a = 25°C

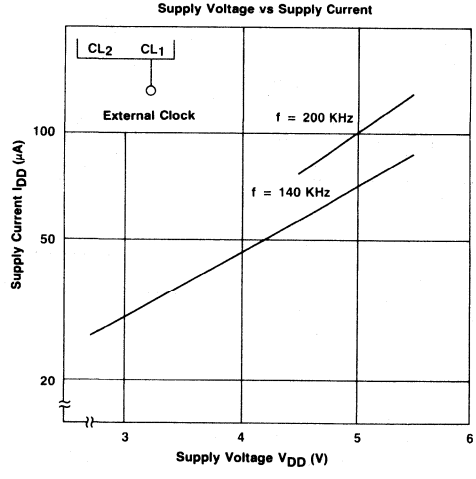
External Resistance vs Oscillation Frequency



Supply Voltage vs Oscillation Frequency



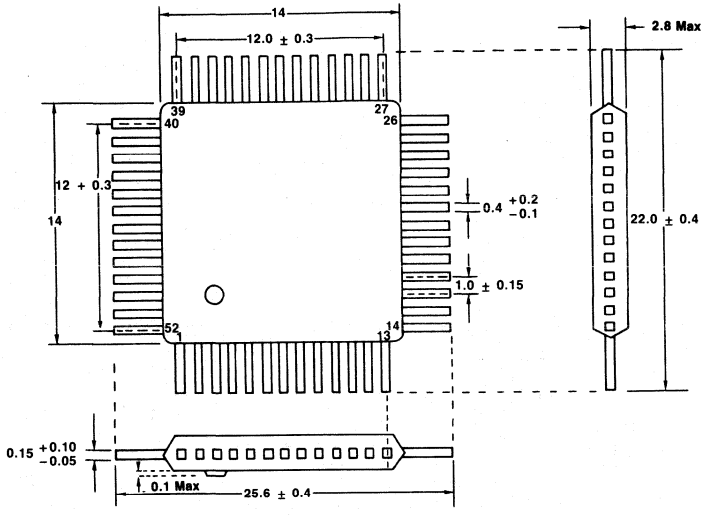
Supply Voltage vs Supply Current



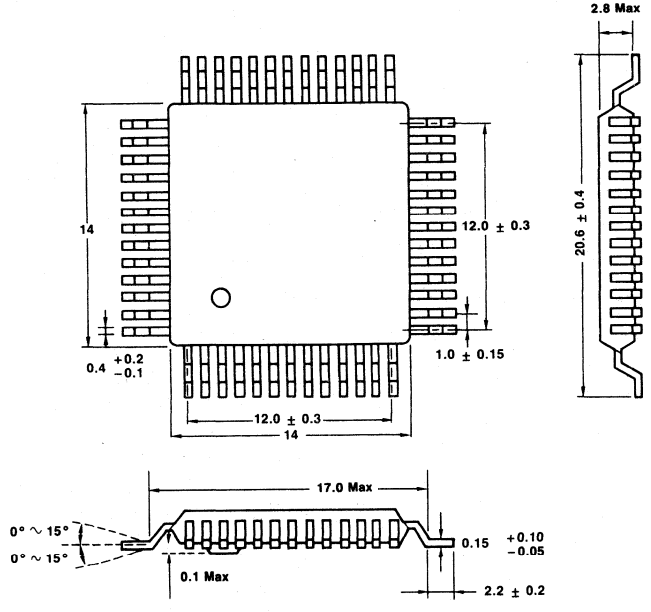
Package Dimensions (Unit: mm)

Use IC Socket IC-53-51 for all packages.

μPD7225G-01



μPD7225G-00



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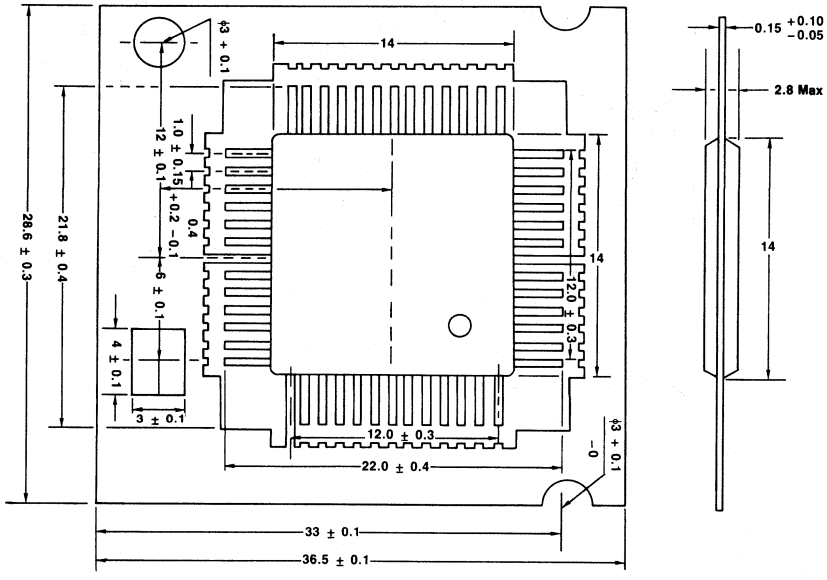
Package Dimensions (Cont.) (Unit: mm)

μPD7225G-A1



μPD7227 INTELLIGENT DOT-MATRIX LCD CONTROLLER/DRIVER

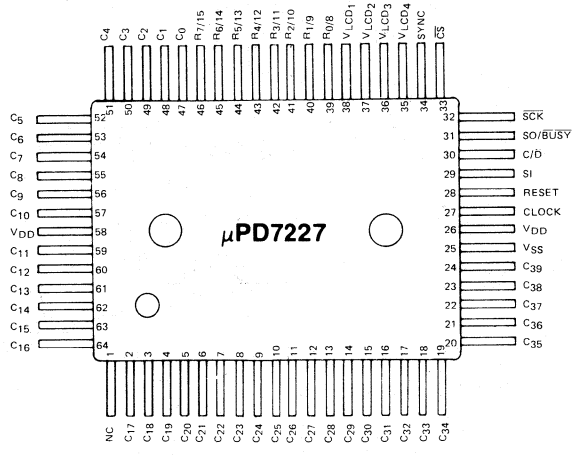
DESCRIPTION

The μPD7227 Intelligent Dot-matrix LCD Controller/Driver is a peripheral device designed to interface most microprocessors with a wide variety of dot matrix LCDs. It can directly drive any multiplexed LCD organized as 8 rows by 40 columns, and is easily cascaded up to 16 rows and 280 columns. The μPD7227 is equipped with several hardware logic blocks, such as an 8-bit serial interface, ASCII character generator, 40 x 16 static RAM with full read/write capability, and an LCD timing controller; all of which reduce microprocessor system software requirements. The μPD7227 is manufactured with a single 5V CMOS process, and is available in a space-saving 64-pin flat plastic package.

FEATURES

- Single-chip LCD controller with direct LCD drive
- Compatible with most microprocessors
- Eight row drives
  - Designed for dot-matrix LCD configurations up to 280 dots
  - Designed for 5 x 7 dot-matrix character LCD configuration; up to 8 characters
  - Cascadable to 16 row drives
- 40 column drives
  - Cascadable to 280 column drives
- Hardware logic blocks reduce system software requirements
  - 8-bit serial interface for communication
  - ASCII 5 x 7 dot-matrix character generator with 64-character vocabulary
  - 40 x 16 bit static RAM for data storage, retrieval, and complete back-up memory capability
  - Voltage controller generates LCD bias voltages
  - Timing controller synchronizes column drives with sequentially-multiplexed row drives
- Single +5V power supply
- CMOS technology

PIN CONFIGURATION



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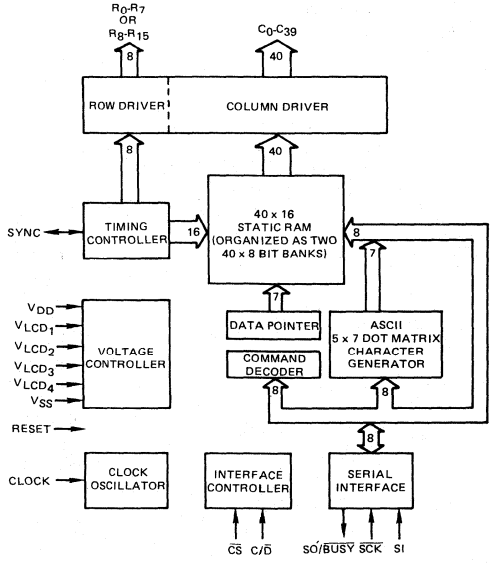
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	NC	No connection.
2-24, 47-57, 59-64	C_0-C_{39}	LCD Column Driver Outputs.
25	V_{SS}	Ground
26, 58	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
27	CLOCK	System Clock input (active high) connect to external clock source.
28	RESET	Reset input (active high). R/C circuit or pulse initializes μPD7227 after power-up.
29	SI	Serial input (active high). Data input from microprocessor.
30	C/$\overline{D}$	Command/Data Select input (active both high and low). Distinguishes serially input data byte as a command or as display data.
31	SO/$\overline{BUSY}$	Serial Output (active high)/Busy output (active low). Data output from μPD7227 to microprocessor when in READ MODE and C/$\overline{D}$ is low. Handshake output indicates that μPD7227 is ready to receive/send next data byte.
32	$\overline{SCK}$	Serial Clock input (active low). Synchronizes 8-bit serial data transfer between microprocessor and μPD7227.
33	$\overline{CS}$	Chip Select Input (active low) enables μPD7227 for communication with microprocessor.
34	SYNC	Synchronization port (active high). For multichip operation tie all SYNC lines together, and configure with MODE SET command.
35-38	V_{LCD_1}, V_{LCD_2}, V_{LCD_3}, V_{LCD_4}	LCD Bias Voltage supply inputs to LCD Voltage Controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.
39-46	$R_{0/8}$-$R_{7/15}$	LCD Row Driver Outputs.

BLOCK DIAGRAM



COMMAND SUMMARY

Command	Description	Instruction Code								
		Binary								HEX
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1. MODE SET	Initialize the μPD7227, including selection of 1. LCD Drive Configuration 2. Row Driver Port Function 3. RAM Bank 4. SYNC Port Function	0	0	0	1	1	D_2	D_1	D_0	18-1F
2. FRAME FREQUENCY SET	Set LCD Frame Frequency	0	0	0	1	0	D_2	D_1	D_0	10-17
3. LOAD DATA POINTER	Load Data Pointer with 7 bits of Immediate Data	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0	80-E7
4. WRITE MODE	Write Display Byte in Serial Register to RAM location addressed by Data Pointer; modify Data Pointer	0	1	1	0	0	1	D_1	D_0	64-67
5. READ MODE	Load RAM contents addressed by Data Pointer into Serial Register for output; modify Data Pointer	0	1	1	0	0	0	D_1	D_0	60-63
6. AND MODE	Perform a Logical AND between the display byte in the Serial Register and the RAM contents addressed by Data Pointer; write result to same RAM location; modify Data Pointer	0	1	1	0	1	1	D_1	D_0	6C-6F
7. OR MODE	Perform a Logical OR between the display byte in the Serial Register and the RAM contents addressed by Data Pointer; write Result to same RAM location; modify Data Pointer	0	1	1	0	1	0	D_1	D_0	68-6B
8. CHARACTER MODE	Decode display byte in Serial Register into 5 x 7 character with Character Generator; write character to RAM location addressed by Data Pointer; increment Data Pointer by 5	0	1	1	1	0	0	1	0	72
9. SET BIT	Set single bit of RAM location addressed by Data Pointer; modify Data Pointer	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
10. RESET BIT	Reset single bit of RAM location addressed by Data Pointer; modify Data Pointer	0	0	1	D_4	D_3	D_2	D_1	D_0	20-3F
11. ENABLE DISPLAY	Turn on the LCD	0	0	0	0	1	0	0	1	09
12. DISABLE DISPLAY	Turn off the LCD	0	0	0	0	1	0	0	0	08

Further details of operation can be found in the "μPD7227 Intelligent Dot-Matrix LCD Controller/Driver Technical Manual."

ABSOLUTE MAXIMUM RATINGS*

Power Supply, V_{DD} . . . . . -0.3V to +7.0V
All inputs and outputs with respect to V_{SS} . . . . . -0.3V to V_{DD} +0.3
Storage Temperature . . . . . -40°C to +125°C
Operating Temperature . . . . . -10°C to +70°C

T_a = 25°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = -10°C to +70°C, V_{DD} = + 5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	CONDITIONS
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	
Input Leakage Current High	I_{LIH}			+10	μA	$V_{IH} = V_{DD}$
Input Leakage Current Low	I_{LIL}			-10	μA	V_{IH} = 0V
Output Voltage High	V_{OH_1}	V_{DD}-0.5			V	SO/$\overline{BUSY}$, I_{OH} = -400 μA
	V_{OH_2}					SYNC, I_{OH} = -100 μA
Output Voltage Low	V_{OL_1}			0.45	V	SO/$\overline{BUSY}$, I_{OL} = +1.7mA
	V_{OL_2}					SYNC, I_{OL} = +100 μA
Output Leakage Current High	I_{LOH}			+10	μA	$V_{OH} = V_{DD}$
Output Leakage Current Low	I_{LOL}			-10	μA	V_{OL} = 0V
LCD Operating Voltage	V_{LCD}	3.0		V_{DD}	V	8-Row Multiplexed LCD Drive Configuration
			V_{DD}			16-Row Multiplexed LCD Drive Configuration
Row Drive Output Impedance	R_{ROW}		4	8	kΩ	
Column Drive Output Impedance	R_{COLUMN}		10	15	kΩ	
Supply Current	I_{DD}		200	400	μA	fφ = 400 KHz

CAPACITANCE

T_a = -25°C, V_{DD} = 0V

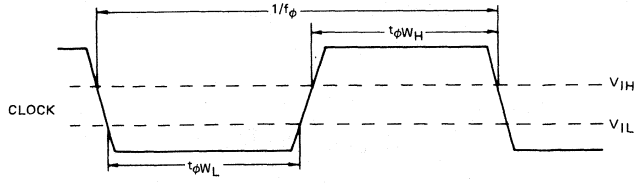
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	CONDITIONS
Input Capacitance	C_I			10	pF	fφ = 1 MHz
Output Capacitance	C_O			25	pF	Unmeasured pins returned to Ground.
Input/Output Capacitance	C_{IO}			15	pF SYNC	

AC CHARACTERISTICS

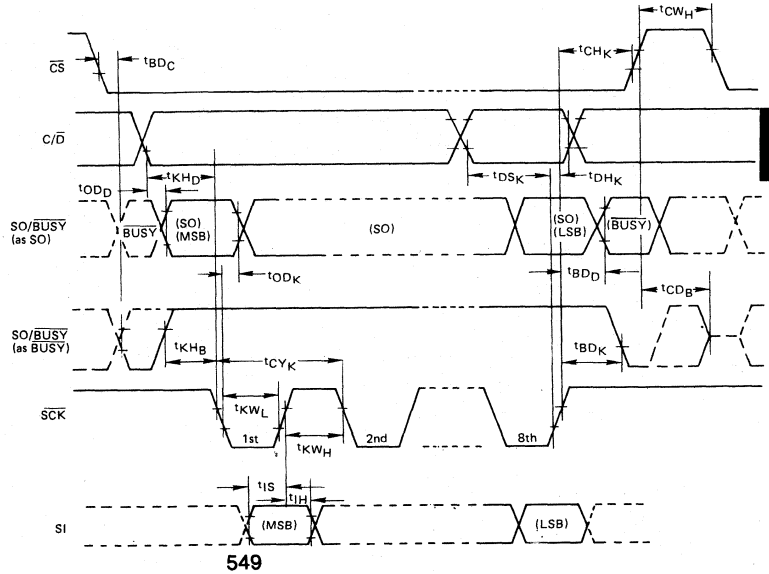
T_a = −10°C to +70°C, V_{DD} = +5.0V ±10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	CONDITIONS
Clock Frequency	$f\phi$	100		1000	KHz	
Clock Pulse Width High	$t\phi W_H$	400			ns	
Clock Pulse Width Low	$t\phi W_L$	400			ns	
$\overline{SCK}$ Cycle	t_{CY_K}	0.9			μs	
$\overline{SCK}$ Pulse Width High	t_{kW_H}	400			ns	
$\overline{SCK}$ Pulse Width Low	t_{KW_L}	400			ns	
$\overline{SCK}$ Hold Time After $\overline{BUSY}$↑	t_{KH_B}	0			ns	
SI Setup Time To $\overline{SCK}$↑	t_{IS_K}	100			ns	
SI Hold Time After $\overline{SCK}$↑	t_{IH_K}	250			ns	
SO Delay Time After $\overline{SCK}$↓	t_{OD_K}			320	ns	C_{LOAD} = 50 pF
SO Delay Time After C/$\overline{D}$↓	t_{OD_D}			2	μs	
$\overline{SCK}$ Hold Time After C/$\overline{D}$↓	t_{KH_D}	2			μs	
$\overline{BUSY}$ Delay Time After 8th $\overline{SCK}$↑	t_{BD_K}			3	μs	
$\overline{BUSY}$ Delay Time After C/$\overline{D}$↑	t_{BD_D}			2	μs	
$\overline{BUSY}$ Delay Time After $\overline{CS}$↓	t_{BD_C}			2	μs	
C/$\overline{D}$ Setup Time to 8th $\overline{SCK}$↑	t_{DS_K}	2			μs	
C/$\overline{D}$ Hold Time After 8th $\overline{SCK}$↑	t_{DH_K}	2			μs	
$\overline{CS}$ Hold Time After 8th $\overline{SCK}$↑	t_{CH_K}	2			μs	
$\overline{CS}$ Pulse Width High	t_{CW_H}	2/$f\phi$			μs	
$\overline{CS}$↑ Delay Time to $\overline{BUSY}$ Floating	t_{CD_B}	2			μs	C_{LOAD} = 50 pF
SYNC Load Capacitance	C_{LOAD_S}			100	pF	

CLOCK WAVEFORM



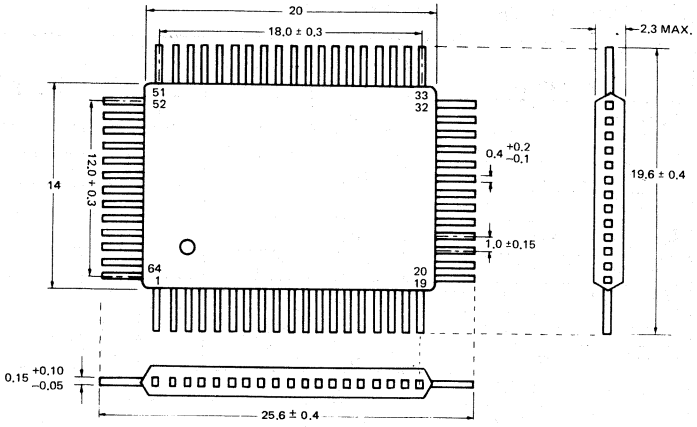
SERIAL INTERFACE TIMING WAVEFORMS



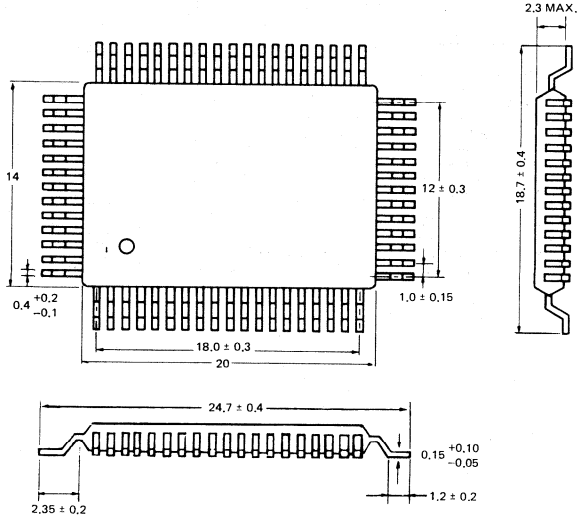
9

PACKAGE DIMENSIONS
(UNIT:mm)
Use I.C. socket #IC-51-595

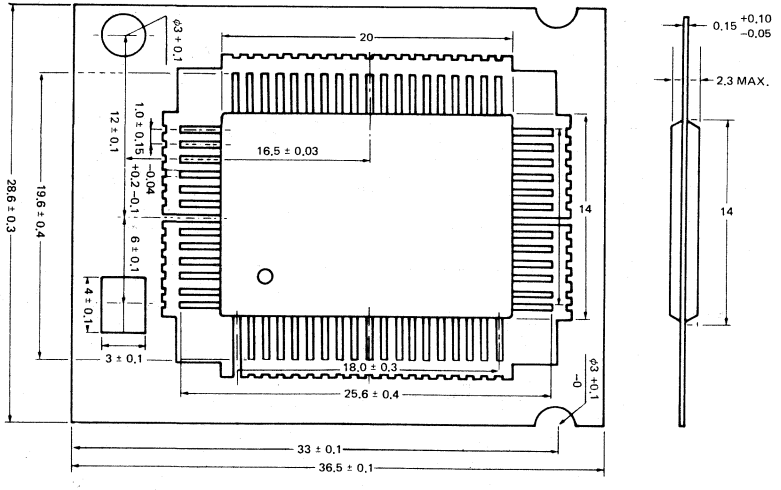
μPD7227G-11



μPD7227G-12



μPD7227G-B1



DIGITAL SIGNAL PROCESSOR

DESCRIPTION

The NEC μPD7720 Signal Processing Interface (SPI) is an advanced architecture microcomputer optimized for signal processing algorithms. Its speed and flexibility allow the SPI to efficiently implement signal processing functions in a wide range of environments and applications.

The NEC SPI is the state of the art in signal processing today, and for the future.

APPLICATIONS

- Speech Synthesis and Analysis
- Digital Filtering
- Fast Fourier Transforms (FFT)
- Dual-Tone Multi-Frequency (DTMF) Transmitters/Receivers
- High Speed Data Modems
- Equalizers
- Adaptive Control
- Sonar/Radar Image Processing
- Numerical Processing

PERFORMANCE BENCHMARKS

• Second Order Digital Filter (BiQuad)	2.25 μs
• SINE/COS of Angles	5.25 μs
• μ/A LAW to Linear Conversion	0.50 μs
• FFT: 32 Point Complex	0.7 ms
64 Point Complex	1.6 ms

FEATURES

- Fast Instruction Execution – 250 ns
- 16-Bit Data Word
- Multi-Operation Instructions for Optimizing Program Execution
- Large Memory Capacities
  - Program ROM 512 x 23 Bits
  - Coefficient ROM 510 x 13 Bits
  - Data RAM 128 x 16 Bits
- Fast (250 ns) 16 x 16-31 Bit Multiplier
- Dual Accumulators
- Four Level Subroutine Stack for Program Efficiency
- Multiple I/O Capabilities
  - Serial
  - Parallel
  - DMA
- Compatible with Most Microprocessors, Including:
  - μPD8080
  - μPD8085
  - μPD8086
  - μPD780 (Z80™*)
- Power Supply +5V
- Technology NMOS
- Package – 28 Pin Dip

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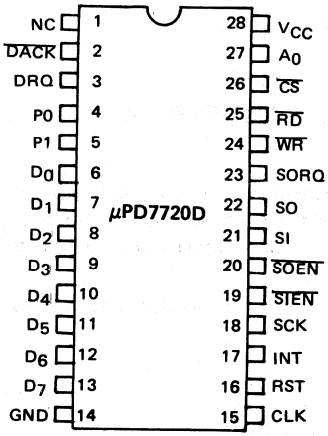
*Z80 is a registered trademark of Zilog Corporation.

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

Fabricated in high speed NMOS, the μPD7720 SPI is a complete 16-bit microcomputer on a single chip. ROM space is provided for program and coefficient storage, while the on-chip RAM may be used for temporary data, coefficients and results. Computational power is provided by a 16-bit Arithmetic/Logic Unit (ALU) and a separate 16 x 16-bit fully parallel multiplier. This combination allows the implementation of a "sum of products" operation in a single 250 nsec instruction cycle. In addition, each arithmetic instruction provides for a number of data movement operations to further increase throughput. Two serial I/O ports are provided for interfacing to codecs and other serially-oriented devices while a parallel port provides both data and status information to conventional μP for more sophisticated applications. Handshaking signals, including DMA controls, allow the SPI to act as a sophisticated programmable peripheral as well as a stand alone microcomputer.

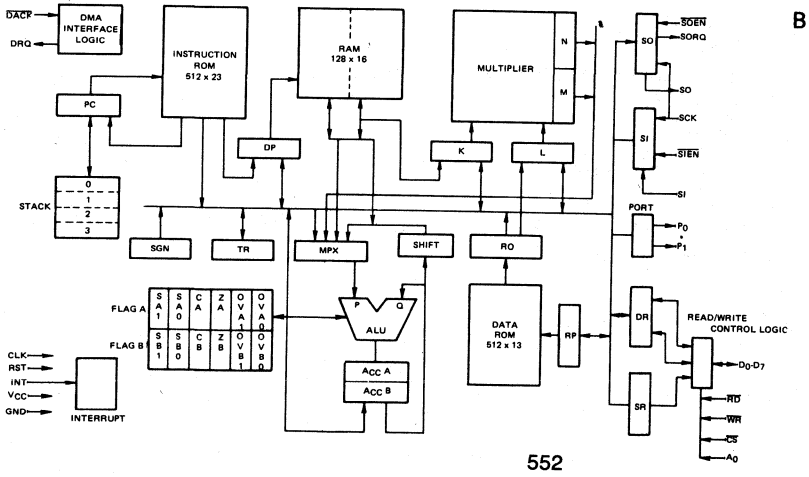
MEMORY

Memory is divided into three types, Program ROM, Data ROM, and Data RAM. The 512 x 23-bit words of Program ROM are addressed by a 9-bit Program Counter which can be modified by an external reset, interrupt, call, jump, or return instruction.

The Data ROM is organized in 512 x 13-bit words and is also addressed through a 9-bit ROM pointer (RP Reg.) which may be modified as part of an arithmetic instruction so that the next value is available for the next instruction. The Data ROM is ideal for storing the necessary coefficients, conversion tables and other constants for all your processing needs.

The Data RAM is 128 x 16-bit words and is addressed through a 7-bit Data Pointer (DP Reg.). The DP has extensive addressing features that operate simultaneously with arithmetic instructions so that no added time is taken for addressing or address modification.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN	NAME	I/O	FUNCTION
1	NC	I	No Connection.
2	$\overline{DACK}$	I	DMA Request Acknowledge. Indicates to the μPD7720 that the Data Bus is ready for a DMA transfer. ($\overline{DACK} = \overline{CS} \bullet A_0 = 0$)
3	DRQ	O	DMA Request signals that the μPD7720 is requesting a data transfer on the Data Bus.
4,5	P_0, P_1	O	P_0, P_1 are general purpose output control lines.
6-13	D_0-D_7	I/O Tristate	Port for data transfer between the Data Register or Status Register and Data Bus.
14	GND		
15	CLK	I	Single phase Master Clock input.
16	RST	I	Reset initializes the μPD7720 internal logic and sets the PC to 0.
17	INT	I	Interrupt. A low to high transition on this pin will (if interrupts are enabled by the program) execute a call instruction to location 100H.
18	SCK	I	Serial Data Input/Output Clock. A serial data bit is transferred when this pin is high.
19	$\overline{SIEN}$	I	Serial Input Enable. This line enables the shift clock to the Serial Input Register.
20	$\overline{SOEN}$	I	Serial Output Enable. This pin enables the shift clock to the Serial Output Register.
21	SI	I	Serial Data Input. This pin inputs 8 or 16 bit serial data words from an external device such as an A/D converter.
22	SO	O	Serial Data Output. This pin outputs 8 or 16 bit data words to an external device such as an D/A converter.
23	SORQ	O	Serial Data Output Request. Specifies to an external device that the Serial Data Register has been loaded and is ready for output. SORQ is reset when the entire 8 or 16 bit word has been transferred.
24	$\overline{WR}$	I	Write Control Signal writes the contents of data bus into the Data Register.
25	$\overline{RD}$	I	Read Control Signal. Enables an output to the Data Port from the Data or Status Register.
26	$\overline{CS}$	I	Chip Select. Enables data transfer with Data or Status Port with $\overline{RD}$ or $\overline{WR}$.
27	A_0	I	Selects Data Register for Read/Write (low) or Status Register for read (high).
28	V_{CC}		+5V Power

ARITHMETIC CAPABILITIES

General

One of the unique features of the SPI's architecture is its arithmetic facilities. With a separate multiplier, ALU, and multiple internal data paths, the SPI is capable of carrying out a multiply, an add, or other arithmetic operation, and move data between internal registers in a single instruction cycle.

ALU

The ALU is a 16-bit 2's complement unit capable of executing 16 distinct operations on virtually any of the SPI's internal registers, thus giving the SPI both speed and versatility for efficient data management.

Accumulators (ACCA/ACCB)

Associated with the ALU are a pair of 16-bit accumulators, each with its own set of flags, which are updated at the end of each arithmetic instruction (except NOP). In addition to Zero Result, Sign Carry, and Overflow Flags, the SPI incorporates auxiliary Overflow and Sign Flags (SA1, SB1, OVA1, OVB1). These flags enable the detection of an overflow condition and maintain the correct sign after as many as 3 successive additions or subtractions.

FLAG A	SA1	SA0	CA	ZA	OVA1	OVA0
FLAG B	SB1	SB0	CB	ZB	OVB1	OVB0

ACC A/B FLAG REGISTERS

Sign Register (SGN)

When OVA1 (or OVB1) is set, the SA1 (or SB1) bit will hold the corrected sign of the overflow. The SGN Register will use SA1 (SB1) to automatically generate saturation constants 7FFFH(+) or 8000H(−) to permit efficient limiting of a calculated valve.

Multiplier

Thirty-one bit results are developed by a 16 x 16 bit 2's complement multiplier in 250 ns. The result is automatically latched in 2-16-bit registers M&N (LSB in N is zero) at the end of each instruction cycle. The ability to have a new product available and to be able to use it in each instruction cycle, provides significant advantages in maximizing processing speed for real time signal processing.

Stack

The SPI contains a 4-level program stack for efficient program usage and interrupt handling.

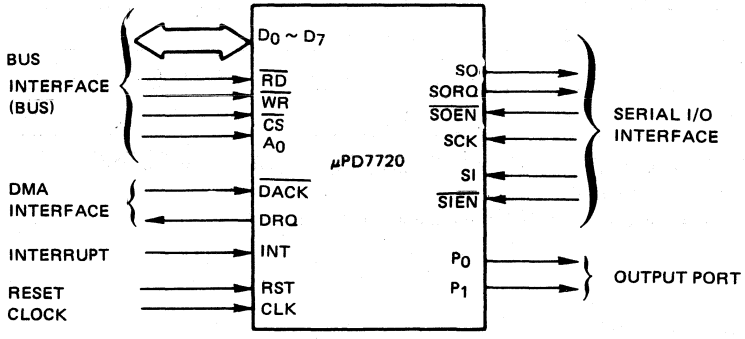
Interrupt

A single level interrupt is supported by the SPI. Upon sensing a high level on the INT terminal, a subroutine call to location 100H is executed. The EI bit of the status register is automatically reset to 0 thus disabling the interrupt facilities until reenabled under program control.

INPUT/OUTPUT

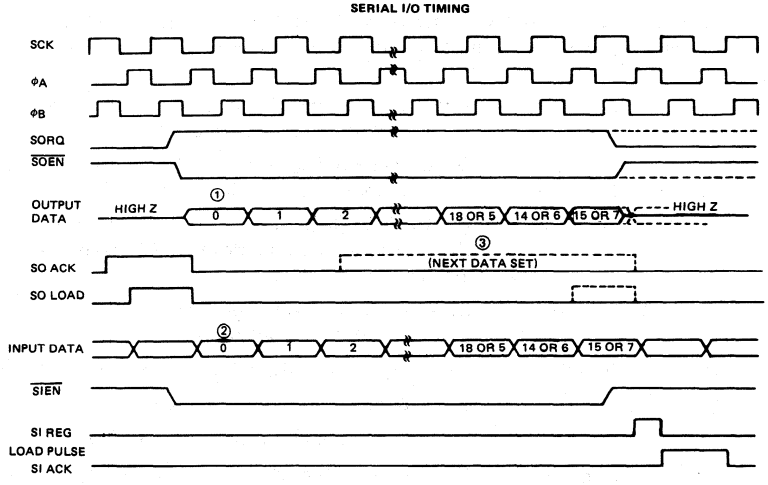
General

The NEC SPI has 3 communication ports; 2 serial and one 8-bit parallel, each with their own control lines for interface handshaking. The parallel port also includes DMA control lines (DRQ and $\overline{DACK}$) for high speed data transfer and reduced processor overhead. A general purpose 2 bit output (see Figure 1) port, rounds out a full complement of interface capability.



Serial I/O

Two shift registers (SI, SO) that are software-configurable to 8 or 16 bits and are externally clocked (SCK) provide simple interface between the SPI and serial peripherals such as, A/D and D/A converters, codecs, or other SPIs.



① Data clocked out on falling edge of SCK.
② Data clocked in on rising edge of SCK.
③ Broken line denotes consecutive sending of next data.

PARALLEL I/O

The 8-bit parallel I/O port may be used for transferring data or reading the SPI's status. Data transfer is handled through a 16-bit Data Register (DR) that is software-configurable for double or single byte data transfers. The port is ideally suited for operating with 8080, 8085 and 8086 processor buses and may be used with other processors and computer systems.

PARALLEL R/W OPERATION

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	OPERATION
1	X	X	X	No effect on internal operation. D_0-D_7 are at high impedance levels.
X	X	1	1	
0	0	0	1	Data from D_0-D_7 is latched to DR ①
0	0	1	0	Contents of DR are output to D_0-D_7 ①
0	1	0	1	Illegal
0	1	1	0	Eight MSBs of SR are output to D_0-D_7
0	X	0	0	Illegal

① Eight MSBs or 8 LSBs of data register (DR) are used depending on DR status bit (DRS).
The condition of $\overline{DACK}$ = 0 is equivalent to $A_0 = \overline{CS} = 0$.

Status Register (SR)

MSB LSB

RQM	USF1	USF0	DRS	DMA	DRC	SOC	SIC	EI	0	0	0	0	0	P1	P0

The status register is a 16-bit register in which the 8 most significant bits may be read by the system's MPU for the latest I/O and processing status.

RQM — (Request for Master): A read or write from DR to IDB sets RQM = 1. An Ext read (write) resets RQM = 0.

USF1 — (User Flag 1):
USF0 — (User Flag 0): General purpose flags which may be read by an external processor for user defined signalling

DRS — (DR Status): For 16 bit DR transfers (DRC = 0) DRS = 1 after first 8 bits have been transferred, DRS = 0 after all 16 bits

DMA— (DMA Enable): DMA = 0 (Non DMA transfer mode)
DMA = 1 (DMA transfer mode)

DRC — (DR Control): DRC = 0 (16 bit mode), DRC = 1 (8 bit mode)

SOC — (SO Control): SOC = 0 (16 bit mode), SOC = 1 (8 bit mode)

SIC — (SI Control): SIC = 0 (16 bit mode), SIC = 1 (8 bit mode)

EI — (Enable Interrupt): EI = 0 (interrupts disabled), EI = 1 (interrupts enabled)

P0/P1 (Ports 0 and 1): P0 and P1 directly control the state of output pins P0 and P1

INSTRUCTIONS

The SPI has 3 types of instructions all of which are one word, 23 bits long and execute in 250 ns.

A) Arithmetic/Move-Return (OP = 00/RT = 01)

	22 21	20 19 18 17 16 15	14	13 12	11 10 9	8	7 6 5 4	3 2 1 0
OP	0 0	P-SELECT / ALU	ASL	DP_L	DP_H·M	RPDCR	SRC	DST
RT	0 1	Same as OP instruction						

There are two instructions of this type, both of which are capable of executing all ALU functions listed in Table 2 on the value specified by the ALU input (i.e., P select field see Table 1).

Table 1. OP, RT

Mnemonic	P-Select Field D_{20}	D_{19}	ALU Input
RAM	0	0	RAM
IDB	0	1	*Internal Data Bus
M	1	0	M Register
N	1	1	N Register

*Any value on the on-chip data bus. Value may be selected from any of registers listed in Table 7 source register selections.

Table 2. OP, RT

Mnemonic	ALU Field D_{18}	D_{17}	D_{16}	D_{15}	ALU Function	Flag A / Flag B	Flags Affected SA1 / SB1	SA0 / SB0	CA / CB	ZA / ZB	OVA1 / OVB1	OVA0 / OVB0
NOP	0	0	0	0	No Operation		–	–	–	–	–	–
OR	0	0	0	1	OR		X	‡	Ø	‡	Ø	Ø
AND	0	0	1	0	AND		X	‡	Ø	‡	Ø	Ø
XOR	0	0	1	1	Exclusive OR		X	‡	Ø	‡	Ø	Ø
SUB	0	1	0	0	Subtract		‡	‡	‡	‡	‡	‡
ADD	0	1	0	1	ADD		‡	‡	‡	‡	‡	‡
SBB	0	1	1	0	Subtract with Borrow		‡	‡	‡	‡	‡	‡
ADC	0	1	1	1	Add with Carry		‡	‡	‡	‡	‡	‡
DEC	1	0	0	0	Decrement A_{CC}		‡	‡	‡	‡	‡	‡
INC	1	0	0	1	Increment A_{CC}		‡	‡	‡	‡	‡	‡
CMP	1	0	1	0	Complement A_{CC} (1's Complement)		X	‡	Ø	‡	Ø	Ø
SHR1	1	0	1	1	1-bit R-Shift		X	‡	‡	‡	Ø	Ø
SHL1	1	1	0	0	1-bit L-Shift		X	‡	‡	‡	Ø	Ø
SHL2	1	1	0	1	2-bit L-Shift		X	‡	Ø	‡	Ø	Ø
SHL4	1	1	1	0	4-bit L-Shift		X	‡	Ø	‡	Ø	Ø
XCHG	1	1	1	1	8-bit Exchange		X	‡	Ø	‡	Ø	Ø

Notes: ‡ May be affected, depending on the results
– Previous status can be held
Ø Reset
X Indefinite

Table 3. OP, RT

Mnemonic	ASL Field D_{14}	A_{CC} Selection
ACCA	0	A_{CC} A
ACCB	1	A_{CC} B

Table 4. OP, RT

Mnemonic	DP_L Field D_{13}	D_{12}	DP_3-DP_0
DPNOP	0	0	No Operation
DPINC	0	1	Increment DP_L
DPDEC	1	0	Decrement DP_L
DPCLR	1	1	Clear DP_L

Table 5. OP, RT

Mnemonic	DP_H-M Field D_{11}	D_{10}	D_9	Exclusive OR
M0	0	0	0	(DP_6 DP_5 DP_4) ∀ (0 0 0)
M1	0	0	1	DP_6 DP_5 DP_4 ∀ (0 0 1)
M2	0	1	0	DP_6 DP_5 DP_4 ∀ (0 1 0)
M3	0	1	1	DP_6 DP_5 DP_4 ∀ (0 1 1)
M4	1	0	0	DP_6 DP_5 DP_4 ∀ (1 0 0)
M5	1	0	1	DP_6 DP_5 DP_4 ∀ (1 0 1)
M6	1	1	0	DP_6 DP_5 DP_4 ∀ (1 1 0)
M7	1	1	1	DP_6 DP_5 DP_4 ∀ (1 1 1

Table 6. OP,RT

Mnemonic	RPDCR D_8	Operation
RPNOP	0	No Operation
RPDEC	1	Decrement RP

Besides the arithmetic functions these instructions can also modify (1) the RAM Data Pointer DP, (2) the Data ROM Pointer RP, and (3) move data along the on-chip data bus from a source register to a destination register (the possible source and destination registers are listed in Tables 7 and 8 respectively). The difference in the two instructions of this type is that one executes a subroutine or interrupt return at the end of the instruction cycle while the other does not.

Table 7. OP, RT

Mnemonic	SRC Field D_7	D_6	D_5	D_4	Specified Register
NON	0	0	0	0	NO Register
A	0	0	0	1	ACC A (Accumulator A)
B	0	0	1	0	ACC B (Accumulator B)
TR	0	0	1	1	TR Temporary Register
DP	0	1	0	0	DP Data Pointer
RP	0	1	0	1	RP ROM Pointer
RO	0	1	1	0	RO ROM Output Data
SGN	0	1	1	1	SGN Sign Register
DR	1	0	0	0	DR Data Register
DRNF	1	0	0	1	DR Data No Flag ①
SR	1	0	1	0	SR Status
SIM	1	0	1	1	SI Serial in MSB ②
SIL	1	1	0	0	SI Serial in LSB ③
K	1	1	0	1	K Register
L	1	1	1	0	L Register
MEM	1	1	1	1	RAM

Notes: ① DR to IDB RQM not set. IN DMA DRQ not set.
② First bit in goes to MSB, last bit to LSB.
③ First bit in goes to LSB, last bit to MSB (bit reversed).

Table 7 — List of Registers Specified by the Source Field (SRC)

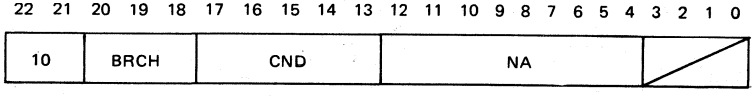
Table 8. OP, RT, LDI

Mnemonic	DST Field D_3	D_2	D_1	D_0	Specified Register
@NON	0	0	0	0	NO Register
@A	0	0	0	1	ACC A (Accumulator A)
@B	0	0	1	0	ACC B (Accumulator B)
@TR	0	0	1	1	TR Temporary Register
@DP	0	1	0	0	DP Data Pointer
@RP	0	1	0	1	RP ROM Pointer
@DR	0	1	1	0	DR Data Register
@SR	0	1	1	1	SR Status Register
@SOL	1	0	0	0	SO Serial Out LSB ①
@SOM	1	0	0	1	SO Serial Out MSB ②
@K	1	0	1	0	K (Mult)
@KLR	1	0	1	1	IDB → K ROM → L ③
@KLM	1	1	0	0	Hi RAM → K IDB → L ④
@L	1	1	0	1	L (Mult)
@NON	1	1	1	0	NO Register
@MEM	1	1	1	1	RAM

Notes: ① LSB is first bit out.
② MSB is first bit out.
③ Internal data bus to K and ROM to L register.
④ Contents of RAM address specified by $DP_6 = 1$ (i.e., 1, DP_5, DP_4, DP_0) is placed in K register. IDB is placed in L.

Table 8 — List of Registers Specified by the Destination Field (DST)

B) Jump/Call/Branch



JP Instruction Field Specifications

Three types of execution address modification instructions are accommodated by the processor and are listed in Table 9. All of the instructions, if unconditional or the specified condition is true, take their next program execution address from the Next Address field (NA), otherwise PC = PC + 1.

Table 9. Branch Field Selections (BRCH)

20	19	18	Instruction
1	0	0	Uncondition jump
1	0	1	Subroutine call
0	1	0	Condition jump

For the conditional jump instruction, the condition field specifies the jump condition. Table 10 lists all the instruction mnemonics of the J/C/B OP codes.

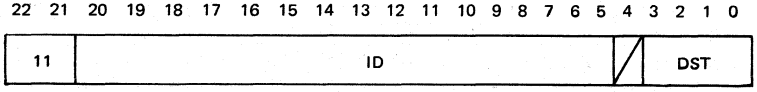
The SPI offers all the execution modification instructions necessary for efficient, data, I/O and arithmetic control.

Table 10. Condition Field Specifications

Mnemonic	BRCH/CND Fields								Conditions
	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	
JMP	1	0	0	0	0	0	0	0	No Condition
CALL	1	0	1	0	0	0	0	0	No Condition
JNCA	0	1	0	0	0	0	0	0	CA = 0
JCA	0	1	0	0	0	0	0	1	CA = 1
JNCB	0	1	0	0	0	0	1	0	CB = 0
JCB	0	1	0	0	0	0	1	1	CB = 1
JNZA	0	1	0	0	0	1	0	0	ZA = 0
JZA	0	1	0	0	0	1	0	1	ZA = 1
JNZB	0	1	0	0	0	1	1	0	ZB = 0
JZB	0	1	0	0	0	1	1	1	ZB = 1
JNOVA0	0	1	0	0	1	0	0	0	OVA0 = 0
JOVA0	0	1	0	0	1	0	0	1	OVA0 = 1
JNOVB0	0	1	0	0	1	0	1	0	OVB0 = 0
JOVB0	0	1	0	0	1	0	1	1	OVB0 = 1
JNOVA1	0	1	0	0	1	1	0	0	OVA1 = 0
JOVA1	0	1	0	0	1	1	0	1	OVA1 = 1
JNOVB1	0	1	0	0	1	1	1	0	OVB1 = 0
JOVB1	0	1	0	0	1	1	1	1	OVB1 = 1
JNSA0	0	1	0	1	0	0	0	0	SA0 = 0
JSA0	0	1	0	1	0	0	0	1	SA0 = 1
JNSB0	0	1	0	1	0	0	1	0	SB0 = 0
JSB0	0	1	0	1	0	0	1	1	SB0 = 1
JNSA1	0	1	0	1	0	1	0	0	SA1 = 0
JSA1	0	1	0	1	0	1	0	1	SA1 = 1
JNSB1	0	1	0	1	0	1	1	0	SB1 = 0
JSB1	0	1	0	1	0	1	1	1	SB1 = 1
JDPL0	0	1	0	1	1	0	0	0	$DP_L = 0$
JDPLF	0	1	0	1	1	0	0	1	DP_L = F (HEX)
JNSIAK	0	1	0	1	1	0	1	0	SI ACK = 0
JSIAK	0	1	0	1	1	0	1	1	SI ACK = 1
JNSOAK	0	1	0	1	1	1	0	0	SO ACK = 0
JSOAK	0	1	0	1	1	1	0	1	SO ACK = 1
JNRQM	0	1	0	1	1	1	1	0	RQM = 0
JRQM	0	1	0	1	1	1	1	1	RQM = 1

*BRCH or CND values not in this table are prohibited.

C) Load Data (LDI)



The Load Data instruction will take the 16-bit value contained in the Immediate Data field (ID) and place it in the location specified by the Destination field (DST) (see Table 8).

ABSOLUTE MAXIMUM RATINGS*

Voltage (V_{CC} Pin) . . . . . -0.5 to +7.0 Volts ①
Voltage, Any Input . . . . . -0.5 to +7.0 Volts ①
Voltage, Any Output . . . . . -0.5 to +7.0 Volts ①
Operating Temperature . . . . . -10°C to +70°C
Storage Temperature . . . . . -65°C to +150°C

Note: ① With respect to GND.

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10 ~ +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} +0.5	V	
CLK Low Voltage	$V_{\phi L}$	-0.5		0.45	V	
CLK High Voltage	$V_{\phi H}$	3.5		V_{CC} +0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{LIL}			−10	μA	V_{IN} = 0V
Input Load Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Output Float Leakage	I_{LOL}			−10	μA	V_{OUT} = 0.47V
Output Float Leakage	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Power Supply Current	I_{CC}		180	280	mA	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
CLK, SCK Input Capacitance	C_ϕ			20	pF	f_c = 1 MHz
Input Pin Capacitance	C_{IN}			10	pF	
Output Pin Capacitance	C_{OUT}			20	pF	

AC CHARACTERISTICS

$T_a = -10 \sim +70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
CLK Cycle Time	ϕCY	122		2000	ns	①
CLK Pulse Width	ϕD	60			ns	
CLK Rise Time	ϕR			10	ns	①
CLK Fall Time	ϕF			10	ns	①
Address Setup Time for $\overline{RD}$	t_{AR}	0			ns	
Address Hold Time for $\overline{RD}$	t_{RA}	0			ns	
$\overline{RD}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{RD}$	t_{RD}			150	ns	$C_L = 100$ pF
Read to Data Floating	t_{DF}	10		100	ns	$C_L = 100$ pF
Address Setup Time for $\overline{WR}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WW}	250			ns	
Data Setup Time for $\overline{WR}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WR}$	t_{WD}	0			ns	
$\overline{RD}$, $\overline{WR}$, Recovery Time	t_{RV}	250			ns	②
DRQ Delay	t_{AM}			150	ns	
$\overline{DACK}$ Delay Time	t_{DACK}	1			ϕD	②
SCK Cycle Time	t_{SCY}	480		DC	ns	
SCK Pulse Width	t_{SCK}	230			ns	
SCK Rise/Fall Time	t_{RSC}			20	ns	①
$\overline{SORQ}$ Delay	t_{DRQ}	30		150	ns	$C_L = 100$ pF
$\overline{SOEN}$ Setup Time	t_{SOC}	50			ns	
$\overline{SOEN}$ Hold Time	t_{CSO}	30			ns	
SO Delay from SCK = LOW	t_{DCK}			150	ns	
SO Delay from SCK with SORQ↑	t_{DZRQ}	20		300	ns	②
SO Delay from SCK	t_{DZSC}	20		300	ns	②
SO Delay from $\overline{SOEN}$	t_{DZE}	20		180	ns	②
$\overline{SOEN}$ to SO Floating	t_{HZE}	20		200	ns	②
SCK to SO Floating	t_{HZSC}	20		300	ns	②
SO Delay from SCK with SORQ↓	t_{HZRQ}	70		300	ns	②
$\overline{SIEN}$, SI Setup Time	t_{DC}	55			ns	②
$\overline{SIEN}$, SI Hold Time	t_{CD}	30			ns	
P_0, P_1 Delay	t_{DP}			ϕCY +150	ns	
RST Pulse Width	t_{RST}	4			ϕCY	
INT Pulse Width	t_{INT}	8			ϕCY	

Notes: ① Voltage at measuring point of timing 1.0V and 3.0V

② Voltage at measuring point of AC Timing

$V_{IL} = V_{OL} = 0.8V$

$V_{IH} = V_{OH} = 2.0V$

Input Waveform of AC Test (except CLK, SCK)

2.4	2.0	2.0
0.45	0.8	0.8

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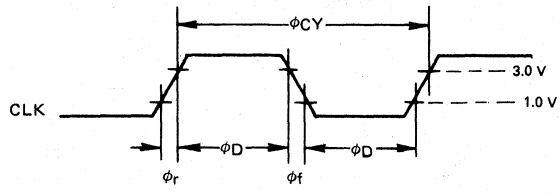
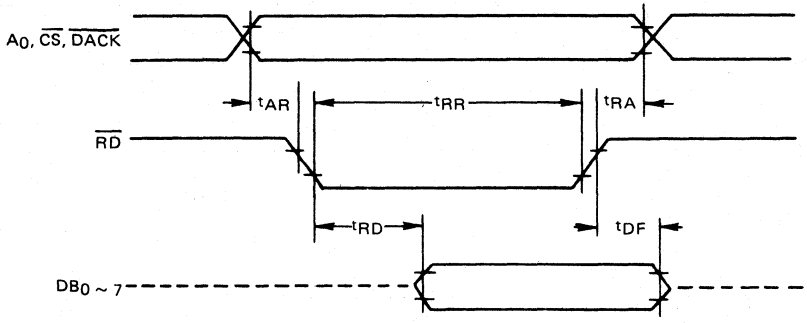
TIMING WAVEFORMS

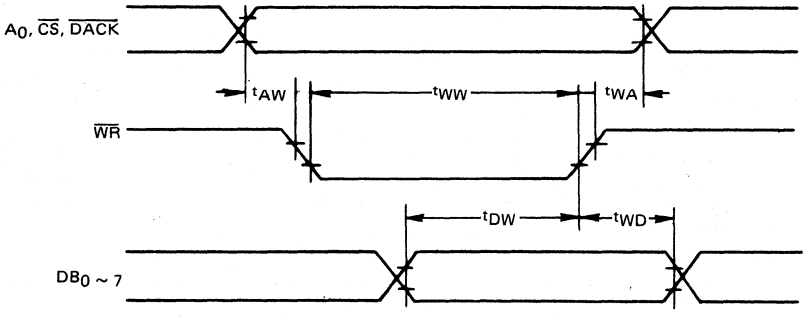
CLOCK



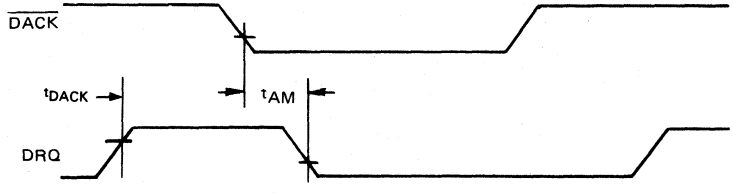
READ OPERATION



WRITE OPERATION

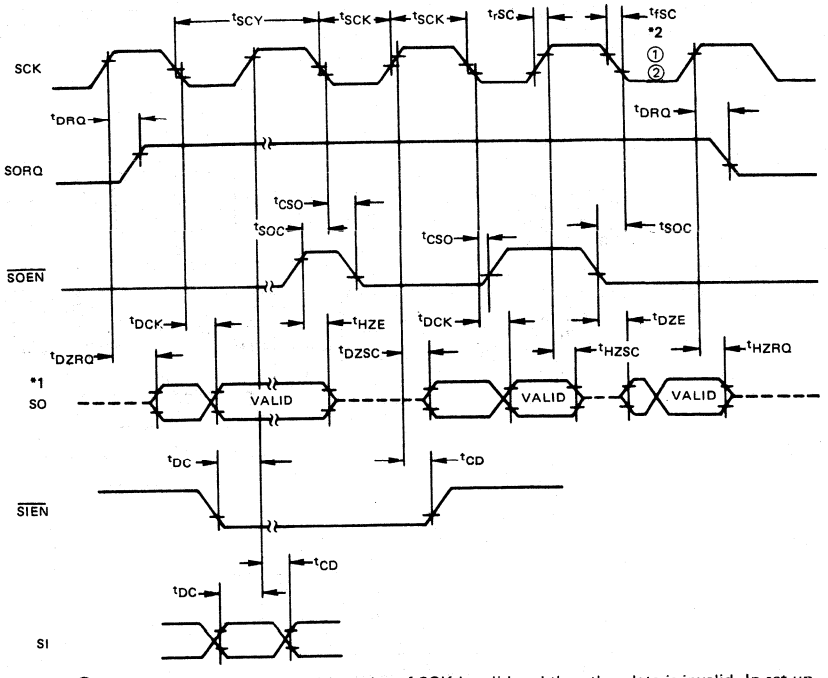


DMA OPERATION



TIMING WAVEFORMS (CON'T.)

SERIAL TIMING



Notes: ① For SO timing, the data at rising edge of SCK is valid and the other data is invalid. In set-up hold time of data for SCK, the most strict specifications are the following.

set-up = $t_{SCK} - t_{DCK}$

hold = t_{HZRQ}

② Voltage at measuring point of t_{rsc} and t_{fsc} for SCK timing

① 3.0V ② 1.0V

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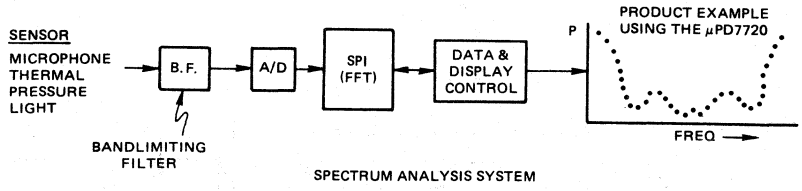
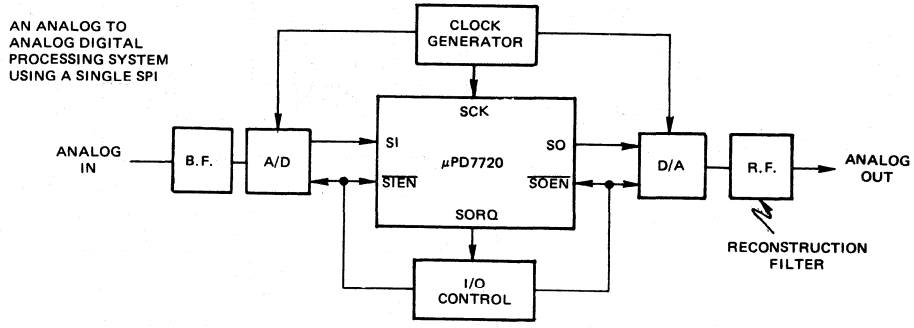
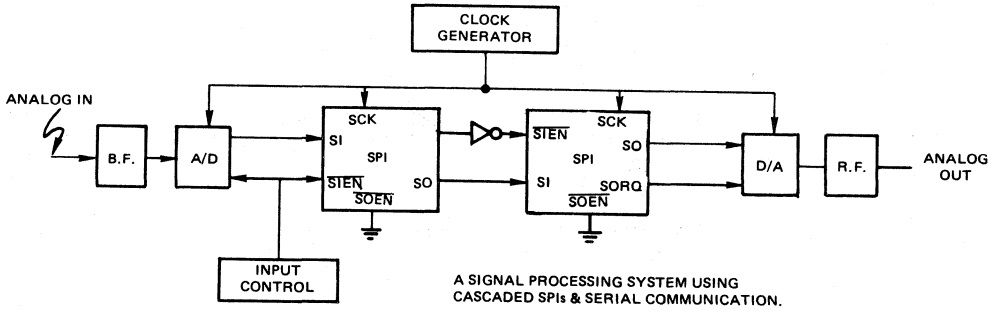
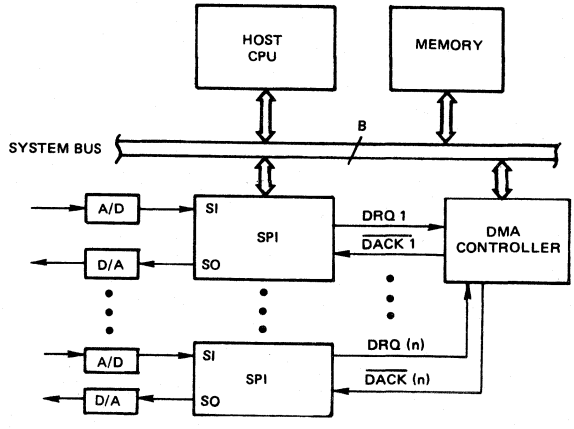


SPECTRUM ANALYSIS SYSTEM



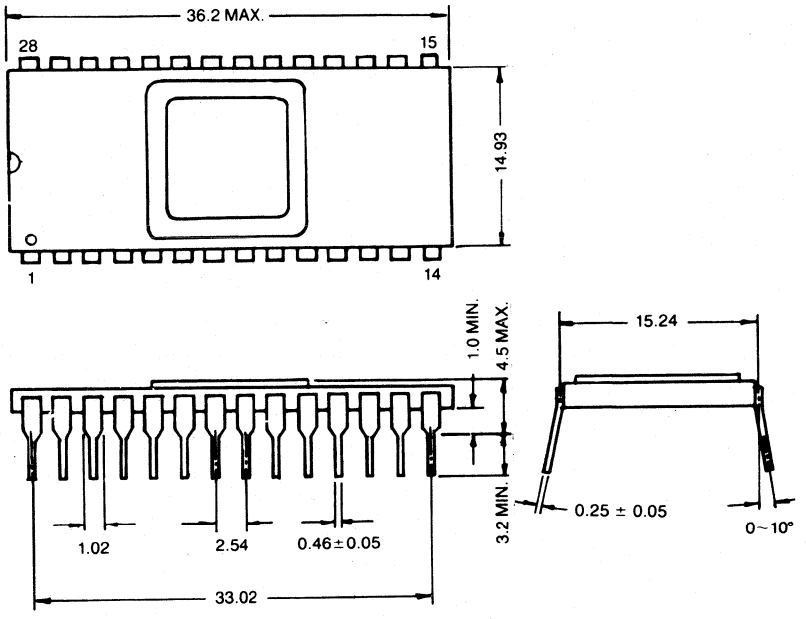


A SIGNAL PROCESSING SYSTEM USING CASCADED SPIs & SERIAL COMMUNICATION.



A SIGNAL PROCESSING SYSTEM USING SPI(s) AS A COMPLEX COMPUTER PERIPHERAL

PACKAGE DIMENSIONS



9

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

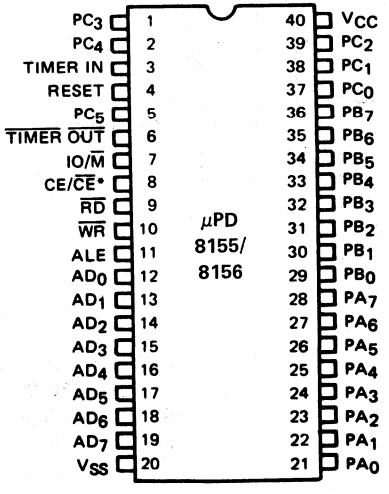
DESCRIPTION

The μPD8155 and μPD8156 are μPD8085A family components having 256 X 8 Static RAM, 3 programmable I/O ports and a programmable timer. They directly interface to the multiplexed μPD8085A bus with no external logic. The μPD8155 has an active low chip enable while the μPD8156 is active high.

FEATURES

- 256 X 8-Bit Static RAM
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Single Power Supplies: +5 Volt, ±10%
- Directly interfaces to the μPD8085A and μPD8085A-2
- Available in 40 Pin Plastic Packages

PIN CONFIGURATION



*μPD8155: $\overline{CE}$
μPD8156: CE

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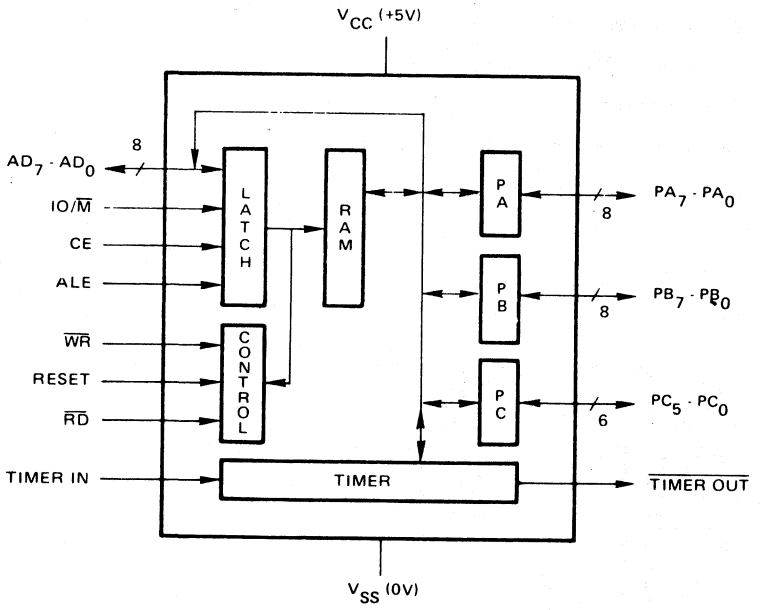
FUNCTIONAL DESCRIPTION

The μPD8155 and μPD8156 contain 2048 bits of Static RAM organized as 256 X 8. The 256 word memory location may be selected anywhere within the 64K memory space by using combinations of the upper 8 bits of address from the μPD8085A as a chip select.

The two general purpose 8-bit ports (PA and PB) may be programmed for input or output either in interrupt or status mode. The single 6-bit port (PC) may be used as control for PA and PB or general purpose input or output port. The μPD8155 and μPD8156 are programmed for their system personalities by writing into their Command/Status Registers (C/S) upon system initialization.

The timer is a single 14-bit down counter which is programmable for 4 modes of operation; see Timer Section.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	-0.5 to +7 Volts①
Power Dissipation	1.5 W

Note: ① **With Respect to Ground.**

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 5 39, 38, 37	PC_3, PC_4, PC_5 PC_2, PC_1, PC_0	Port C	Used as control for PA and PB or as a 6-bit general purpose port
3	TIMER IN	Timer Clock In	Clock input to the 14-bit binary down counter
4	RESET	Reset In	From μPD8085A system reset to set PA, PB, PC to the input mode
6	$\overline{\text{TIMER OUT}}$	Timer Counter Output	The output of the timer function
7	IO/$\overline{M}$	I/O or Memory Indicator	Selects whether operation to and from the chip is directed to the internal RAM or to I/O ports
8	CE/$\overline{CE}$	Chip Enable	Chip Enable Input. Active low for μPD8155 and active high for μPD8156
9	$\overline{RD}$	Read Strobe	Causes Data Read
10	$\overline{WR}$	Write Strobe	Causes Data Write
11	ALE	Address Low Enable	Latches low order address in when valid
12-19	$AD_0 - AD_7$	Low Address/Data	3-State address/data bus to interface directly to μPD8085A
20	V_{SS}	Ground	Ground Reference
21-28	$PA_0 - PA_7$	Port A	General Purpose I/O Port
29-36	$PB_0 - PB_7$	Port B	General Purpose I/O Port
40	V_{CC}	5 Volt Input	Power Supply

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 10\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage		V_{IL}	-0.5		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = 400 μA
Input Leakage		I_{IL}			±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Leakage Current		I_{LO}			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CC} Supply Current		I_{CC}			180	mA	
Chip Enable Leakage	μPD8155	I_{IL} (CE)			+100	μA	$V_{IN} = V_{CC}$ to 0V
	μPD8156	I_{IL}(CE)			-100	μA	

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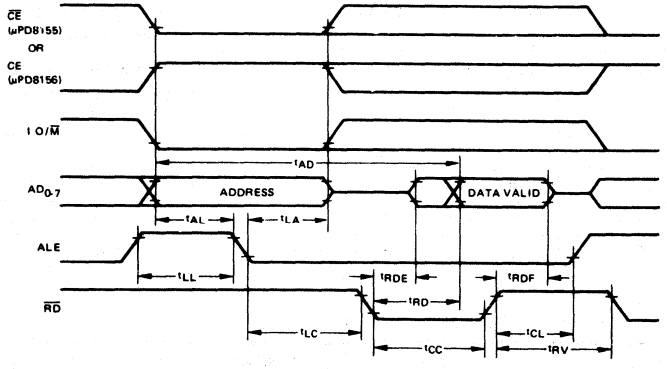
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 10%

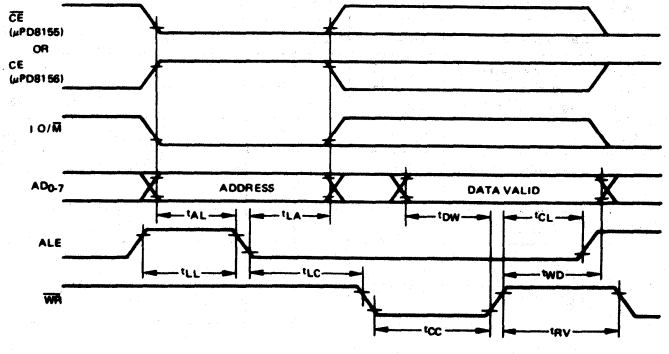
PARAMETER	SYMBOL	LIMITS 8155/8156 MIN	LIMITS 8155/8156 MAX	LIMITS 8155-2/8156-2 MIN	LIMITS 8155-2/8156-2 MAX	UNIT	TEST CONDITIONS
Address to Latch Set Up Time	t_{AL}	50		30		ns	150 pF Load
Address Hold Time after Latch	t_{LA}	80		30		ns	
Latch to READ/WRITE Control	t_{LC}	100		40		ns	
Valid Data Out Delay from READ Control	t_{RD}		170		140	ns	
Address Stable to Data Out Valid	t_{AD}		400		330	ns	
Latch Enable Width	t_{LL}	100		70		ns	
Data Bus Float After READ	t_{RDF}	0	100	0	80	ns	
READ/WRITE Control to Latch Enable	t_{CL}	20		10		ns	
READ/WRITE Control Width	t_{CC}	250		200		ns	
Data In to WRITE Set Up Time	t_{DW}	150		100		ns	
Data In Hold Time After WRITE	t_{WD}	0		0		ns	
Recovery Time Between Controls	t_{RV}	300		200		ns	
WRITE to Port Output	t_{WP}		400		300	ns	
Port Input Setup Time	t_{PR}	70		50		ns	
Port Input Hold Time	t_{RP}	50		10		ns	
Strobe to Buffer Full	t_{SBF}		400		300	ns	
Strobe Width	t_{SS}	200		150		ns	
READ to Buffer Empty	t_{RBE}		400		300	ns	
Strobe to INTR On	t_{SI}		400		300	ns	
READ to INTR Off	t_{RDI}		400		300	ns	
Port Setup Time to Strobe	t_{PSS}	50		0		ns	
Port Hold Time After Strobe	t_{PHS}	120		100		ns	
Strobe to Buffer Empty	t_{SBE}		400		300	ns	
WRITE to Buffer Full	t_{WBE}		400		300	ns	
WRITE to INTR Off	t_{WI}		400		300	ns	
TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low	t_{TL}		400		300	ns	
TIMER-IN to $\overline{\text{TIMER-OUT}}$ High	t_{TH}		400		300	ns	
Data Bus Enable from READ Control	t_{RDE}	10		10		ns	

TIMING WAVEFORMS

READ CYCLE

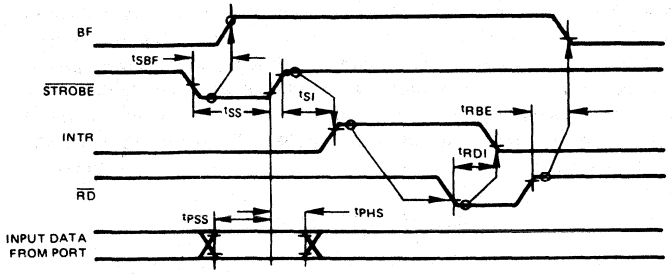


WRITE CYCLE

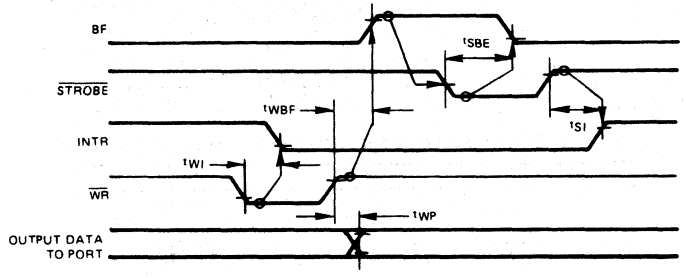


TIMING WAVEFORMS
(CONT.)

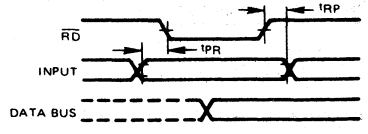
STROBED INPUT MODE



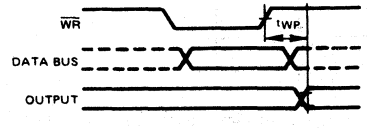
STROBED OUTPUT MODE



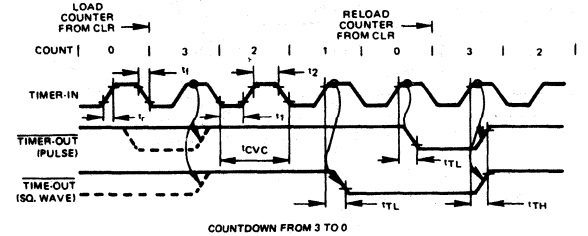
BASIC INPUT MODE



BASIC OUTPUT MODE



TIMER OUTPUT



COUNTDOWN FROM 3 TO 0

	μPD8155/8156	μPD8155-2/8156-2
t_{CYC}	320 ns MIN.	200 ns MIN.
t_{RISE} & t_{FALL}	30 ns MAX.	30 ns MAX.
t_1	80 ns MIN.	40 ns MIN.
t_2	120 ns MIN.	70 ns MIN.
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ LOW (TO BE DEFINED).	
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ HIGH (TO BE DEFINED).	

9

COMMAND STATUS REGISTER

The Command Status Register is an 8-bit register which must be programmed before the μPD8155/8156 may perform any useful functions. Its purpose is to define the mode of operation for the three ports and the timer. Programming of the device may be accomplished by writing to I/O address XXXXX000 (X denotes don't care) with a specific bit pattern. Reading of the Command Status Register can be accomplished by performing an I/O read operation at address XXXXX000. The pattern returned will be a 7-bit status report of PA, PB and the Timer. The bit patterns for the Command Status Register are defined as follows:

COMMAND STATUS WRITE

TM2	TM1	IEB	IEA	PC_2	PC_1	PB	PA

where:

TM2-TM1	Define Timer Mode
IEB	Enable Port B Interrupt
IEA	Enable Port A Interrupt
PC_2-PC_1	Define Port C Mode
PB/PA	Define Port B/A as In or Out ①

The Timer mode of operation is programmed as follows during command status write:

TM2	TM1	TIMER MODE
0	0	Don't Affect Timer Operation
0	1	Stop Timer Counting
1	0	Stop Counting after TC
1	1	Start Timer Operation

Interrupt enable status is programmed as follows:

IEB/IEA	INTERRUPT ENABLE PORT B/A
0	No
1	Yes

Port C may be placed in four possible modes of operation as outlined below. The modes are selected during command status write as follows:

PC_2	PC_1	PORT C MODE
0	0	ALT 1
0	1	ALT 3
1	0	ALT 4
1	1	ALT 2

The function of each pin of port C in the four possible modes is outlined as follows:

PIN	ALT 1	ALT 2	ALT 3 ②	ALT 4 ②
PC0	IN	OUT	A INTR	A INTR
PC1	IN	OUT	A BF	A BF
PC2	IN	OUT	A $\overline{STB}$	A $\overline{STB}$
PC3	IN	OUT	OUT	B INTR
PC4	IN	OUT	OUT	B BF
PC5	IN	OUT	OUT	B $\overline{STB}$

Notes: ① PB/PA Sets Port B/A Mode: 0 = Input; 1 = Output

② In ALT 3 and ALT 4 mode the control signals are initialized as follows:

CONTROL	INPUT	OUTPUT
$\overline{STB}$ (Input Strobe)	Input Control	Input Control
INTR (Interrupt Request)	Low	High
BF (Buffer Full)	Low	Low

COMMAND STATUS REGISTER (CONT.)

COMMAND STATUS READ

	TI	INTE B	B BF	INTR B	INTE A	A BF	INTR A

Where the function of each bit is as follows:

TI	Defines a Timer Interrupt. Latched high at TC and reset after reading the CS register or starting a new count, or reset.
INTE B/A	Defines If Port B/A Interrupt is Enabled. High = enabled.
B/A BF	Defines If Port B/A Buffer is Full-Input Mode or Empty-Output Mode. High = active.
INTR B/A	Port B/A Interrupt Request. High = active.

The programming address summary for the status, ports, and timer are as follows:

I/O Address	Number of Bits	Function
XXXXX000	8	Command Status
XXXXX001	8	PA
XXXXX010	8	PB
XXXXX011	6	PC
XXXXX100	8	Timer-Low
XXXXX101	8	Timer-High

TIMER

The Internal Timer is a 14-bit binary down counter capable of operating in 4 modes. Its desired mode of operation is programmable at any time during operation. Any TTL clock meeting timer in requirements (See AC Characteristics) may be used as a time base and fed to the timer input. The timer output may be looped around and cause an interrupt or used as I/O control. The operational modes are defined as follows and programmed along with the 6 high bits of timer data.

M2	M1	Operation
0	0	High at Start, Low During Second Half of Count
0	1	Square Wave (Period = Count Length, Auto Reload at TC)
1	0	Single Pulse at TC
1	1	Single Pulse at TC with Auto Reload

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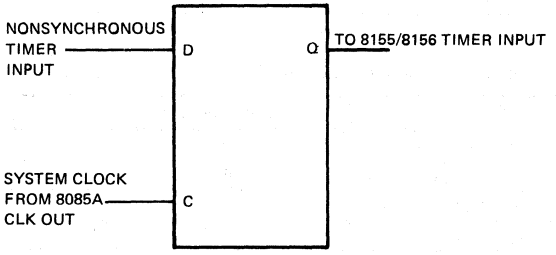
TIMER (CONT.)

Programming the timer requires two words to be written to the μPD8155/8156 at I/O address XXXXX100 and XXXXX101 for the low and high order bytes respectively. Valid count length must be between 2_H and $3FFF_H$. The bit assignments for the high and low programming words are as follows:

Word	Bit Pattern								I/O Address
High Byte	M_2	M_1	T13	T12	T11	T10	T9	T8	XXXXX101
Low Byte	T7	T6	T5	T4	T3	T2	T1	T0	XXXXX100

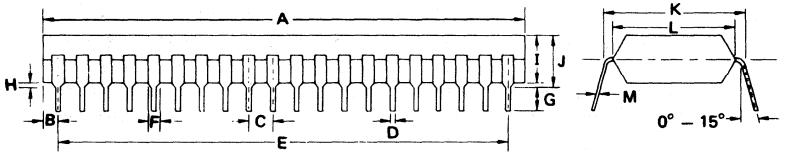
The control of the timer is performed by TM2 and TM1 of the Command Status Word.

Note that counting will be stopped by a hardware reset and a START command must be issued via the Command Status Register to begin counting. A new mode and/or count length can be loaded while counter is counting, but will not be used until a START command is issued.



When using the timer of the 8155/8156 care must be taken if the timer input is an external, nonsynchronous event. To sync this signal to the system clock the flip-flop shown should be used.

PACKAGE OUTLINE
μPD8155C
μPD8156C



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

EIGHT-BIT INPUT/OUTPUT PORT

DESCRIPTION

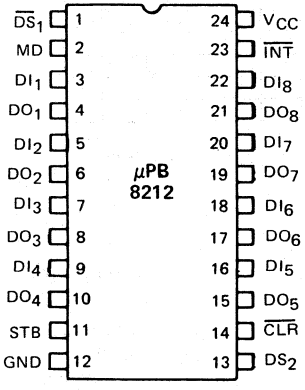
The μPB8212 input/output port consists of an 8-bit latch with three-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the control and generation of interrupts to the microprocessor.

The device is multimode in nature and can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

FEATURES

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current – 0.25 mA Max
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080A Processor
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in 24-pin Plastic and Cerdip Packages

PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_8$	Data In
$DO_1 - DO_8$	Data Out
$\overline{DS_1}$, DS_2	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt (Active Low)
$\overline{CLR}$	Clear (Active Low)

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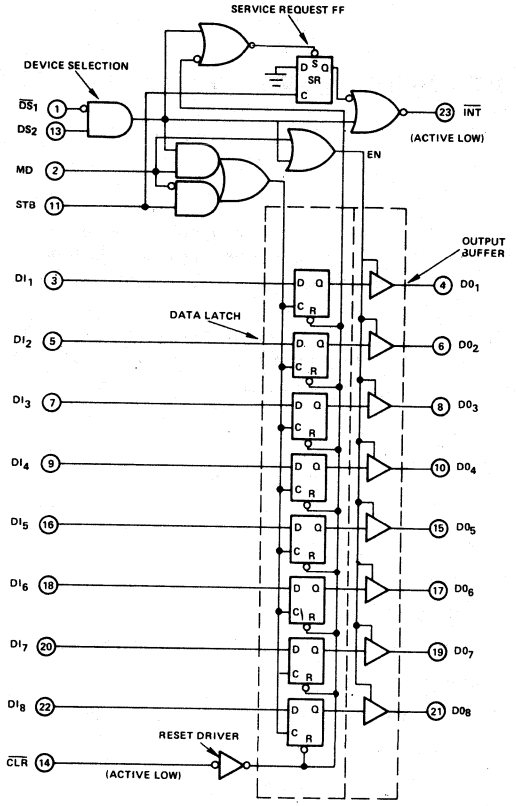
BLOCK DIAGRAM



STB	MD	$(\overline{DS_1} \cdot DS_2)$	DATA OUT EQUALS
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

$\overline{CLR}$	$(\overline{DS_1} \cdot DS_2)$	STB	SR ②	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	0	0	③	③
1	↓	0	1	1
1	0	↓	0	0
1	1	0	1	0
1	↓	↓	0	0

Notes: ① $\overline{CLR}$ resets data latch sets SR flip-flop. (No effect on output buffer)
② Internal SR flip-flop
③ Previous data remains

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	125 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current STB, DS_2, $\overline{CLR}$, $DI_1 - DI_8$ Inputs	IIL1		−0.25	mA	V_F = 0.45V
Input Load Current MD Input	IIL2		−0.75	mA	V_F = 0.45V
Input Load Current $\overline{DS_1}$ Input	IIL3		−1.0	mA	V_F = 0.45V
Input Leakage Current STB DS, $\overline{CLR}$, $DI_1 - DI_8$ Inputs	IIH1		10	μA	V_R = 5.25V
Input Leakage Current MD Input	IIH2		30	μA	V_R = 5.25V
Input Leakage Current $\overline{DS_1}$ Input	IIH3		40	μA	V_R = 5.25V
Input Forward Voltage Clamp	V_C		−1.0	V	I_C = −5 mA
Input "Low" Voltage	V_{IL}		0.85	V	
Input "High" Voltage	V_{IH}	2.0		V	
Output "Low" Voltage	V_{OL}		0.48	V	I_{OL} = 15 mA
Output "High" Voltage	V_{OH}	3.65		V	I_{OH} = −1 mA
Short Circuit Output Current	I_O5	−15	−75	mA	V_O = 0V V_{CC} = 5V
Output Leakage Current High Impedance State $DO_0 - DO_8$	I_O		20	μA	V_O = 0.45V/5.25V
Power Supply Current	I_{CC}		130	mA	

CAPACITANCE ①

T_a = 25°C; V_{CC} = +5V; V_{BIAS} = 2.5V; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		12	pF	$\overline{DS_1}$, MD
Input Capacitance	C_{IN}		9	pF	DS_2, $\overline{CLR}$, STB, $DI_1 - DI_8$
Output Capacitance	C_{OUT}		12	pF	$DO_1 - DO_8$

Note: ① This parameter is periodically sampled and not 100% tested

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Pulse Width	t_{pw}	30		ns	Input Pulse Amplitude = 2.5V
Data To Output Delay	t_{pd}		30	ns	
Write Enable To Output Delay	t_{we}		40	ns	Input Rise and Fall Times = 5 ns
Data Setup Time	t_{set}	15		ns	
Data Hold Time	t_h	20		ns	Between 1V and 2V Measurement made at 1.5V with 15 mA and 30 pF Test Load
Reset to Output Delay	t_r		40	ns	
Set To Output Delay	t_s		30	ns	
Output Enable/Disable Time	t_e/t_d		45	ns	①
Clear To Output Delay	t_c		55	ns	

Notes: ① R_1 = 300Ω/10KΩ; R_2 = 600Ω/1KΩ

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FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that compose the data latch are of a "D" type design. The output (Q) of the flip-flop follows the data input (D) while the clock input (C) is high. Latching occurs when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$).
(Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to three-state, non-inverting output buffers. These buffers have a common control line (EN); enabling the buffer to transmit the data from the outputs of the data latch (Q) or disabling the buffer, forcing the output into a high impedance state (three-state).

This high-impedance state allows the designer to connect the μPB8212 directly to the microprocessor bi-directional data bus.

Control Logic

The μPB8212 has four control inputs: $\overline{DS}_1$, DS_2, MD and STB. These inputs are employed to control device selection, data latching, output buffer state and the service request flip-flop.

$\overline{DS}_1$, DS_2 (Device Select)

These two inputs are employed for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

Service Request Flip-Flop (SR)

The (SR) flip-flop is employed to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output (Q) of the (SR) flip-flop is connected to an inverting input of a "NOR" gate. The other input of the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

MD (Mode)

This input is employed to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is in the output mode (high) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

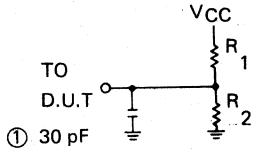
When MD is in the input mode (low) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

STB is employed as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request flip-flop (SR).

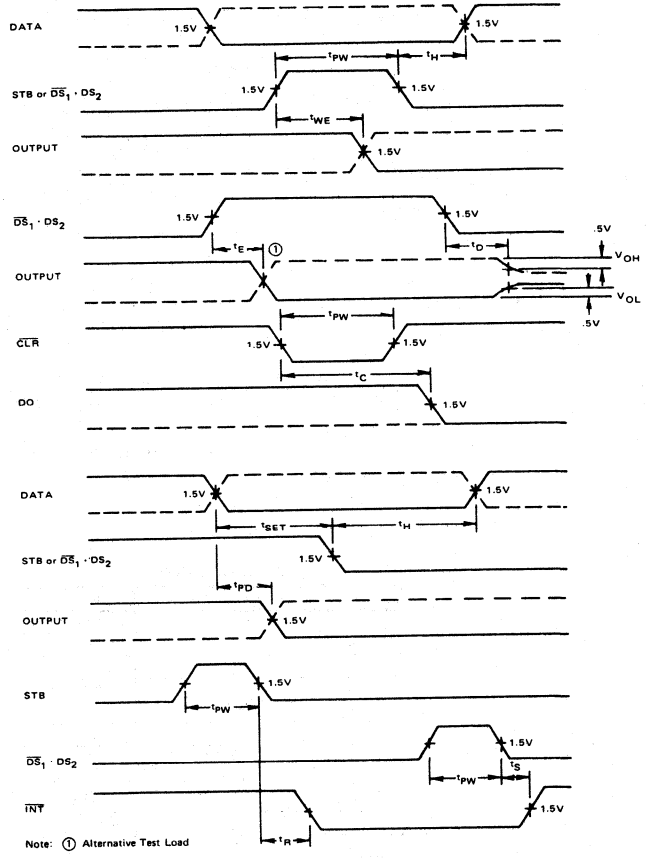
Note that the SR flip-flop triggers on the negative edge of STB which overrides $\overline{CLR}$.

TIMING WAVEFORMS

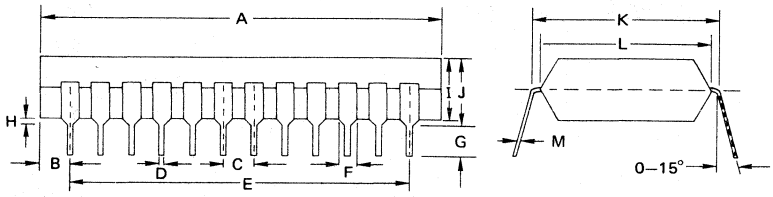


Note: ① Including Jig and Probe Capacitance

TEST CIRCUIT



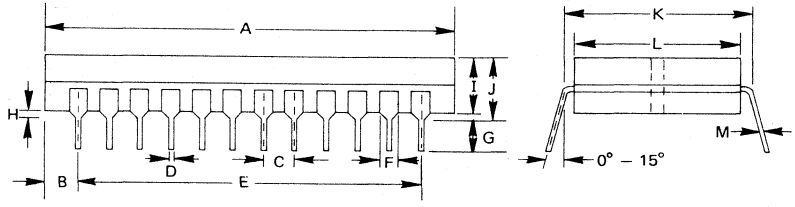
PACKAGE OUTLINE
μPB8212C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPB8212D'



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX	1.32 MAX
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.2 MAX
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

PRIORITY INTERRUPT CONTROLLER

DESCRIPTION

The μPB8214 is an eight-level priority interrupt controller. Designed to simplify interrupt driven microcomputer systems, the μPB8214 requires a single +5V power supply and is packaged in a 24 pin plastic Dual-in-line package.

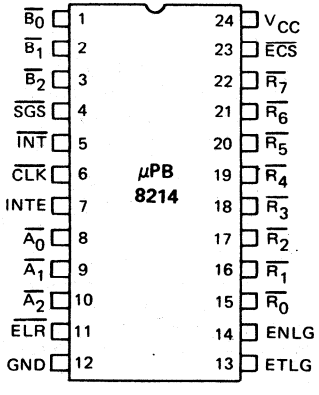
The μPB8214 accepts up to eight interrupts, determines which has the highest priority and then compares that priority with a software created current status register. If the incoming requires is of a higher priority than the interrupt currently being serviced, an interrupt request to the processor is generated. Vector information that identifies the interrupting device is also generated.

The interrupt structure of the microcomputer system can be expanded beyond eight interrupt levels by cascading μPB8214s. The μPB8214's interrupt and vector information outputs are open collector and control signals are provided to simplify expansion of the interrupt structure.

FEATURES

- Eight Priority Levels
- Current Status Register and Priority Comparator
- Easily Expanded Interrupt Structure
- Single +5 Volt Supply

PIN CONFIGURATION



PIN NAMES

Inputs:		
$\overline{R_0}$–$\overline{R_7}$	Request Levels ($\overline{R_7}$ Highest Priority)	
$\overline{B_0}$–$\overline{B_2}$	Current Status	
$\overline{SGS}$	Status Group Select	
$\overline{ECS}$	Enable Current Status	
INTE	Interrupt Enable	
$\overline{CLK}$	Clock (INT F-F)	
$\overline{ELR}$	Enable Level Read	
ETLG	Enable This Level Group	
Outputs:		
$\overline{A_0}$–$\overline{A_2}$	Request Levels	Open
$\overline{INT}$	Interrupt (Act. Low)	Collector
ENLG	Enable Next Level Group	

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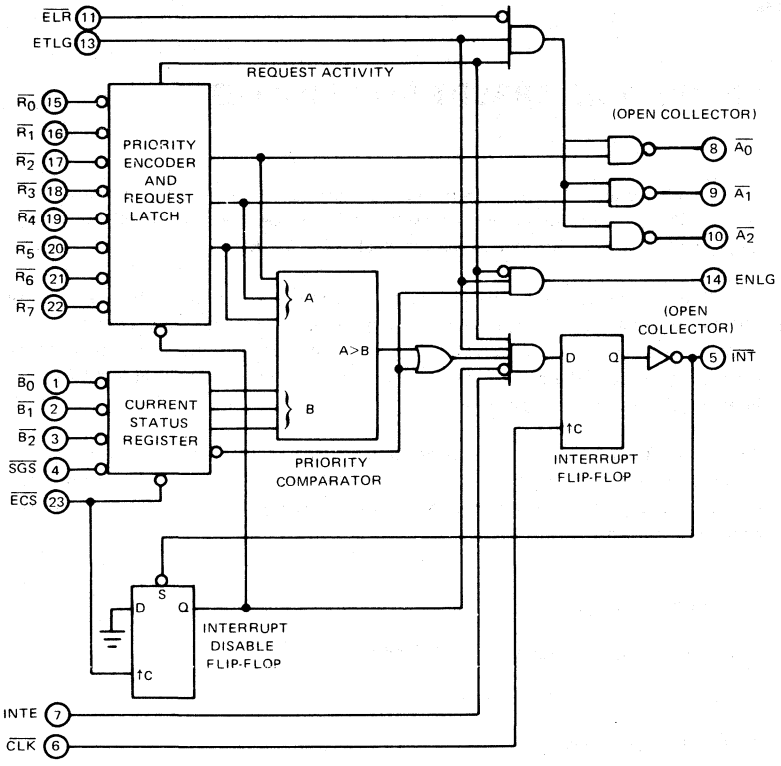
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output and Supply Voltages	-0.5 to +7 Volts
All Input Voltages	-1.0 to +5.5 Volts
Output Currents	100 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Clamp Voltage (all inputs)	V_C		-1.0	V	I_C=-5mA
Input Forward Current: ETLG input	I_F		-0.5	mA	V_F=0.45V
all other inputs	I_F		-0.25	mA	
Input Reverse Current: ETLG input	I_R		80	μA	V_R=5.25V
all other inputs	I_R		40	μA	
Input LOW Voltage: all inputs	V_{IL}		0.8	V	V_{CC}=5.0V
Input HIGH Voltage: all inputs	V_{IH}	2.0		V	V_{CC}=5.0V
Power Supply Current	I_{CC}		130	mA	①
Output LOW Voltage: all outputs	V_{OL}		.45	V	I_{OL}=10mA
Output HIGH Voltage: ENLG output	V_{OH}	2.4		V	I_{OH}=-1mA
Short Circuit Output Current: ENLG output	I_{OS}	-20	-55	mA	V_{OS}=0V, V_{CC}=5.0V
Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$-$\overline{A_2}$	I_{CEX}		100	μA	V_{CEX}=5.25V

CAPACITANCE ②

$T_a = 25°C$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		10	pF	V_{BIAS}=2.5V
Output Capacitance	C_{OUT}		12	pF	V_{CC}=5V f=1mHz

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
$\overline{CLK}$ Cycle Time	t_{CY}	80		ns	Input pulse amplitude: 2.5 Volts
$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	t_{PW}	25		ns	
INTE Setup Time to $\overline{CLK}$	t_{ISS}	16		ns	
INTE Hold Time after $\overline{CLK}$	t_{ISH}	20		ns	
ETLG Setup Time to $\overline{CLK}$	t_{ETCS} ③	25		ns	Input rise and fall times: 5 ns between 1 and 2 Volts
ETLG Hold Time After $\overline{CLK}$	t_{ETCH} ③	20		ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECCS} ③	80		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECCH} ④	0		ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECRS} ④	110		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECRH} ④	0			Output loading of 15 mA and 30 pF.
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECSS} ③	75		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECSH} ③	0		ns	
$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{CLK}$	t_{DCS} ③	70		ns	
$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{CLK}$	t_{DCH} ③	0		ns	Speed measurements taken at the 1.5 Volts levels.
$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{CLK}$	t_{RCS} ④	90		ns	
$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{CLK}$	t_{RCH} ④	0		ns	
$\overline{INT}$ Setup Time to $\overline{CLK}$	t_{ICS}	55		ns	
$\overline{CLK}$ to $\overline{INT}$ Propagation Delay	t_{CI}		25	ns	
$\overline{R_0}$-$\overline{R_7}$ Setup Time to $\overline{INT}$	t_{RIS} ⑤	10		ns	
$\overline{R_0}$-$\overline{R_7}$ Hold Time After $\overline{INT}$	t_{RIH} ⑤	35		ns	
$\overline{R_0}$-$\overline{R_7}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay	t_{RA}		100	ns	
$\overline{ELR}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay	t_{ELA}		55	ns	
$\overline{ECS}$ to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay	t_{ECA}		120	ns	
ETLG to $\overline{A_0}$-$\overline{A_2}$ Propagation Delay	t_{ETA}		70	ns	
$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Setup Time to $\overline{ECS}$	t_{DECS} ⑤	15		ns	
$\overline{SGS}$ and $\overline{B_0}$-$\overline{B_2}$ Hold Time After $\overline{ECS}$	t_{DECH} ⑤	15		ns	
$\overline{R_0}$-$\overline{R_7}$ to ENLG Propagation Delay	t_{REN}		70	ns	
ELTG to ENLG Propagation Delay	t_{ETEN}		25	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECRN}		90	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECSN}		55	ns	

Notes:
① $\overline{B_0}$-$\overline{B_2}$, $\overline{SGS}$, $\overline{CLK}$, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.
② This parameter is not 100% tested.
③ Required for proper operation if INTE is enabled during next clock pulse.
④ These times are not required for proper operation but for desired change in interrupt flip-flop.
⑤ Required for new request or status to be properly loaded.

FUNCTIONAL DESCRIPTION

General

The μPB8214 is an LSI device designed to simplify the circuitry required to implement an interrupt driven microcomputer system. Up to eight interrupting devices can be connected to a μPB8214, which will assign priority to incoming interrupt requests and accept the highest. It will also compare the priority of the highest incoming request with the priority of the interrupt being serviced. If the serviced interrupt has a higher priority, the incoming request will not be accepted.

A system with more than eight interrupting devices can be implemented by interconnecting additional μPB8214s. In order to facilitate this expansion, control signals are provided for cascading the controllers so that there is a priority established among the controllers. In addition, the interrupt and vector information outputs are open collector.

Priority Encoder and Request Latch

The priority encoder portion of the μPB8214 accepts up to eight active low interrupt requests ($\overline{R_0}$–$\overline{R_7}$). The circuit assigns priority to the incoming requests, with $\overline{R_7}$ having the highest priority and $\overline{R_0}$ the lowest. If two or more requests occur simultaneously, the μPB8214 accepts the one having the highest priority. Once an incoming interrupt request is accepted, it is stored by the request latch and a three-bit code is output. As shown in the following table, the outputs, ($\overline{A_0}$–$\overline{A_2}$) are the complement of the request level (modulo 8) and directly correspond to the bit pattern required to generate the one byte RESTART (RST) instructions recognized by an 8080A. Simultaneously with the $\overline{A_0}$–$\overline{A_2}$ outputs, a system interrupt request ($\overline{INT}$) is output by the μPB8214. It should be noted that incoming interrupt requests that are *not* accepted are not latched and must remain as an input to the μPB8214 in order to be serviced.

Interrupt Control Circuitry

The μPB8214 contains two flip-flops and several gates which determine whether an accepted interrupt request to the μPB8214 will generate a system interrupt to the 8080A. A condition gate drives the D input of the interrupt flip-flop whenever an interrupt request has been completely accepted. This requires that: the ETLG (Enable This Level Group) and INTE (Interrupt Enable) inputs to the μPB8214 are high; the $\overline{ELR}$ input is low; the incoming request must be of a higher priority than the contents of the current status register; and the μPB8214 must have been enabled to accept interrupt requests by the clearing of the interrupt disable flip-flop.

Once the condition gate drives the D input of the interrupt flip-flop high, a system interrupt ($\overline{INT}$) to the 8080A is generated on the next rising edge of the $\overline{CLK}$ input to the μPB8214. This $\overline{CLK}$ input is typically connected to the $\phi 2$ (TTL) output of an 8224 so that 8080A set-up time specifications are met. When $\overline{INT}$ is generated, it sets the interrupt disable flip-flop so that no additional system interrupts will be generated until it is reset. It is reset by driving $\overline{ECS}$ (Enable Current Status) low, thereby writing into the current status register.

It should be noted that the open collector $\overline{INT}$ output from the μPB8214 is active for only one clock period and thus must be externally latched for inputting to the 8080A. Also, because the $\overline{INT}$ output is open collector, when μPB8214's are cascaded, an $\overline{INT}$ output from any one will set all of the interrupt disable flip-flops in the array. Each μPB8214's interrupt disable flip-flop must then be cleared individually in order to generate subsequent system interrupts.

FUNCTIONAL DESCRIPTION (CONT.)

RESTART GENERATION TABLE

PRIORITY REQUEST		RST	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			1	1	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	1	1	1
LOWEST	$\overline{R_0}$	7	1	1	1	1	1	1	1	1
	$\overline{R_1}$	6	1	1	1	1	0	1	1	1
	$\overline{R_2}$	5	1	1	1	0	1	1	1	1
	$\overline{R_3}$	4	1	1	1	0	0	1	1	1
	$\overline{R_4}$	3	1	1	0	1	1	1	1	1
	$\overline{R_5}$	2	1	1	0	1	0	1	1	1
	$\overline{R_6}$	1	1	1	0	0	1	1	1	1
HIGHEST	$\overline{R_7}$	0*	1	1	0	0	0	1	1	1

*CAUTION: RST 0 will vector the program counter to location 0 (zero) and invoke the same routine as the "RESET" input to 8080A.

Current Status Register

The current status register is designed to prevent an incoming interrupt request from overriding the servicing of an interrupt with higher priority. Via software, the priority level of the interrupt being serviced by the microprocessor is written into the current status register on $\overline{B_0}$–$\overline{B_2}$. The bit pattern written should be the complement of the interrupt level.

The interrupt level currently being serviced is written into the current status register by driving $\overline{ECS}$ (Enable Current Status) low. The μPB8214 will only accept interrupts with a higher priority than the value contained by the current status register. Note that the programmer is free to use the current status register for other than as above. Other levels may be written into it. The comparison may be completely disabled by driving $\overline{SGS}$ (Status Group Select) low when $\overline{ECS}$ is driven low. This will cause the μPB8214 to accept incoming interrupts only on the basis of their priority to each other.

Priority Comparator

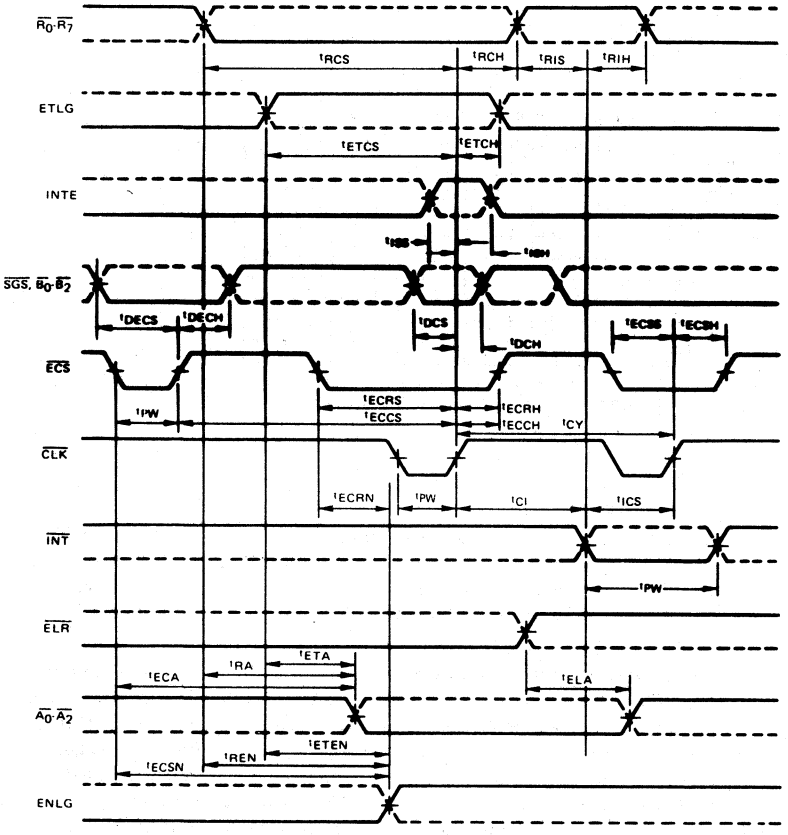
The priority comparator circuitry compares the level of the interrupt accepted by the priority encoder and request latch with the contents of the current status register. If the incoming request has a priority level higher than that of the current status register, the $\overline{INT}$ output is enabled. Note that this comparison can be disabled by loading the current status register with $\overline{SGS}$=0.

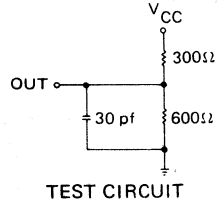
Expansion Control Signals

A microcomputer design may often require more than eight different interrupts. The μPB8214 is designed so that interrupt system expansion is easily performed via the use of three signals: ETLG (Enable This Level Group); ENLG (Enable Next Level Group); and $\overline{ELR}$ (Enable Level Read). A high input to ETLG indicates that the μPB8214 may accept an interrupt. In a typical system, the ENLG output from one μPB8214 is connected to the ETLG input of another μPB8214, etc. The ETLG of the μPB8214 with the highest priority is tied high. This configuration sets up priority among the cascaded μPB8214's. The ENLG output will be high for any device that does not have an interrupt pending, thereby allowing a device with lower priority to accept interrupts. The $\overline{ELR}$ input is basically a chip enable and allows hardware or software to selectively disable/enable individual μPB8214's. A low on the $\overline{ELR}$ input enables the device.

9

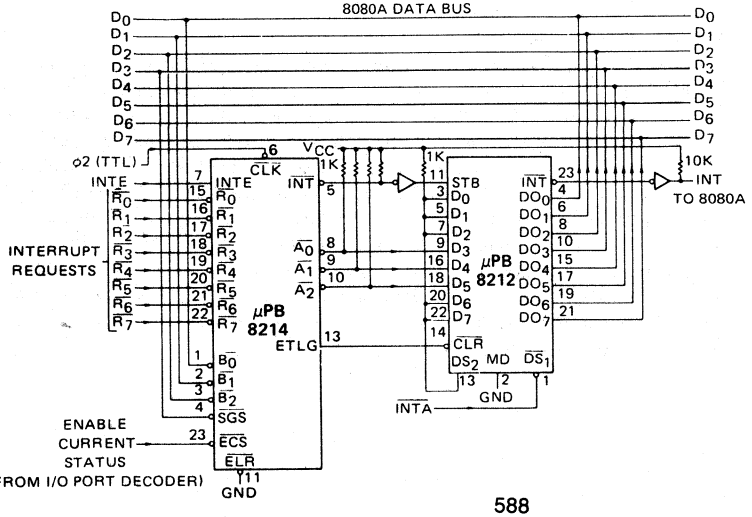
TIMING WAVEFORMS



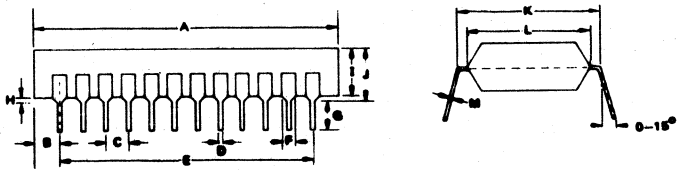


TEST CIRCUIT

TYPICAL μPB8214 CIRCUITRY



PACKAGE OUTLINE
μPB8214C



PLASTIC

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.28
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	3.2 MIN	0.125 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	0.25 ± 0.1	0.01 ± 0.004

9

4-BIT PARALLEL BIDIRECTIONAL BUS DRIVER

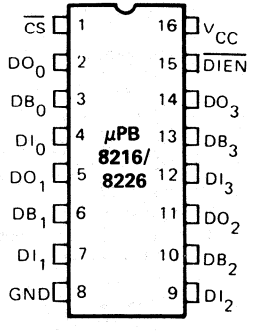
DESCRIPTION

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V (V_{OH}), and for high capacitance terminated bus structures, the DB outputs provide a high 55 mA (I_{OL}) capability.

FEATURES

- Data Bus Buffer Driver for μCOM-8 Microprocessor Family
- Low Input Load Current – 0.25 mA Maximum
- High Output Drive Capability for Driving System Data Bus
- 3.65V Output High Voltage for Direct Interface to μCOM-8 Microprocessor Family
- Three State Outputs
- Reduces System Package Count
- Available in 16-pin packages: Cerdip and Plastic

PIN CONFIGURATION



PIN NAMES

DB_0 - DB_3	Data Bus Bi Directional
DI_0 - DI_3	Data Input
DO_0 - DO_3	Data Output
$\overline{DIEN}$	Data in Enable Direction Control
$\overline{CS}$	Chip Select

9

FUNCTIONAL DESCRIPTION

Microprocessors like the μPD8080A are MOS devices and are generally capable of driving a single TTL load. This also applies to MOS memory devices. This type of drive is sufficient for small systems with a few components, but often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The μPD8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

Each buffered line of the four bit driver consists of two separate buffers. They are three state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this is used to interface to the system side components such as memories, I/O, etc. Its interface is directly TTL compatible and it has high drive (55 mA). For maximum flexibility on the other side of the driver the inputs and outputs are separate. They can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080A Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080A processor is achieved with an adequate amount of noise immunity (650 mV worst case).

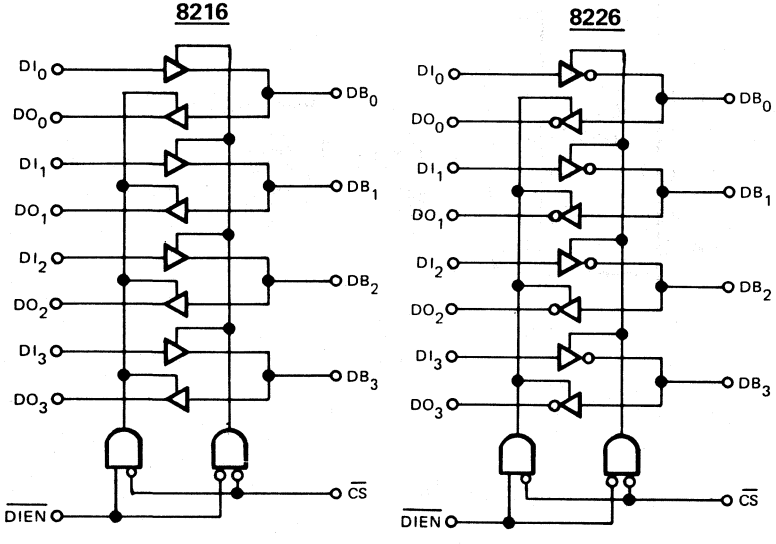
Control Gating $\overline{CS}$, $\overline{DIEN}$

The $\overline{CS}$ input is used for device selection. When $\overline{CS}$ is "high" the output drivers are all forced to their high-impedance state. When it is "low" the device is selected (enabled) and the data flow direction is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the data flow direction (see Block Diagrams for complete truth table). This directional control is accomplished by forcing one of the pair of buffers to its high impedance state. This allows the other to transmit its data. This is accomplished by a simple two gate circuit.

The μPB8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.

BLOCK DIAGRAMS



$\overline{DIEN}$	$\overline{CS}$	RESULT
0	0	DI → DB
1	0	DB → DO
0	1	High Impedance
1	1	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
All Output and Supply Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −1.0 to +5.5 Volts
Output Currents . . . . . 125 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current $\overline{DIEN}$, $\overline{CS}$		I_{F1}			−0.5	mA	$V_F = 0.45$
Input Load Current All Other Inputs		I_{F2}			−0.25	mA	$V_F = 0.45$
Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		I_{R1}			20	μA	$V_R = 5.25V$
Input Leakage Current DI Inputs		I_{R2}			10	μA	$V_R = 5.25V$
Input Forward Voltage Clamp		V_C			−1.0	V	$I_C = -5$ mA
Input "Low" Voltage		V_{IL}			0.95	V	
Input "High" Voltage		V_{IH}	2.0			V	
Output Leakage Current (3-State)	DO	I_O			20	μA	$V_O = 0.45/5.25V$
	DB	I_O			100		
Power Supply Current	8216	I_{CC}			130	mA	
	8226	I_{CC}			120	mA	
Output "Low" Voltage		V_{OL1}			0.48	V	DO Outputs $I_{OL} = 15$ mA DB Outputs $I_{OL} = 25$ mA
Output "Low" Voltage	8216	V_{OL2}			0.7	V	DB Outputs $I_{OL} = 55$ mA
	8226	V_{OL2}			0.7	V	DB Outputs $I_{OH} = 50$ mA
Output "High" Voltage		V_{OH1}	3.65			V	DO Outputs $I_{OH} = -1$ mA
Output "High" Voltage		V_{OH2}	2.4			V	DB Outputs $I_{OH} = -10$ mA
Output Short Circuit Current		I_{OS}	−15		−65	mA	DO Outputs $V_O = 0V$
		I_{OS}	−30		−120	mA	DB Outputs $V_{CC} = 5.0V$

Note: ① Typical values are for $T_a = 25°C$, $V_{CC} = 5.0V$.

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	$V_{BIAS} = 2.5V$
Output Capacitance	C_{OUT1}			10 ②	pF	$V_{CC} = 5V$
Output Capacitance	C_{OUT2}			18 ③	pF	$T_a = 25°C$ f = 1 MHz

Notes: ① This parameter is not 100% tested.
② DO Output.
③ DB Output.

9

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V±5%

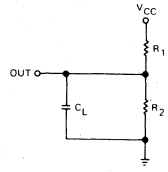
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input to Output Delay DO Outputs		t_{PD1}			25	ns	C_L = 30 pF, R_1 = 300Ω, R_2 = 600Ω ④
Input to Output Delay	8216	t_{PD2}			30	ns	C_L = 300 pF, R_1 = 90Ω,
DB Outputs	8226	t_{PD2}			25	ns	R_2 = 180Ω 4
Output Enable Time	8216	t_E			65	ns	② ④
	8226	t_E			54	ns	
Output Disable Time		t_D			35	ns	③ ④

Notes: ① Typical values are for T_a = 25°C, V_{CC} = 5.0V

② DO Outputs, C_L = 30 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 300 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

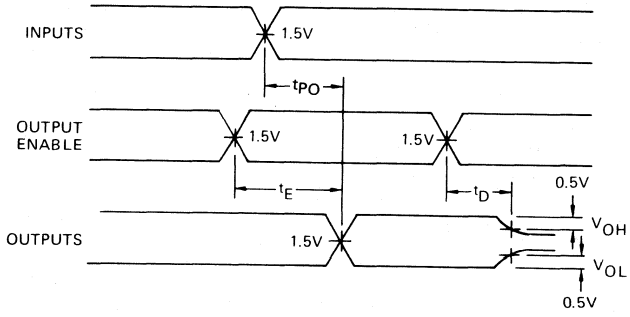
③ DO Outputs, C_L = 5 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 5 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

④ Input pulse amplitude: 2.5V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.



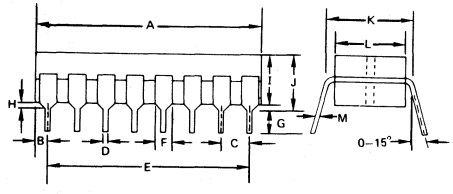
TEST CIRCUIT

TIMING WAVEFORMS



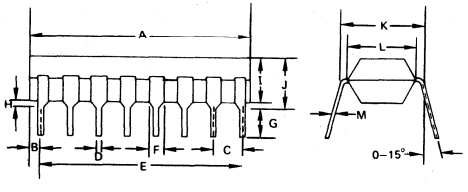
PACKAGE OUTLINE
μPB8216C/D
μPB8226C/D

Cerdip



ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	$0.0098^{+0.0039}_{0.0019}$

Plastic



ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	0.01

CLOCK GENERATOR AND DRIVER FOR 8080A PROCESSORS

DESCRIPTION

The μPB8224 is a single chip clock generator and driver for 8080A processors. The clock frequency is determined by a user specified crystal and is capable of meeting the timing requirements of the entire 8080A family of processors. MOS and TTL level clock outputs are generated.

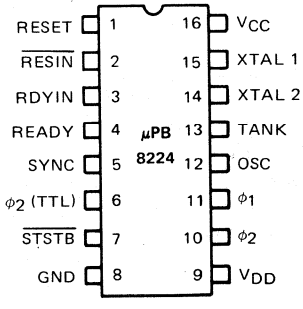
Additional logic circuitry of the μPB8224 provides signals for power-up reset, an advance status strobe and properly synchronizes the ready signal to the processor. This greatly reduces the number of chips needed for 8080A systems.

The μPB8224 is fabricated using NEC's Schottky bipolar process.

FEATURES

- Crystal Controlled Clocks
- Oscillator Output for External Timing
- MOS Level Clocks for 8080A Processor
- TTL Level Clock for DMA Activities
- Power-up Reset for 8080A Processor
- Ready Synchronization
- Advanced Status Strobe
- Reduces System Package Count
- Available in 16-pin Cerdip and Plastic Packages

PIN CONFIGURATION



PIN NAMES

$\overline{\text{RESIN}}$	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
$\overline{\text{STSTB}}$	Status STB Output
φ1	Processor Clocks
φ2	
XTAL 1	Crystal Connections
XTAL 2	
TANK	Used With Overtone Crystal
OSC	Oscillator Output
φ2 (TTL)	φ2 CLK (TTL Level)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

9

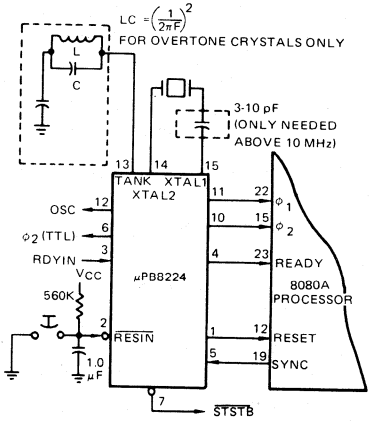
Clock Generator

The clock generator circuitry consists of a crystal controlled oscillator and a divide-by-nine counter. The crystal frequency is a function of the 8080A processor speed and is basically nine times the processor frequency, i.e.:

$$\text{Crystal frequency} = \frac{9}{t_{CY}}$$

where t_{CY} is the 8080A processor clock period.

A series resonant fundamental mode crystal is normally used and is connected across input pins XTAL1 and XTAL2. If an overtone mode crystal is used, an additional LC network, AC coupled to ground, must be connected to the TANK input of the μPB8224 as shown in the following figure.



The formula for the LC network is:

$$LC = \left(\frac{1}{2\pi F}\right)^2$$

where F is the desired frequency of oscillation.

The output of the oscillator is input to the divide-by-nine counter. It is also buffered and brought out on the OSC pin, allowing this stable, crystal controlled source to be used for derivation of other system timing signals. The divide-by-nine counter generates the two non-overlapping processor clocks, ϕ_1 and ϕ_2, which are buffered and at MOS levels, a TTL level ϕ_2 and internal timing signals.

The ϕ_1 and ϕ_2 high level outputs are generated in a 2-5-2 digital pattern, with ϕ_1 being high for two oscillator periods, ϕ_2 being high for five oscillator periods, and then neither being high for two oscillator periods. The TTL level ϕ_2,ϕ_2 (TTL), is normally used for DMA activities by gating the external device onto the 8080A bus once a Hold Acknowledge (HLDA) has been issued.

Additional Logic

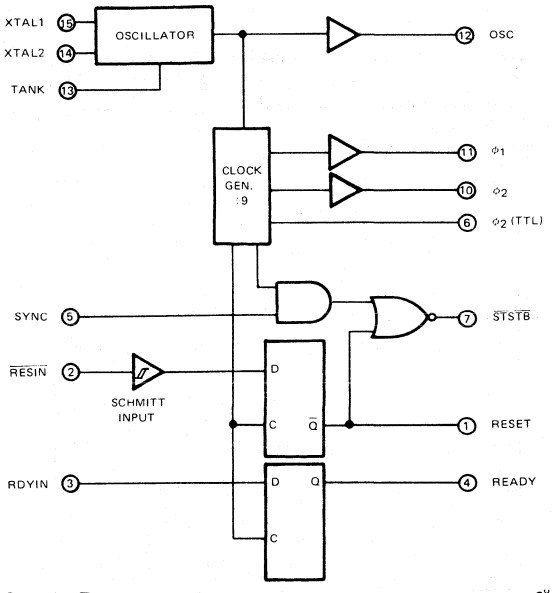
In addition to the clock generator circuitry, the μPB8224 contains additional logic to aid the system designer in the proper timing of several interface signals.

The $\overline{\text{STSTB}}$ signal indicates, at the earliest possible moment, when the status signals output from the 8080A processor are stable on the data bus. $\overline{\text{STSTB}}$ is designed to connect directly to the μPB8228 System Controller and automatically resets the μPB8228 during power-on Reset.

The $\overline{\text{RESIN}}$ input to the μPB8224 is used to automatically generate a RESET signal to the 8080A during power initialization. The slow rise of the power supply voltage in an external RC network is sensed by an internal Schmitt Trigger. The output of the Schmitt Trigger is gated to generate an 8080A compatible RESET. An active low manual switch may also be attached to the RC circuit for manual system reset.

The RDYIN input to the μPB8224 accepts an asynchronous "wait request" and generates a READY output to the 8080A that is fully synchronized to meet the 8080A timing requirements.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Output Voltages (TTL) . . . . . −0.5 to +7 Volts
All Output Voltages (MOS) . . . . . −0.5 to +13.5 Volts
All Input Voltages . . . . . −1.0 to +7 Volts
Supply Voltage V_{CC} . . . . . −0.5 to +7 Volts
Supply Voltage V_{DD} . . . . . −0.5 to +13.5 Volts
Output Currents . . . . . 100 mA

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Current Loading	I_F			−0.25	mA	V_F = 0.45V
Input Leakage Current	I_R			10	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C			−1.0	V	I_C = −5 mA
Input "Low" Voltage	V_{IL}			0.8	V	V_{CC} = 5.0V
Input "High" Voltage	V_{IH}	2.6			V	Reset Input
		2.0				All Other Inputs
RESIN Input Hysteresis	V_{IH}-V_{IL}	0.25			V	V_{CC} = 5.0V
Output "Low" Voltage	V_{OL}			0.45	V	(ϕ_1, ϕ_2), Ready, Reset, STSTB
						I_{OL} = 2.5 mA
				0.45	V	All Other Inputs
						I_{OL} = 15 mA
Output "High" Voltage	V_{OH}					
ϕ_1, ϕ_2		9.4			V	I_{OH} = −100 μA
READY, RESET		3.6			V	I_{OH} = −100 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Output Short Circuit Current (All Low Voltage Outputs Only)	I_{SC} ①	−10		−60	mA	V_O = 0V, V_{CC} = 5.0V
Power Supply Current	I_{CC}			115	mA	
Power Supply Current	I_{DD}			12	mA	

Note: ① Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CAPACITANCE①

T_a = 25°C; f = 1 MHz; V_{CC} = 5V; V_{DD} = 12V; V_{BIAS} = 2.5V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	

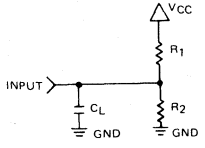
Note: ① This parameter is not 100% tested.

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

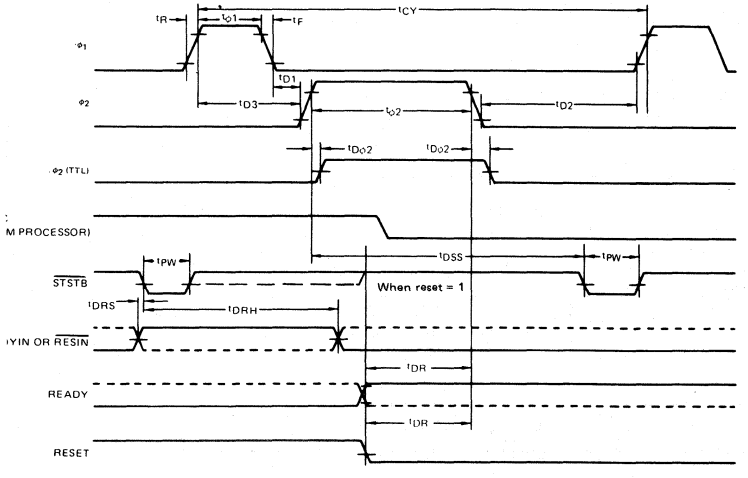
PARAMETER	SYMBOL	LIMITS ①			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
ϕ_1 Pulse Width	$t_{\phi 1}$	$\frac{2t_{CY}}{9}$ −20 ns			ns	C_L = 20 pF to 50 pF
ϕ_2 Pulse Width	$t_{\phi 2}$	$\frac{5t_{CY}}{9}$ −35 ns				
ϕ_1 to ϕ_2 Delay	t_{D1}	0				
ϕ_2 to ϕ_1 Delay	t_{D2}	$\frac{2t_{CY}}{9}$ −14 ns				
ϕ_1 to ϕ_2 Delay	t_{D3}	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +20 ns		
ϕ_1 and ϕ_2 Rise Time	t_R			20		
ϕ_1 and ϕ_2 Fall Time	t_F			20		
ϕ_2 to ϕ_2 (TTL) Delay	$t_{D\phi 2}$	−5		+15	ns	ϕ_2 TTL, CL = 30 pF R_1 = 300Ω R_2 = 600Ω
ϕ_2 to $\overline{STSTB}$ Delay	t_{DSS}	$\frac{6t_{CY}}{9}$ −30 ns		$\frac{6t_{CY}}{9}$	ns	$\overline{STSTB}$, CL = 15 pF R_1 = 2K R_2 = 4K
$\overline{STSTB}$ Pulse Width	t_{PW}	$\frac{t_{CY}}{9}$ −15 ns			ns	
RDYIN Setup Time to $\overline{STSTB}$	t_{DRS}	50 ns − $\frac{4t_{CY}}{9}$				
RDYIN Hold Time After $\overline{STSB}$	t_{DRH}	$\frac{4t_{CY}}{9}$				
READY or RESET to ϕ_2 Delay	t_{DR}	$\frac{4t_{CY}}{9}$ −25 ns			ns	Ready and Reset CL = 10 pF R_1 = 2K R_2 = 4K
Crystal Frequency	f_{CLK}		$\frac{9}{t_{CY}}$		MHz	
Maximum Oscillating Frequency	f_{MAX}			27	MHz	

Note: ① t_{CY} represents the processor clock period



TEST CIRCUIT

TIMING WAVEFORMS



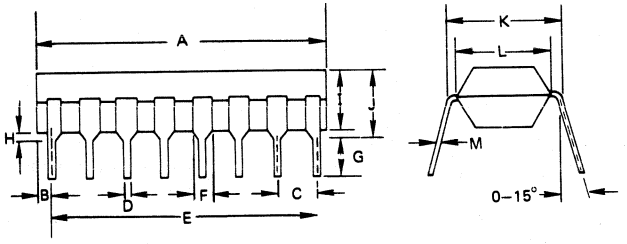
Voltage Measurement Points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

CRYSTAL REQUIREMENTS

Tolerance	0.005% at 0°C–70°C
Resonance	Series (Fundamental) ①
Load Capacitance	20-35 pF
Equivalent Resistance	75-20 ohms
Power Dissipation (Min)	4 mW

Note: ① With tank circuit use 3rd overtone mode.

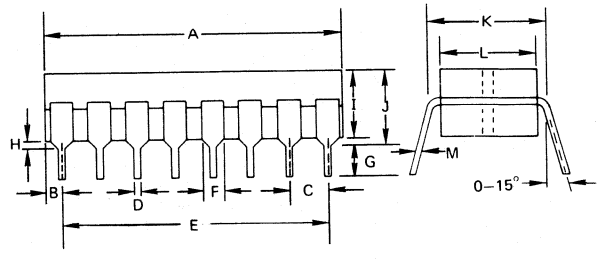
PACKAGE OUTLINE μPB8224C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN.	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

μPB8224D



(CERDIP)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.8	0.27
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

9

8080A SYSTEM CONTROLLER AND BUS DRIVER

DESCRIPTION

The μPB8228 is a single chip controller and bus driver for 8080A based systems. All the required interface signals necessary to connect RAM, ROM and I/O components to a μPD8080A are generated.

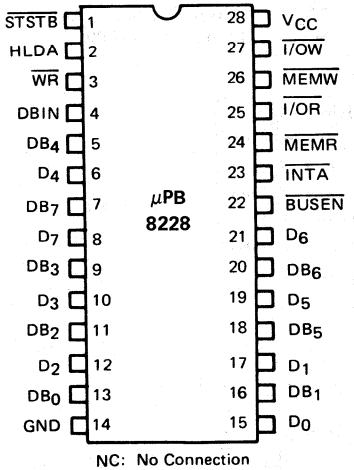
The μPB8228 provides a bi-directional three-state bus driver for high TTL fan-out and isolation of the processor data bus from the system data bus for increased noise immunity.

The system controller portion of the μPB8228 consists of a status latch for definition of processor machine cycles and a gating array to decode this information for direct interface to system components. The controller can enable gating of a multi-byte interrupt onto the data bus or can automatically insert a RESTART 7 onto the data bus without any additional components.

FEATURES

- System Controller for 8080A Systems
- Bi-Directional Data Bus for Processor Isolation
- 3.60V Output High Voltage for Direct Interface to 8080A Processor
- Three State Outputs on System Data Bus
- Enables Use of Multi-Byte Interrupt Instructions
- Generates RST 7 Interrupt Instruction
- μPB8228 for Small Memory Systems
- Reduces System Package Count
- Schottky Bipolar Technology

PIN CONFIGURATION



NC: No Connection

PIN NAMES

$D_7 - D_0$	Data Bus (Processor Side)
$DB_7 - DB_0$	Data Bus (System Side)
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
DBIN	DBIN (From Processor)
$\overline{INTA}$	Interrupt Acknowledge
HLDA	HLDA (From Processor)
$\overline{WR}$	WR (From Processor)
$\overline{BUSEN}$	Bus Enable Input
$\overline{STSTB}$	Status Strobe (From μPB8224)
V_{CC}	+5V
GND	0 Volts

9

μPB8228

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver

The eight bit, bi-directional bus driver provides buffering between the processor data bus and the system data bus. On the processor side, the μPB8228 exceeds the minimum input voltage requirements (3.0V) of the μPD8080A. On the system side, the driver is capable of adequate drive current (10 mA) for connection of a large number of memory and I/O devices to the bus. Single flow in the bus driver is controlled by the gating array and its outputs can be forced into a high impedance state by use of the $\overline{\text{BUSEN}}$ input.

Status Latch

The Status Latch in the μPB8228 stores the status information placed on the data bus by the 8080A at the beginning of each machine cycle. The information is latched when $\overline{\text{STSTB}}$ goes low and is then decoded by the gating array for the generation of control signals.

Gating Array

The Gating Array generates "active low" control signals for direct interfacing to system components by gating the contents of the status latch with control signals from the 8080A.

$\overline{\text{MEM/R}}$, $\overline{\text{I/OR}}$ and $\overline{\text{INTA}}$ are generated by gating the DBIN signal from the processor with the contents of the status latch. $\overline{\text{I/OR}}$ is used to enable an I/O input onto the system data bus. $\overline{\text{MEM/R}}$ is used to enable a memory input.

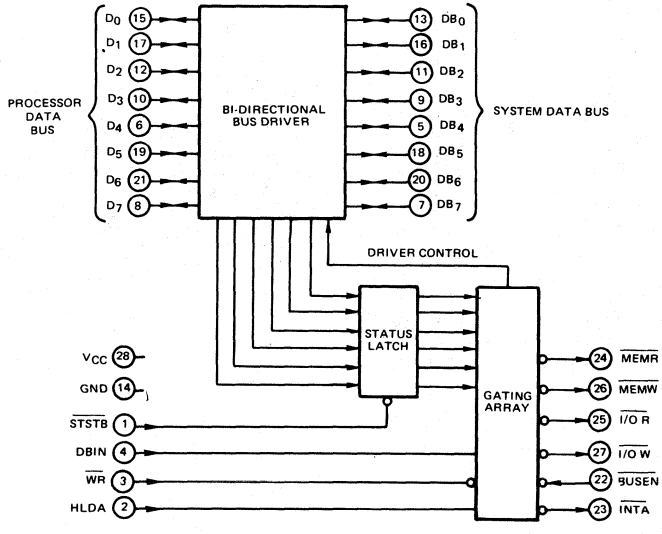
$\overline{\text{INTA}}$ is normally used to gate an interrupt instruction onto the system data bus. When used with the μPD8080A processor, the μPB8228 will decode an interrupt acknowledge status word during all three machine cycles for a multi-byte interrupt instruction. For 8080A type processors that do not generate an interrupt acknowledge status word during the second and third machine cycles of a multi-byte interrupt instruction, the μPB8228 will internally generate an $\overline{\text{INTA}}$ pulse for those machine cycles.

The μPB8228 also provides the designer the ability to place a single interrupt instruction onto the bus without adding additional components. By connecting the +12 volt supply to the $\overline{\text{INTA}}$ output (pin 23) of the μPB8228 through a 1 K ohm series resistor, RESTART 7 will be gated onto the processor data bus when DBIN is active during an interrupt acknowledge machine cycle.

$\overline{\text{MEM/W}}$ and $\overline{\text{I/OW}}$ are generated by gating the $\overline{\text{WR}}$ signal from the processor with the contents of the status latch. $\overline{\text{I/OW}}$ indicates that an output port write is about to occur. $\overline{\text{MEM/W}}$ indicates that a memory write will occur.

The data bus output buffers and control signal buffers can be asynchronously forced into a high impedance state by placing a high on the $\overline{\text{BUSEN}}$ pin of the μPB8228. Normal operation is performed with $\overline{\text{BUSEN}}$ low.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +7.0 Volts
Output Currents	100 mA

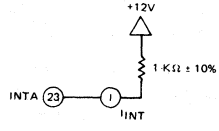
T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Clamp Voltage, All Inputs	V_C			−1.0	V	V_{CC} = 4.75V; I_{CC} = −5 mA
Input Load Current, $\overline{STSTB}$	I_F			500	μA	V_{CC} = 5.25V V_F = 0.45V
D_2 and D_6				750	μA	
D_0, D_1, D_4, D_5, and D_7				250	μA	
All Other Inputs				250	μA	
Input Leakage Current, $\overline{STSTB}$	I_R			100	μA	V_{CC} = 5.25V V_R = 5.0V
DB_0 through DB_7				20	μA	
All Other Inputs				100	μA	
Input Threshold Voltage, All Inputs	V_{TH}	0.8		2.0	V	V_{CC} = 5V
Power Supply Current	I_{CC}			190	mA	V_{CC} = 5.25V
Output Low Voltage, D_0 through D_7	V_{OL}			0.45	V	V_{CC} = 4.75V; I_{OL} = 2 mA
All Other Outputs				0.48	V	I_{OL} = 10 mA
Output High Voltage, D_0 through D_7	V_{OH}	3.6			V	V_{CC} = 4.75V; I_{OH} = −10 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Short Circuit Current, All Outputs	I_{OS}	15		90	mA	V_{CC} = 5V
Off State Output Current, All Control Outputs	$I_{O(off)}$			100	μA	V_{CC} = 5.25V; V_O = 5.0V
				−100	μA	V_O = 0.45V
INTA Current	I_{INT}			5	mA	(See Figure below)



INTA TEST CIRCUIT

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			12	pF	V_{BIAS} = 2.5V, V_{CC} = 5.0V, f = 1 MHz
Output Capacitance Control Signals	C_{OUT}			15	pF	
I/O Capacitance (D or DB)	$C_{I/O}$			15	pF	

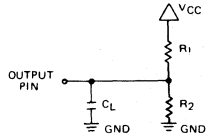
NOTE: This parameter is not 100% tested.

AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

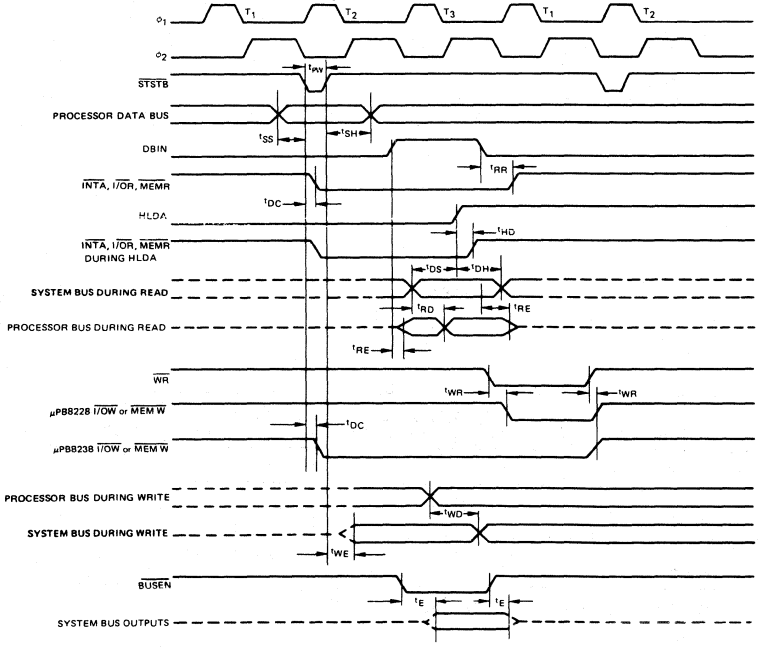
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Width of Status Strobe	t_{PW}	22			ns	
Setup Time, Status Inputs D_0-D_7	t_{SS}	8			ns	
Hold Time, Status Inputs D_0-D_7	t_{SH}	5			ns	
Delay from $\overline{STSTB}$ to any Control Signal	t_{DC}	20		60	ns	C_L = 100 pF
Delay from DBIN to Control Outputs	t_{RR}			30	ns	C_L = 100 pF
Delay from DBIN to Enable/ Disable 8080A Bus	t_{RE}			45	ns	C_L = 25 pF
Delay from System Bus to 8080A Bus during Read	t_{RD}			30	ns	C_L = 25 pF
Delay from $\overline{WR}$ to Control Outputs	t_{WR}	5		45	ns	C_L = 100 pF
Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$	t_{WE}			30	ns	C_L = 100 pF
Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	t_{WD}	5		40	ns	C_L = 100 pF
Delay from $\overline{\text{System Bus Enable}}$ to System Bus DB_0-DB_7	t_E			30	ns	C_L = 100 pF
HLDA to Read Status Outputs	t_{HD}			25	ns	
Setup Time, System Bus Inputs to HLDA	t_{DS}	10			ns	
Hold Time, System Bus Inputs to HLDA	t_{DH}	20			ns	C_L = 100 pF

For D_0-D_7: R_1 = 4 KΩ, R_2 = ∞Ω, C_L = 25 pF. For all other outputs: R_1 = 500Ω, R_2 = 1 KΩ, C_L = 100 pF.



TEST CIRCUIT

TIMING WAVEFORMS

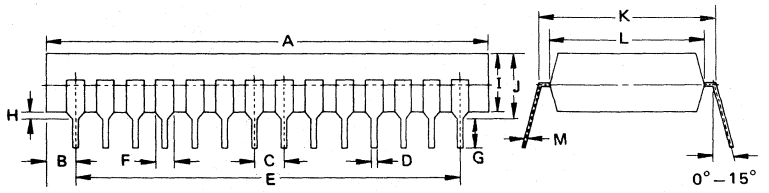


VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

STATUS WORD CHART

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE (M_1)	INT. ACK. (M_2, M_3)	HALT ACKNOWLEDGE	
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	
D_0	INTA	0	0	0	0	0	0	0	1	0	1	μPD8080A OUTPUT
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	1	1	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	
D_5	M_1	1	0	0	0	0	0	0	1	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	
D_7	MEMR	1	1	0	1	0	0	0	0	1	0	
24	$\overline{MEMR}$	0	0	1	0	1	1	1	1	1	1	μPB8228 OUTPUT
26	$\overline{MEMW}$	1	1	0	1	0	1	1	1	1	1	
25	$\overline{I/OR}$	1	1	1	1	1	0	1	1	1	1	
27	$\overline{I/OW}$	1	1	1	1	1	1	0	1	1	1	
23	$\overline{INTA}$	1	1	1	1	1	1	1	0	0	1	
PIN NO.		SIGNAL STATUS										
		μPB8228 CONTROL SIGNALS										

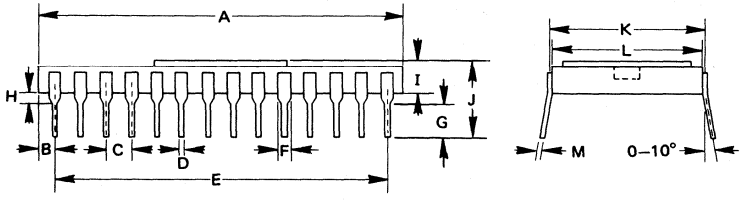
PACKAGE OUTLINE
μPB8228C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX	1.496 MAX
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

μPB8228D



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	36.2 MAX	1.43
B	1.59 MAX	0.06
C	2.54	0.1
D	0.46 ± 0.05	0.02 ± 0.004
E	33.02	1.3
F	1.02	0.04
G	3.2 MIN	0.13
H	1.0	0.04
I	3.5	0.14
J	4.5	0.18
K	15.24	0.6
L	14.93	0.59
M	0.25 ± 0.05	0.01 ± 0.002

μPD8237A-5
HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER

Description

The μPD8237A-5 High Performance DMA Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory. Memory-to-memory transfer capability is also provided. The μPD8237A-5 offers a wide variety of programmable control features to enhance data throughput and allow dynamic reconfiguration under program control.

The μPD8237A-5 is designed to be used with an external 8-bit address register such as the 8282. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

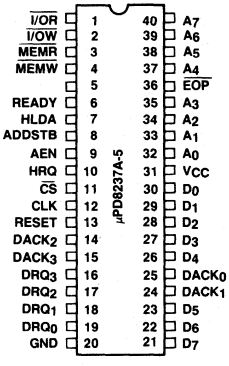
The three basic transfer modes allow the user to program the types of DMA service. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process (EOP).

Each channel has a full 64K byte address and word count capability.

Features

- ☐ Memory-to-memory transfers
- ☐ Memory block initialization
- ☐ Address increment or decrement
- ☐ Four independent DMA channels
- ☐ Multiple transfer modes: block, demand, single word, cascade
- ☐ Independent Autoinitialization of all channels
- ☐ Enable/Disable control of individual DMA requests
- ☐ Independent polarity control for DREQ and DACK signals
- ☐ End of Process input for terminating transfers
- ☐ Software DMA requests
- ☐ High performance: transfers up to 1.6 M-bytes/second
- ☐ Directly expandable to any number of channels
- ☐ 40-pin plastic or ceramic DIP

Pin Configuration



Pin Identification

No.	Symbol	Direction	Function
1	$\overline{I/OR}$	IN/OUT	In Idle state, $\overline{I/OR}$ is an input control line used by the CPU to read control registers. In Active state, the μPD8237A-5 uses $\overline{I/OR}$ as an output control signal to access data from a peripheral during a DMA Write.
2	$\overline{I/OW}$	IN/OUT	In Idle state, the CPU uses $\overline{I/OW}$ as an input control signal to load information to the μPD8237A-5. In Active state, the μPD8237A-5 uses $\overline{I/OW}$ as an output control signal to load data to a peripheral during a DMA Read. The rising edge of $\overline{WR}$ must follow each data byte transfer in order for the CPU to write to the μPD8237A-5. Holding $\overline{I/OW}$ low while toggling $\overline{CS}$ does not produce the same effect.
3	$\overline{MEMR}$	OUT	$\overline{MEMR}$ accesses data from a specified memory location during memory-to-peripheral or memory-to-memory transfers.
4	$\overline{MEMW}$	OUT	$\overline{MEMW}$ writes data to a specified memory location during peripheral-to-memory or memory-to-memory transfers.
5		IN	Pin 5 is always tied high.
6	READY	IN	The READY signal can extend memory read and write pulses for slow memories or I/O peripherals.
7	HLDA	IN	HLDA indicates that the CPU has relinquished control of the system buses.
8	ADDSTB	OUT	This signal strobes the upper address byte from D_0-D_7 into an external latch.
9	AEN	OUT	This signal allows the external latch to output the upper address byte by disabling the system bus during DMA cycles. You should use HLDA and AEN to deselect I/O peripherals that may be erroneously accessed during DMA transfers. The μPD8237A-5 deselects itself during DMA transfers.
10	HRQ	OUT	This signal requests control of the system bus. The μPD8237A-5 issues this signal in response to software requests or DRQ inputs from peripherals.
11	$\overline{CS}$	IN	The CPU uses $\overline{CS}$ to select the μPD8237A-5 as an I/O device during an I/O Read or Write by the CPU. This provides CPU communication on the data bus. $\overline{CS}$ may be held low during multiple transfers to or from the μPD8237A-5 as long as $\overline{I/OR}$ or $\overline{I/OW}$ is toggled following each transfer.
12	CLK	IN	Controls internal operations and data transfer rate.
13	RESET	IN	Clears the Command, Status, Request, and Temporary registers, the first/last flip/flop, and sets the Mask register. The μPD8237A-5 is in Idle state after a Reset.
14, 15 24, 25	$DACK_0$- $DACK_3$	OUT	These lines indicate an active channel. They are sometimes used to select a peripheral. Only one DACK may be active at any time. All DACK lines are inactive unless DMA has control of the bus. You may program the polarity of these lines; however, Reset initializes them to active low.
16-19	DRQ_0-DRQ_3	IN	These are asynchronous channel request inputs used by peripherals to request DMA service. In a Fixed Priority scheme, DRQ_0 has the highest priority and DRQ_3 has the lowest. You may program the polarity of these lines; however, Reset initializes them to active high.
20	GND		Ground.
21-23, 26-30	D_0-D_7	IN/OUT	During an I/O Read, the CPU enables these lines as outputs, allowing it to read an Address register, a Word Count register, or the Status or Temporary register. During an I/O Write, these lines are enabled as inputs, allowing the CPU to program the μPD8237A-5 control registers. During DMA cycles, the eight MSBs of the address are output to the data bus to be strobed to an external latch via ADDSTB.
31	V_{CC}		Power Supply.

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No.	Symbol	Direction	Function
32-35	A_0-A_3	IN/OUT	During DMA Idle states, these lines are inputs, allowing the CPU to load or examine control registers. During DMA Active states, these lines are outputs that provide the 4 LSB of the output address.
36	$\overline{EOP}$	IN/OUT	$\overline{EOP}$ signals that DMA service has been completed. When the word count of a channel becomes zero, the μPD8237A-5 pulses $\overline{EOP}$ low to notify the peripheral that DMA service is complete. The peripheral may pull $\overline{EOP}$ low to prematurely end DMA service. Internal or external receipt of $\overline{EOP}$ causes the currently active channel to end service, set its TC bit in the Status register, and reset its request bit. If the channel is programmed for Autoinitialization, the current registers are updated from the base registers. Otherwise, the channel's mask bit is set and the contents of the register are unaltered. $\overline{EOP}$ is output when TC for channel 1 occurs during memory-to-memory transfers. $\overline{EOP}$ applies to the channel with an active DACK. When $DACK_0$-$DACK_3$ are inactive, external $\overline{EOP}$s are ignored. It is recommended that you use an external pullup resistor of 3.3kΩ or 4.7kΩ. This pin cannot sink the current passed by a 1kΩ pullup.
37-40	A_4-A_7		These lines are outputs that provide the four LSB of the address. These lines are active only during DMA service.

Functional Description

The μPD8237A-5 has three basic control logic blocks, as shown in the block diagram. The Command Control block decodes commands issued by the CPU to the μPD8237A-5 before DMA requests are serviced. It also decodes the Mode Control word of each channel. The Timing Control block generates the external control signals and the internal timing. The Priority Encoder block settles priority contentions among channels simultaneously requesting service.

DMA Operation

The μPD8237A-5 operates in two states: Idle and Active. Each of these is made up of several smaller states equal to one clock cycle. The inactive state, S1, is entered when there are no pending DMA requests. The controller is inactive in S1, but the CPU may program it. S0 is the initial state for DMA service; the μPD8237A-5 requests a hold, but the CPU has not acknowledged. Transfers may begin upon acknowledgement from the CPU. The normal working states of DMA service are S1, S2, S3, and S4. If more time is needed for a transfer, a wait state, SW, can be inserted using the READY line.

A memory-to-memory transfer requires read-from-memory and write-to-memory operations. The states S11, S12, S13, and S14 provide the read-from operation. S21, S22, S23, and S24 provide the write-to part of the transfer. The byte is stored in the Temporary register between operations.

Idle State

When there are no pending service requests, the μPD8237A-5 is in the Idle state; more specifically, in S1. DRQ lines and $\overline{CS}$ are sampled to determine requests for DMA service and CPU attempts to inspect or modify the registers of the μPD8237A-5, respectively. The CPU can read or write to the registers when $\overline{CS}$ and HLDA are low. A_0–A_3 are used as inputs to the μPD8237A and select the registers affected. The $\overline{I/OR}$ and $\overline{I/OW}$ lines select and time the reads and writes. An internal flip-flop generates an additional address bit which determines the upper or lower byte of the Address and Word Count registers. This flip-flop can be reset by master Clear, Reset, or a software command.

When $\overline{CS}$ and HLDA are low (Program Phase), the μPD8237A-5 can execute special software commands. When $\overline{CS}$ and $\overline{I/OW}$ are active, the commands are decoded as addresses and do not use the data bus.

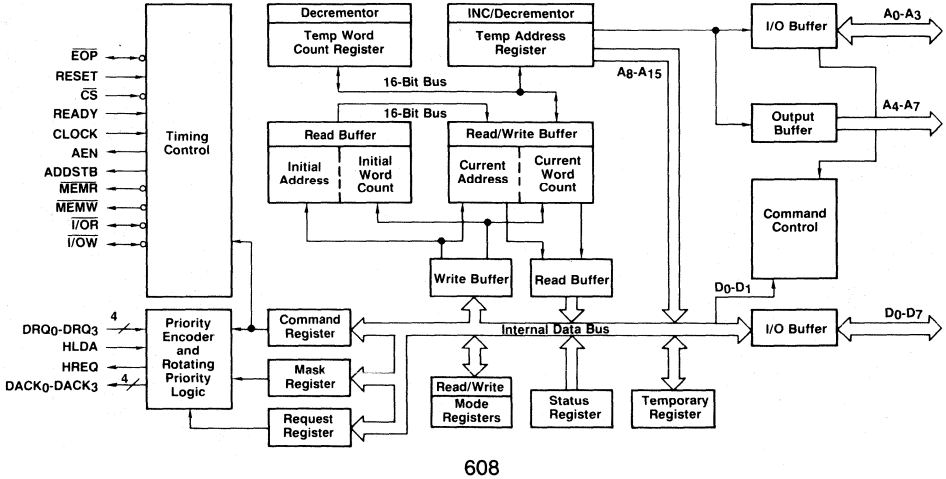
Active State

When a channel requests service while the μPD8237A-5 is in Idle state, the μPD8237A-5 outputs an HRQ to the CPU and enters the Active state. DMA service takes place in the Active state, in one of the four modes described below.

Byte Transfer Mode

In this mode, a one-byte transfer is made during each HRQ/HLDA handshake. HRQ goes active when DRQ goes active. The CPU responds by making HLDA active, and the one-byte transfer takes place. After the transfer, HRQ goes inactive, the word count is decremented, and the address is incremented or decremented. If the word count goes to zero, a Terminal Count (TC) causes

Block Diagram



an Autoinitialize if the channel has been programmed for it.

DRQ is held active only until the corresponding DACK goes active when a single transfer is performed. If DRQ is held active for a longer period, HRQ will become inactive after each transfer, become active again, and a one-byte transfer will be made after each rising edge of HLDA. This assures a full machine cycle between DMA transfers in 8080A/8085A systems. Timing between the μPD8237A-5 and other bus control protocols depends on the CPU being used.

Block Transfer Mode

In this mode, the μPD8237A-5 makes transfers until it encounters a TC or an external $\overline{EOP}$. Hold DRQ active only until DACK goes active. The channel will Autoinitialize at the end of the DMA service if it has been programmed to do so.

Demand Transfer Mode

In this mode, the μPD8237A-5 makes transfers until it encounters a TC or an external EOP, or until DRQ becomes inactive. This allows the device requesting service to stop the transfers by sending DRQ inactive. The device can resume service by making DRQ active. The Current Address and Current Word Count registers may be examined during the time between services when the CPU is allowed to operate. Autoinitialization can occur only after a TC or $\overline{EOP}$ at the end of the DMA service. After an Autoinitialization, there must be an active-going DRQ edge to begin new DMA service.

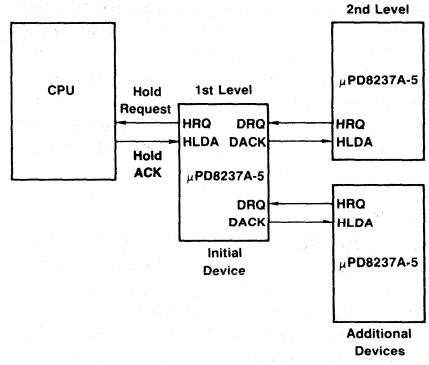
Cascade Mode

In this mode, you can expand your system by cascading several μPD8237A-5s together. Connect the HLDA and HRQ signals from the additional μPD8237A-5s to the DRQ and DACK signals of a channel of the initial μPD8237A-5. This scheme allows the additional devices to send the DMA requests through the priority resolution circuitry of the preceding device, preserving the priority chain and forcing the device to wait its turn to acknowledge requests. The cascade channel in the initial device does not output any address or control signals because its only function is that of assigning priorities. The μPD8237A-5 responds to DRQ with DACK, but all outputs except HRQ are disabled.

The following figure shows two μPD8237A-5s cascaded into two channels of another one, forming a two-level DMA system. You could add more devices at the second level by using the leftover channels of the first level; likewise, you could add more devices to form a third level by cascading into the channels of the second level.

Transfers

There are three types of transfers that can be performed by the three active transfer modes: Read, Write, and Verify. Read transfers activate $\overline{MEMR}$ and $\overline{I/OW}$ to move memory data to an I/O device. Write transfers activate $\overline{I/OR}$ and $\overline{MEMW}$ to move data from an I/O device to memory. Verify transfers are not really transfers; the μPD8237A-5 goes through the motions of a transfer but the memory and I/O lines are not active.



Memory-to-Memory Transfers

Use Block Transfer mode for memory-to-memory transfers. Mask out channels 0 and 1, and initialize the channel 0 word count to the same value as channel 1. Setting bit C0 of the command register to 1 makes channels 0 and 1 operate as memory-to-memory transfer channels. Channel 0 is the source address, channel 1 is the destination address, and the channel 1 word count is used. Initiate the memory-to-memory transfer by setting a DMA request for channel 0. You can write a single source word to a block of memory when channel 0 is programmed for a fixed source address. The μPD8237A-5 responds to external $\overline{EOP}$ signals during these transfers, but no DACK outputs are active. The $\overline{EOP}$ input may be used by data comparators doing block searches to end service when a match is found.

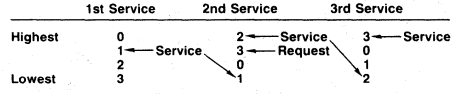
Autoinitialization

A channel may be set for Autoinitialize by programming a bit in the Mode register. Autoinitialize restores the original values of the Current Address and Current Word Count registers from the Initial Address and Initial Word Count registers of that channel. The CPU loads the Current and Initial registers simultaneously and they are unchanged through DMA service. $\overline{EOP}$ does not set the mask bit when the channel is in Autoinitialize. The channel can repeat its service following Autoinitialize without CPU intervention.

Priority Resolution

Two software-selectable priority resolution schemes are available on the μPD8237A-5: Fixed Priority and Rotating Priority. In the Fixed Priority scheme, priority is assigned by the value of the channel number. Channel 3 is the lowest priority and channel 0 is the highest priority.

In the Rotating Priority scheme, the channel that was just serviced assumes the lowest priority and the other channels move up accordingly. This guarantees that a device requesting service can be acknowledged after no more than three other devices have been serviced, preventing any channel from monopolizing the system.



The highest priority channel is selected on each active-going HLDA edge. Once service to a channel begins, it cannot be interrupted by a request from a higher priority channel. A higher priority channel gets control only when the lower priority channel releases HRQ. The CPU gets bus control when control passes from channel to channel, ensuring that a rising HLDA edge can be generated to select the new highest priority request.

Transfer Timing

You can cut transfer timing, if the system allows, by compressing the transfer time to two clock periods. Since state 3 (S_3) extends the access time for the read pulse, you can eliminate S_3, making the width of the read pulse equal to the write pulse. A transfer is then made up of S_2 to change the address and S_4 to perform the read or write. When the address lines A_8–A_{15} need to be updated, S_1 states occur.

Generating Addresses

The eight MSBs of the address are multiplexed on the data lines. These bits are output to an external latch during S_1, after which they can be placed on the address bus. The falling edge of ADDSTB loads the bits from the data lines to the latch. AEN places the bits on the address bus. The eight LSBs of the address are directly output on lines A_0–A_7. Connect A_0–A_7 to the address bus.

Sequential addresses are generated during Block and Demand Transfer mode operations because they include several transfers. Often, data in the external address latch does not change; it changes only when a carry or borrow from A_7 to A_8 occurs in the sequence of addresses. S1 states are executed only when A_8–A_{15} need to be updated. In the course of lengthy transfers, S1 states may be executed only once every 256 transfers.

Registers

The following chart summarizes the registers of the μPD8237A-5.

Register	Bits
Current Address registers (4)	16
Current Word Count registers (4)	16
Initial Address registers (4)	16
Initial Word Count registers (4)	16
Command register	8
Mode registers (4)	6
Request register	4
Mask register	4
Status register	8
Temporary register	8
Temporary Address register	16
Temporary Word Count register	16

Current Address Register

There is a Current Address register for each channel. This register holds the address used for DMA transfers; the address is incremented or decremented after each transfer and the intermediate values are stored here during the transfer. The CPU writes or reads this register in 8-bit bytes. An Autoinitialize restores this register to its initial value.

Current Word Count Register

There is a Current Word Count register for each channel. Program this register with the value of the number of words to be transferred, minus one. The word count is decremented after each transfer and intermediate values are stored in this register during the transfer. A TC is generated when the word count is zero. The CPU writes or reads this register in 8-bit bytes during Program Phase. An Autoinitialize restores this register to its initial value. After an internally generated $\overline{EOP}$, the contents of this register will be FFFFH.

Initial Address and Initial Word Count Registers

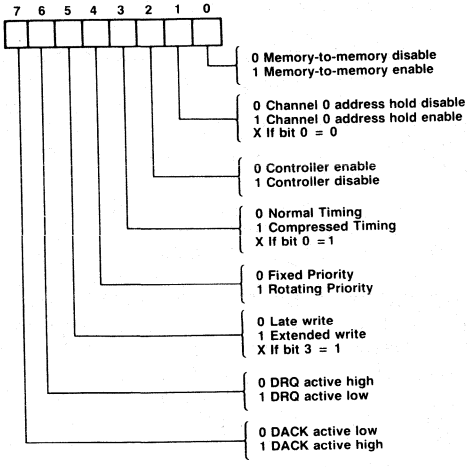
There is an Initial Address register and an Initial Word Count register for each channel. The initial values of the associated Current registers are stored in these registers. The values in these registers are used to restore the Current registers at Autoinitialize. During DMA programming, the CPU writes the Initial registers and the corresponding Current registers at the same time, in 8-bit bytes. Intermediate values in the Current registers are overwritten if you write to the Initial registers while the Current registers contain intermediate values. The CPU cannot read the Initial registers.

		Signals							Internal Flip-Flop	
Channel	Operation	$\overline{CS}$	$\overline{I/OR}$	$\overline{I/OW}$	A_3	A_2	A_1	A_0		D_0-D_7
0	Initial & Current Address Write	0	1	0	0	0	0	0	0	A_0-A_7
		0	1	0	0	0	0	0	1	A_8-A_{15}
	Current Address Read	0	0	1	0	0	0	0	0	A_0-A_7
		0	0	1	0	0	0	0	1	A_8-A_{15}
	Initial & Current Word Count Write	0	1	0	0	0	0	1	0	W_0-W_7
		0	1	0	0	0	0	1	1	W_8-W_{15}
	Current Word Count Read	0	0	1	0	0	0	1	0	W_0-W_7
		0	0	1	0	0	0	1	1	W_8-W_{15}
1	Initial & Current Address Write	0	1	0	0	0	1	0	0	A_0-A_7
		0	1	0	0	0	1	0	1	A_8-A_{15}
	Current Address Read	0	0	1	0	0	1	0	0	A_0-A_7
		0	0	1	0	0	1	0	1	A_8-A_{15}
	Initial & Current Word Count Write	0	1	0	0	0	1	1	0	W_0-W_7
		0	1	0	0	0	1	1	1	W_8-W_{15}
	Current Word Count Read	0	0	1	0	0	1	1	0	W_0-W_7
		0	0	1	0	0	1	1	1	W_8-W_{15}
2	Initial & Current Address Write	0	1	0	0	1	0	0	0	A_0-A_7
		0	1	0	0	1	0	0	1	A_8-A_{15}
	Current Address Read	0	0	1	0	1	0	0	0	A_0-A_7
		0	0	1	0	1	0	0	1	A_8-A_{15}
	Initial & Current Word Count Write	0	1	0	0	1	0	1	0	W_0-W_7
		0	1	0	0	1	0	1	1	W_8-W_{15}
	Current Word Count Read	0	0	1	0	1	0	1	0	W_0-W_7
		0	0	1	0	1	0	1	1	W_8-W_{15}
3	Initial & Current Address Write	0	1	0	0	1	1	0	0	A_0-A_7
		0	1	0	0	1	1	0	1	A_8-A_{15}
	Current Address Read	0	0	1	0	1	1	0	0	A_0-A_7
		0	0	1	0	1	1	0	1	A_8-A_{15}
	Initial & Current Word Count Write	0	1	0	0	1	1	1	0	W_0-W_7
		0	1	0	0	1	1	1	1	W_8-W_{15}
	Current Word Count Read	0	0	1	0	1	1	1	0	W_0-W_7
		0	0	1	0	1	1	1	1	W_8-W_{15}

Word Count and Address Register Command Codes

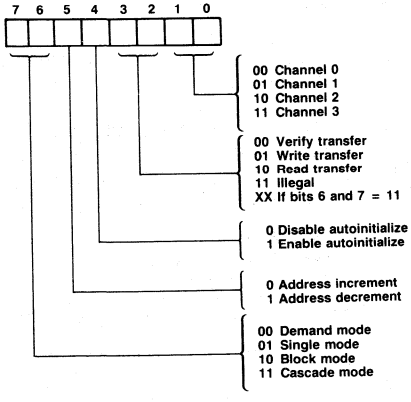
Command Register

The CPU programs this register during Program Phase. The register can be cleared with Reset.



Mode Register

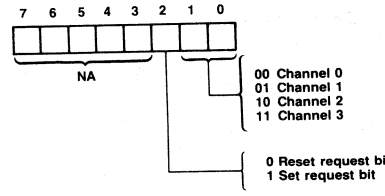
There is a Mode register associated with each channel. When the CPU writes to this register during the Program Phase, bits 0 and 1 determine on which channel Mode register the operation is performed.



Request Register

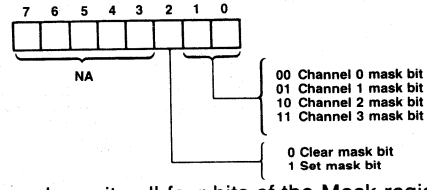
This register allows the μPD8237A-5 to respond to DMA requests from software as well as hardware. There is a bit pattern for each channel in the Request register. These bits can be prioritized by the Priority Resolving circuitry and are not maskable. Each bit is set or reset under software control or cleared when TC or an external $\overline{EOP}$ is generated. A Reset clears the entire register. The correct data word is loaded by software to set or reset a bit.

Software requests receive service only when the channel is in Block mode. The software request for channel 0 should be set at the beginning of a memory-to-memory transfer.

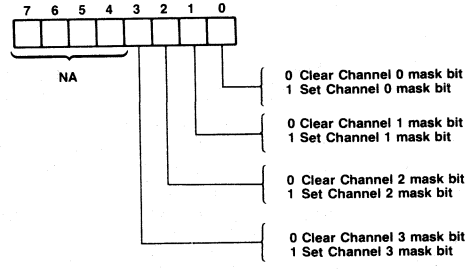


Mask Register

There is a mask bit for each channel which can disable an incoming DRQ. If the channel is not set for Autoinitialize, each mask bit is set when its channel produces an $\overline{EOP}$. Each bit can be set or cleared under software control. Reset clears the register. This disallows DMA requests until they are permitted by a Clear Mask Register instruction.

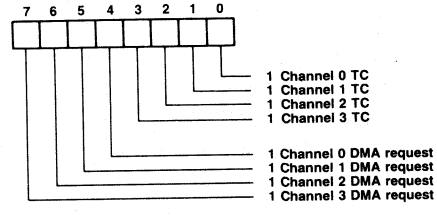


You may also write all four bits of the Mask register with a single command.



Status Register

The Status register indicates which channels have made DMA requests and which channels have reached TC. Each time a channel reaches TC, including after Autoinitialization, bits 0–3 are set. Status Read and Reset clear these bits. Bits 4–7 are set when a channel is requesting service. The CPU can read the Status register.



Temporary Register

The Temporary register holds data during memory-to-memory transfers. The CPU can read the last word moved when the transfer is complete. This register always contains the last byte transferred in a memory-to-memory transfer unless cleared by a Reset.

Software Commands

There are two software commands that can be executed in the Program Phase. These commands are independent of data on the data bus.

Clear First/Last Flip-Flop

You may issue this command before reading or writing any word count or address information. It allows the CPU to access registers, addressing upper and lower bytes correctly, by initializing the flip-flop to an identifiable state.

Master Clear

This command produces the same effect as Reset. It clears the Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers, sets the Mask register, and causes the μPD8237A-5 to enter Idle state.

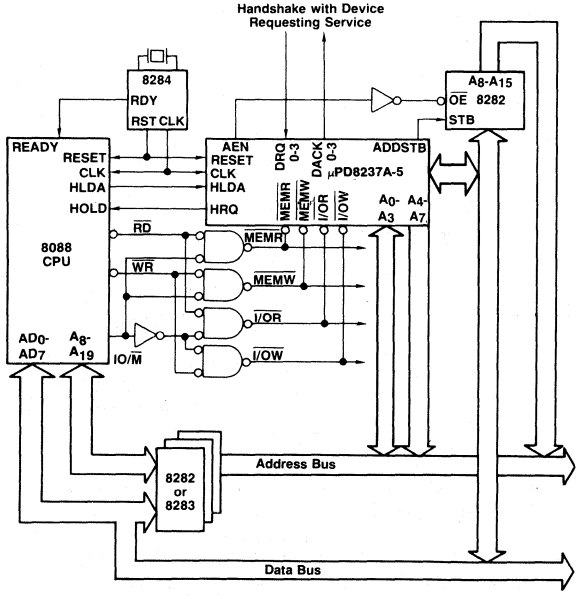
The following chart illustrates address codes for the software commands.

A_3	A_2	A_1	A_0	$\overline{I/OW}$	$\overline{I/OR}$	Operation
1	0	0	0	0	1	Read Status register
1	0	0	0	1	0	Write to Command register
1	0	0	1	1	0	Write to Request register
1	0	1	0	1	0	Write a Mask register bit
1	0	1	1	1	0	Write to Mode register
1	1	0	0	1	0	Clear byte pointer flip-flop
1	1	0	1	0	1	Read Temporary register
1	1	0	1	1	0	Master Clear
1	1	1	1	1	0	Write all Mask register bits

All other bit combinations are illegal.

Application Example

The following diagram shows an application using the μPD8237A-5 with an 8088. The μPD8237A-5 sends a hold request to the CPU whenever there is a valid DMA request from a peripheral device. The μPD8237A-5 takes control of the Address, Data, and Control buses when the CPU replies with an HLDA signal. The address for the first transfer appears in two bytes: the eight LSBs are output on A_0–A_7 and the eight MSBs are output on the data bus pins. The contents of the data bus pins are latched to the 8282 to make up the 16 bits of the address bus. Once the address is latched, the data bus transfers data to or from a memory location or I/O device, using the control bus signals generated by the μPD8237A-5.



AC Characteristics Supplementary Information

All AC timing measurement points are 2.0V for high and 0.8V for low, for both inputs and outputs. The loading on the outputs is one TTL gate plus 100 pF of capacitance for the data bus pins, and one TTL gate plus 50 pF for all other outputs.

Recovery time between successive read and write inputs must be at least 400 ns. I/O or memory write pulse widths will be T_{CY} – 100 ns for normal DMA transfers and 2 T_{CY} – 100 ns for extended cycles. I/O or memory reads will be 2 T_{CY} – 50 ns for normal reads and T_{CY} – 50 ns for compressed cycles. T_{DQ1} and T_{DQ2} are measured on two different levels. T_{DQ1} at 2.0V, T_{DQ2} at 3.3V with a 3.3 kΩ pull-up resistor. DREQ and DACK are both active high and low. DREQ must be held in the active state (user defined) until DACK is returned from the μPD8237A-5. The AC waveforms assume these are programmed to the active high state.

Absolute Maximum Ratings*

Tentative	
Ambient Temperature under Bias	0°C to +70°C
Storage Temperature	−65°C to 150°C
Voltage on any Pin with respect to Ground	−0.5V to +7V
Power Dissipation	1.5 Watt

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ ①	Max	Unit	Test Conditions
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −200 μA
		3.3			V	I_{OH} = −100 μA (HRQ Only)
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA (Data Bus)
						I_{OL} = 3.2 mA (Other Outputs)
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input Load Current	I_{LI}			±10	μA	$0V \leq V_{IN} \leq V_{CC}$
Output Leakage Current	I_{LO}			±10	μA	$0.45 \leq V_{OUT} \leq V_{CC}$
V_{CC} Supply Current	I_{CC}		65	130	mA	T_a = +25°C
			75	150	mA	T_a = 0°C

Note:

① Typical values measured at T_a = 25°C, nominal processing parameters, and nominal V_{CC}.

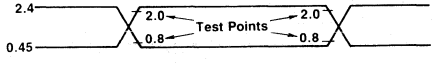
Capacitance

Parameter	Symbol	Limits Min	Typ ①	Max	Unit	Test Conditions
Output Capacitance	C_O		4	8	pF	fc = 1.0 MHz, Inputs = 0V
Input Capacitance	C_I		8	15	pF	
I/O Capacitance	C_{IO}		10	18	pF	

Note:

① Typical values measured at T_a = 25°C, nominal processing parameters, and nominal V_{CC}.

AC Testing Input/Output Waveform



Inputs are driven at 2.4V for logic 1 and 0.45V for logic 0. These timing measurements are made at 2.0V for logic 1 and 0.8V for logic 0. A transition time of 20 ns or less is assumed for input timing parameters. Unless noted, output loading is 1 TTL gate plus 50 pF capacitance.

AC Characteristics

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit
AEN High from CLK Low (S1) Delay Time	t_{AEL}			200	ns
AEN Low from CLK High (S1) Delay Time	t_{AET}			130	ns
ADR Active to Float Delay from CLK High	t_{AFAB}			90	ns
$\overline{READ}$ or $\overline{WRITE}$ Float from CLK High	t_{AFC}			120	
DB Active to Float Delay from CLK High	t_{AFDB}			170	ns
ADR from $\overline{READ}$ High Hold Time	t_{AHR}	t_{CY} – 100			ns
DB from ADDSTB Low Hold Time	t_{AHS}	30			ns
ADR from $\overline{WRITE}$ High Hold Time	t_{AHW}	t_{CY} – 50			ns
DACK Valid from CLK Low Delay Time				170	ns
$\overline{EOP}$ High from CLK High Delay Time	t_{AK}			170	ns
$\overline{EOP}$ Low to CLK High Delay Time				100	ns
ADR Stable from CLK High	t_{ASM}			170	ns
Data Bus to ADDSTB Low Setup Time	t_{ASS}	100			ns
Clock High Time (Transitions ≤ 10 ns)	t_{CH}	80			ns
Clock Low Time (Transitions ≤ 10 ns)	t_{CL}	68			
CLK Cycle Time	t_{CY}	200			ns
CLK High to $\overline{READ}$ or $\overline{WRITE}$ Low Delay ①	t_{DCL}			190	ns
$\overline{READ}$ High from CLK High (S4) Delay Time ①	t_{DCTR}			190	ns
$\overline{WRITE}$ High from CLK High (S4) Delay Time ①	t_{DCTW}			130	ns
HRQ Valid from CLK High Delay Time ②	t_{DQ1}			120	ns
	t_{DQ2}			120	ns
$\overline{EOP}$ Low from CLK Low Setup Time	t_{EPS}	40			
$\overline{EOP}$ Pulse Width	t_{EPW}	220			ns
ADR Float to Active Delay from CLK High	t_{FAAB}			170	ns
$\overline{READ}$ or $\overline{WRITE}$ Active from CLK High	t_{FAC}			150	ns
Data Bus Float to Active Delay from CLK High	t_{FADB}			200	ns
HLDA Valid to CLK High Setup Time	t_{HS}	75			ns
Input Data from $\overline{MEMR}$ High Hold Time	t_{IDH}	0			ns
Input Data to $\overline{MEMR}$ High Setup Time	t_{IDS}	170			ns
Output Data from $\overline{MEMW}$ High Hold Time	t_{ODH}	10			ns
Output Data Valid to $\overline{MEMW}$ High	t_{ODV}	130			ns
DRQ to CLK Low (S_1, S_4) Setup Time	t_{QS}	0			ns
CLK to READY Low Hold Time	t_{RH}	20			ns
READY to CLK Low Setup Time	t_{RS}	75			ns
ADDSTB High from CLK High Delay Time	t_{STL}			130	ns
ADDSTB Low from CLK High Delay Time	t_{STT}			90	ns

Notes:

① Net $\overline{I/OW}$ or $\overline{MEMW}$ pulse width for normal write is t_{CY} – 100 ns and $2t_{CY}$ – 100 ns for extended write. Net $\overline{I/OR}$ or $\overline{MEMR}$ pulse width for normal read is $2t_{CY}$ – 50 ns and t_{CY} – 50 ns for compressed read.

② T_{DQ1} is measured at 2.0V. t_{DQ2} is measured at 3.3V. An external pullup resistor of 3.3kΩ connected from HRQ to V_{CC} is assumed for t_{DQ2}.

AC Characteristics Peripheral Mode

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit
ADR Valid or $\overline{CS}$ Low to $\overline{READ}$ Low	t_{AR}	50			ns
ADR Valid to $\overline{WRITE}$ High Setup Time	t_{AW}	160			ns
$\overline{CS}$ Low to $\overline{WRITE}$ High Setup Time	t_{CW}	160			ns
Data Valid to $\overline{WRITE}$ High Setup Time	t_{DW}	160			ns
ADR or $\overline{CS}$ Hold from $\overline{READ}$ High	t_{RA}	0			ns
Data Access from $\overline{READ}$ Low ①	t_{RDE}			140	ns
Data Bus Float Delay from $\overline{READ}$ High	t_{RDF}	0		70	ns
Power Supply High to RESET Low Setup Time	t_{RSTD}	500			ns
RESET to First I/OW	t_{RSTS}	$2t_{CY}$			ns
RESET Pulse Width	t_{RSTW}	300			ns
$\overline{READ}$ Width	t_{RW}	200			ns
ADR from $\overline{WRITE}$ High Hold Time	t_{WA}	20			ns
$\overline{CS}$ High from $\overline{WRITE}$ High Hold Time	t_{WC}	20			ns
Data from $\overline{WRITE}$ High Hold Time	t_{WD}	30			ns
Write Width	t_{WWS}	160			ns

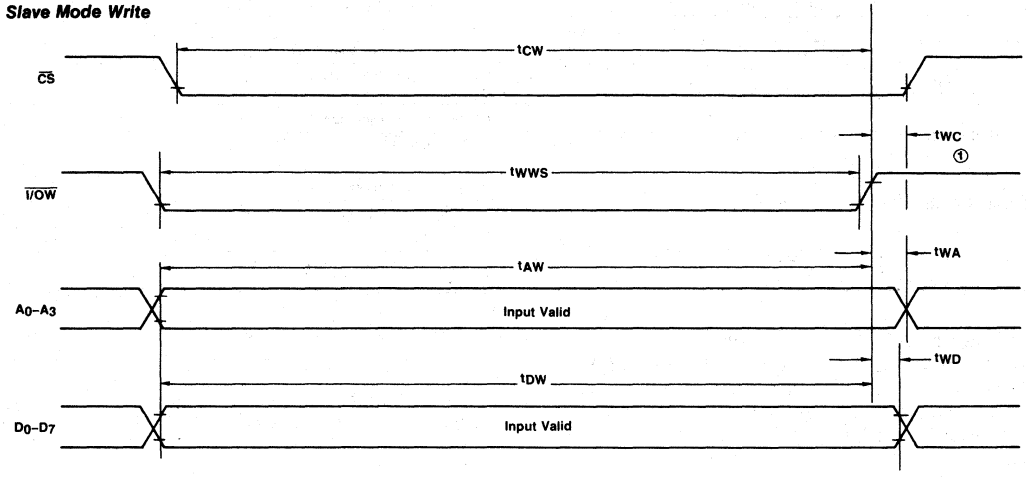
Note:

① Data bus output loading is 1 TTL gate plus 100 pF capacitance.

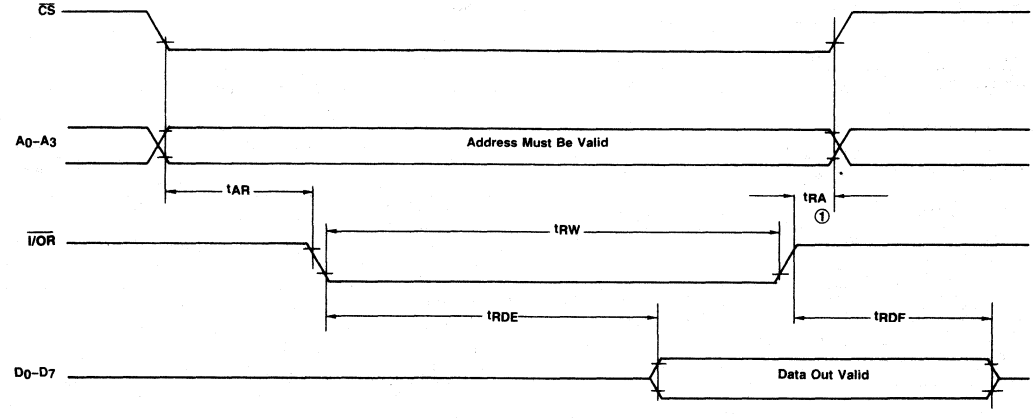
9

Timing Waveforms

Slave Mode Write



Slave Mode Read

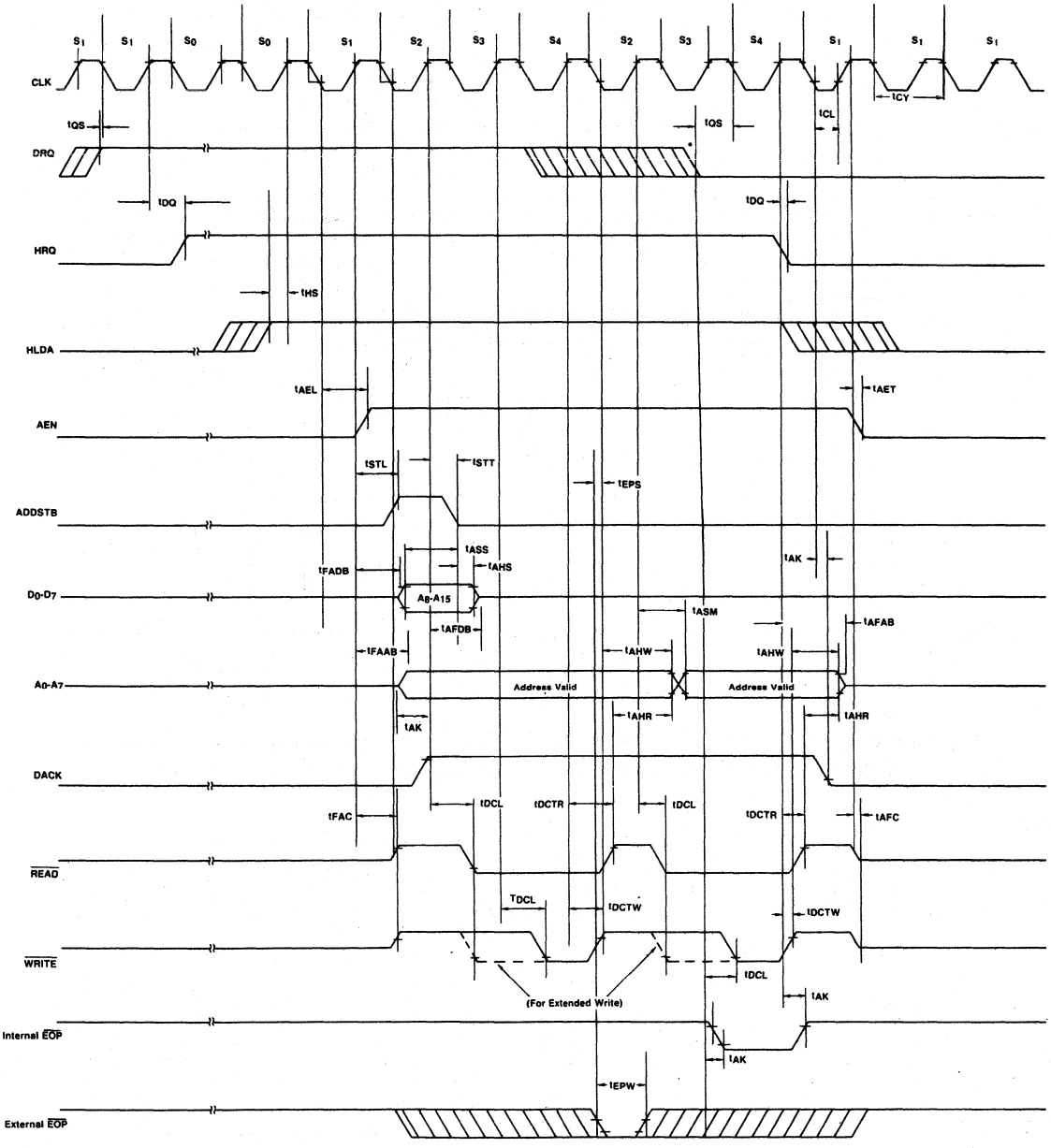


Note:

① You must time successive read or write operations by the CPU to allow at least 400 ns recovery time for the μPD8237A-5 between read and write pulses.

Timing Waveforms (Cont.)

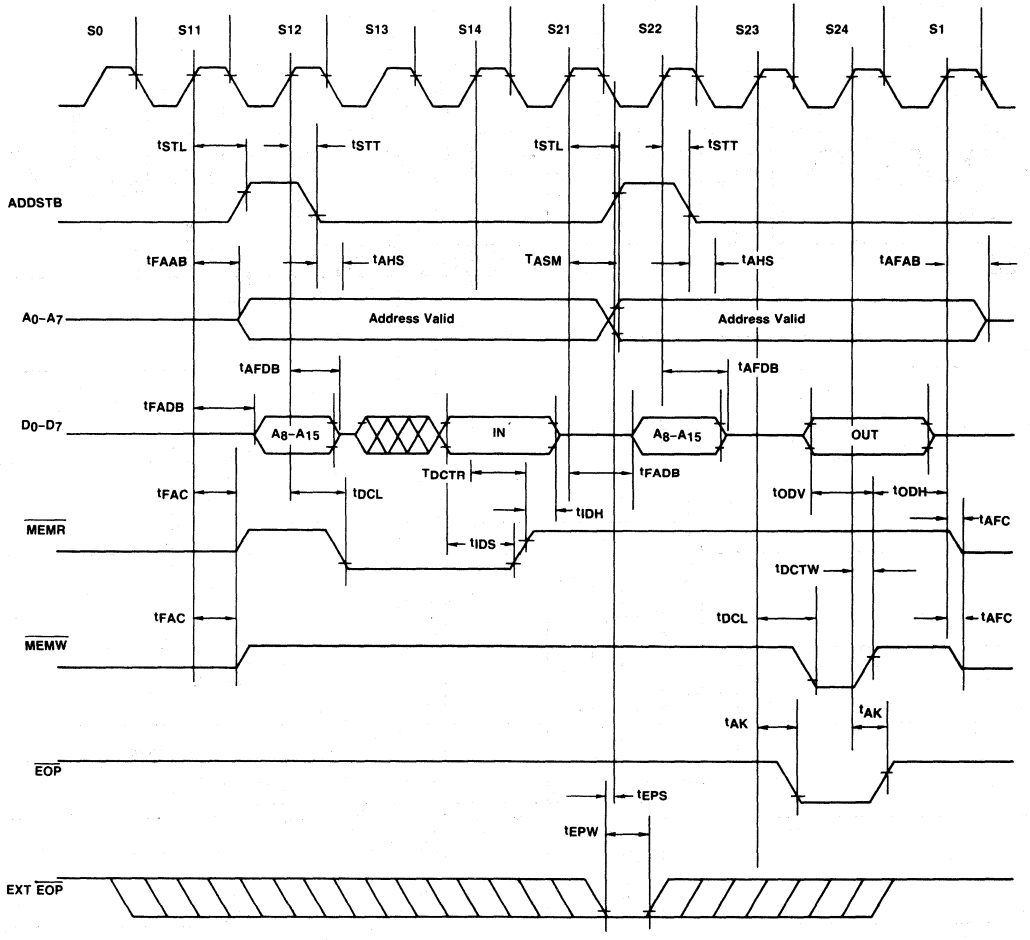
DMA Transfer



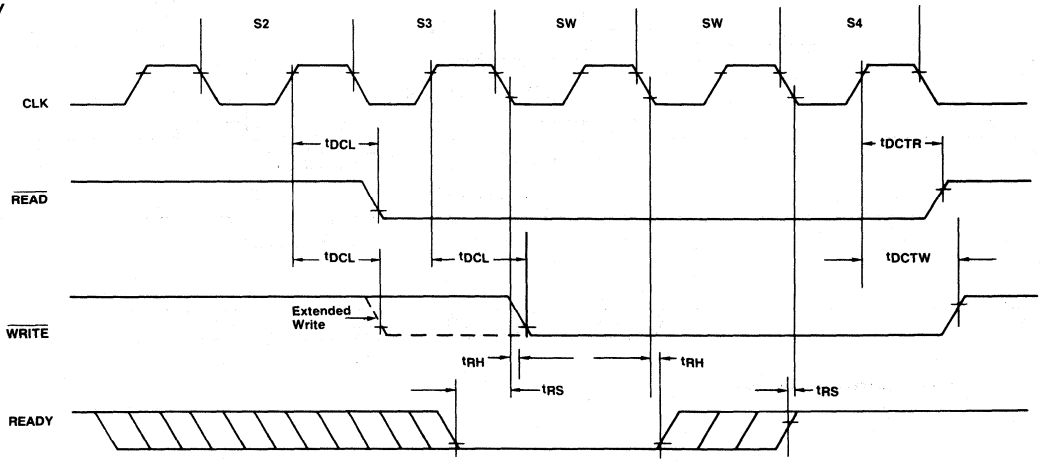
*See Note 2, AC Characteristics, DMA Mode

Timing Waveforms (Cont.)

Memory-to-Memory Transfer

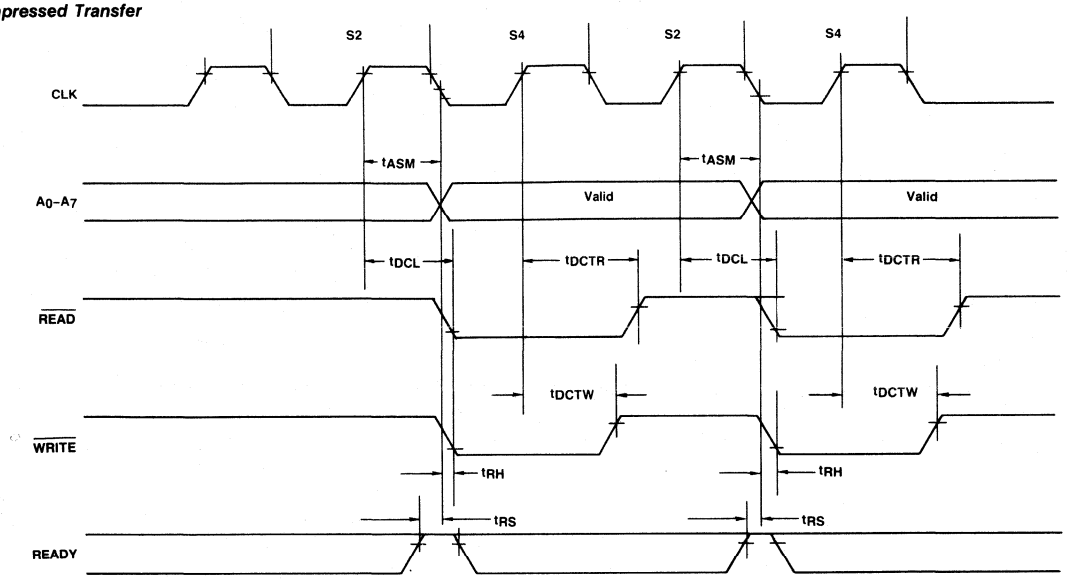


Ready

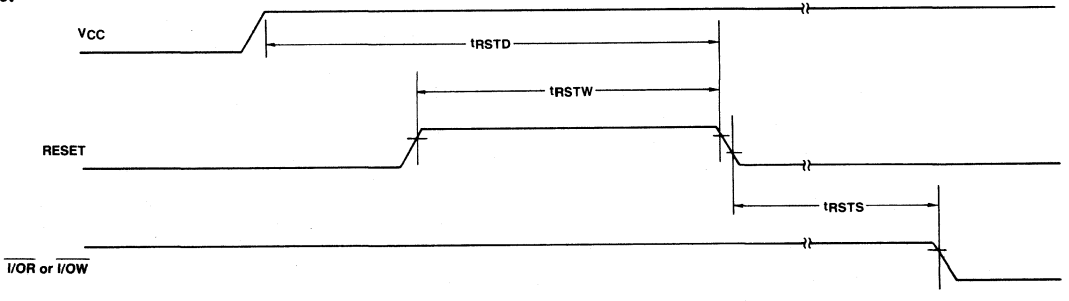


Timing Waveforms (Cont.)

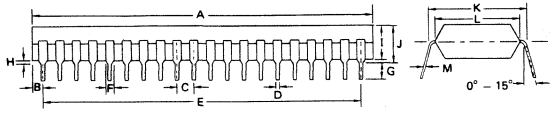
Compressed Transfer



Reset



Package Outline μPD8237AC-5



Plastic

Item	Millimeters	Inches
A	51.5 Max	2.028 Max
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 Min	0.047 Min
G	2.54 Min	0.10 Min
H	0.5 Min	0.019 Min
I	5.22 Max	0.206 Max
J	5.72 Max	0.225 Max
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

9

INPUT/OUTPUT EXPANDER FOR μPD8048 FAMILY

DESCRIPTION

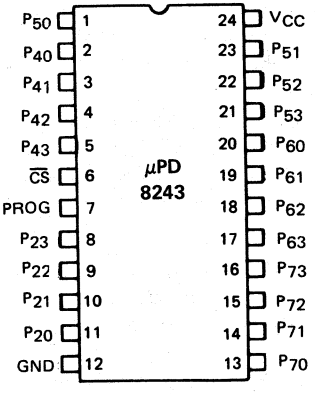
The μPD8243 input/output expander is directly compatible with the μPD8048 family of single-chip microcomputers. Using NMOS technology the μPD8243 provides high drive capabilities while requiring only a single +5V supply voltage.

The μPD8243 interfaces to the μPD8048 family through a 4-bit I/O port and offers four 4-bit bi-directional static I/O ports. The ease of expansion allows for multiple μPD8243's to be added using the bus port.

The bi-directional I/O ports of the μPD8243 act as an extension of the I/O capabilities of the μPD8048 microcomputer family. They are accessible with their own ANL, MOV, and ORL instructions.

FEATURES

- Four 4-Bit I/O Ports
- Fully Compatible with μPD8048 Microcomputer Family
- High Output Drive
- NMOS Technology
- Single +5V Supply
- Direct Extension of Resident μPD8048 I/O Ports
- Logical AND and OR Directly to Ports
- Compatible with Industry Standard 8243
- Available in a 24-Pin Plastic Package



9

FUNCTIONAL DESCRIPTION

General Operation

The I/O capabilities of the μPD8048 family can be enhanced in four 4-bit I/O port increments using one or more μPD8243's. These additional I/O lines are addressed as ports 4-7. The following lists the operations which can be performed on ports 4-7.

- Logical AND Accumulator to Port.
- Logical OR Accumulator to Port.
- Transfer Port to Accumulator.
- Transfer Accumulator to Port.

Port 2 (P_{20}-P_{23}) forms the 4-bit bus through which the μPD8243 communicates with the host processor. The PROG output from the μPD8048 family provides the necessary timing to the μPD8243. There are two 4-bit nibbles involved in each data transfer. The first nibble contains the op-code and port address followed by the second nibble containing the 4-bit data. Multiple μPD8243's can be used for additional I/O. The output lines from the μPD8048 family can be used to form the chip selects for the additional μPD8243's.

Power On Initialization

Applying power to the μPD8243 sets ports 4-7 to the tri-state mode and port 2 to the input mode. The state of the PROG pin at power on may be either high or low. The PROG pin must make a high-to-low transition in order to exit from the power on mode. The power on sequence is initiated any time V_{CC} drops below 1V. The table below shows how the 4-bit nibbles on Port 2 correspond to the μPD8243 operations.

Port Address			Op-Code		
P_{21}	P_{20}	Address Code	P_{23}	P_{22}	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

For example an 0010 appearing on P_{20}-P_{23}, respectively, would result in a Write to Port 4.

Read Mode

There is one Read mode in the μPD8243. A falling edge on the PROG pin latches the op-code and port address from input Port 2. The port address and Read operation are then decoded causing the appropriate outputs to be tri-stated and the input buffers switched on. The rising edge of PROG terminates the Read operation. The Port (4,5,6, or 7) that was selected by the Port address (P_{21}-P_{20}) is returned to the tri-state mode, and Port 2 is switched to the input mode.

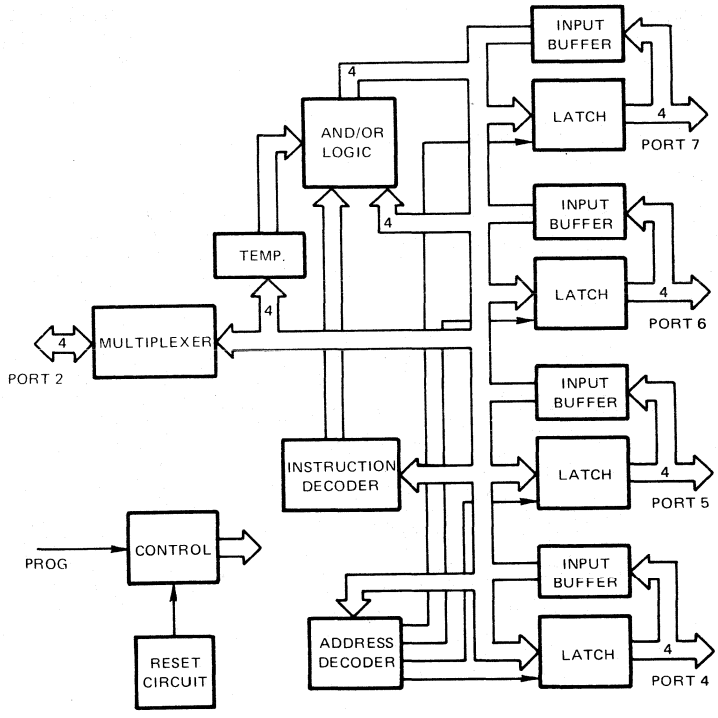
Generally, in the read mode, a port will be an input and in the write mode it will be an output. If during program operation, the μPD8243's modes are changed, the first read pulse immediately following a write should be ignored. The subsequent read signals are valid. Reading a port will then force that port to a high impedance state.

Write Modes

There are three write modes in the μPD8243. The MOVD $P_{p,A}$ instruction from the μPD8048 family writes the new data directly to the specified port (4,5,6, or 7). The old data previously latched at that port is lost. The ORLD $P_{p,A}$ instruction performs a logical OR between the new data and the data currently latched at the selected port. The result is then latched at that port. The final write mode uses the ANLD $P_{p,A}$ instruction. It performs a logical AND between the new data and the data currently latched at the specified port. The result is latched at that port.

The data remains latched at the selected port following the logical manipulation until new data is written to that port.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
2-5 1, 21-23 17-20 13-16	P_{40}-P_{43} P_{50}-P_{53} P_{60}-P_{63} P_{70}-P_{73}	The four 4-bit static bi-directional I/O ports. They are programmable into the following modes: input mode (during a Read operation); low impedance latched output mode (after a Write operation); and the tri-state mode (following a Read operation). Data appearing on I/O lines P_{20}-P_{23} can be written directly. That data can also be logically ANDed or ORed with the previous data on those lines.
6	$\overline{CS}$	Chip Select input (active-low). When the μPD8343 is deselected ($\overline{CS}$ = 1), output or internal status changes are inhibited.
7	PROG	Clock input pin. The control and address information are present on port lines P_{20}-P_{23} when PROG makes a high-to-low transition. Data is present on port lines P_{20}-P_{23} when PROG makes a low-to-high transition.
8-11	P_{20}-P_{23}	P_{20}-P_{23} form a 4-bit bi-directional port. Refer to PROG function for contents of P_{20}-P_{23} at the rising and falling edges of PROG. Data from a selected port is present on P_{20}-P_{23} prior to the rising edge of PROG if during a Read operation.
12	GND	The μPD8041/8741 ground potential.
24	V_{CC}	+5 volt supply.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	-0.5 to +7 Volts①
Power Dissipation	1 W

Note: ① With respect to ground.

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage (Ports 4-7)	V_{OL1}			0.45	V	I_{OL} = 5 mA ①
Output Low Voltage (Port 7)	V_{OL2}			1	V	I_{OL} = 20 mA
Output Low Voltage (Port 2)	V_{OL3}			0.45	V	I_{OL} = 0.6 mA
Output High Voltage (Ports 4-7)	V_{OH1}	2.4			V	I_{OH} = 240 μA
Output High Voltage (Port 2)	V_{OH2}	2.4			V	I_{OH} = 100 μA
Sum of All I_{OL} From 16 Outputs	I_{OL}			100	mA	5 mA Each Pin
Input Leakage Current (Ports 4-7)	I_{IL1}	-10		20	μA	V_{IN} = V_{CC} to 0V
Input Leakage Current (Port 2, $\overline{CS}$, PROG)	I_{IL2}	-10		10	μA	V_{IN} = V_{CC} to 0V
V_{CC} Supply Current	I_{CC}		10	20	mA	

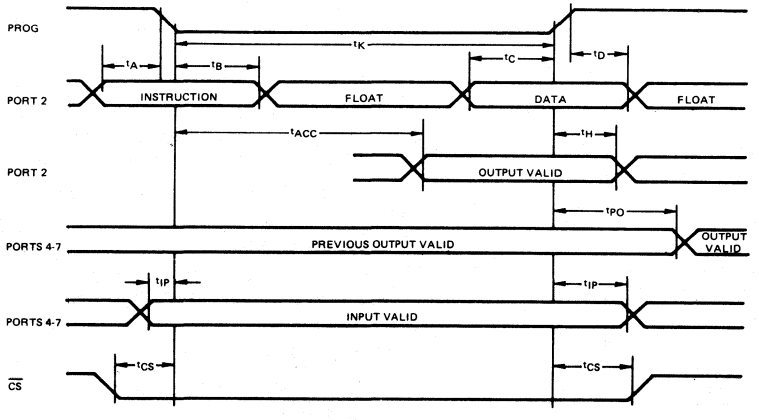
Note: ① Refer to graph of additional sink current drive.

AC CHARACTERISTICS

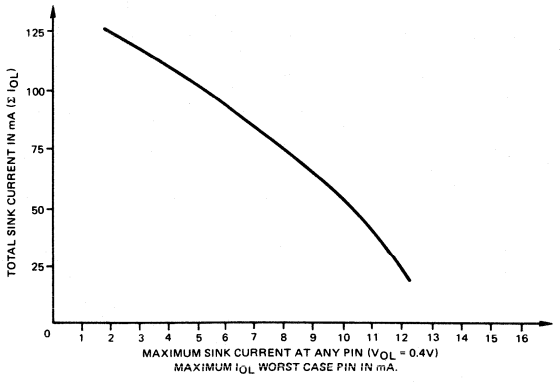
T_a = 0°C to +70°C; V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Code Valid Before PROG	t_A	100			ns	80 pF Load
Code Valid After PROG	t_B	60			ns	20 pF Load
Data Valid Before PROG	t_C	200			ns	80 pF Load
Data Valid After PROG	t_D	20			ns	20 pF Load
Port 2 Floating After PROG	t_H	0		150	ns	20 pF Load
PROG Negative Pulse Width	t_K	700			ns	
Ports 4-7 Valid After PROG	t_{PO}			700	ns	100 pF Load
Ports 4-7 Valid Before/After PROG	t_{LP1}	100			ns	
Port 2 Valid After PROG	t_{ACC}			650	ns	80 pF Load
$\overline{CS}$ Valid Before/After PROG	$t_{\overline{CS}}$	50			ns	

TIMING WAVEFORMS

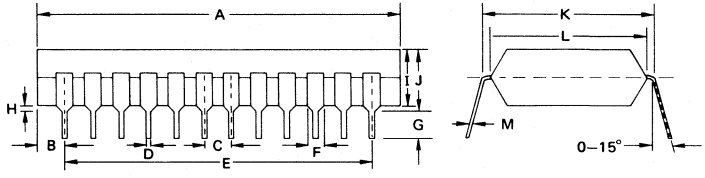


CURRENT SINKING CAPABILITY ①



Note: ① This curve plots the guaranteed worst case current sinking capability of any I/O port line versus the total sink current of all pins. The μPD8243 is capable of sinking 5 mA (for V_{OL} = 0.4V) through each of the 16 I/O lines simultaneously. The current sinking curve shows how the individual I/O line drive increases if all the I/O lines are not fully loaded.

PACKAGE OUTLINES μPD8243C



(PLASTIC)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

9

CMOS INPUT/OUTPUT EXPANDER FOR μPD8048/80C48 FAMILY

DESCRIPTION

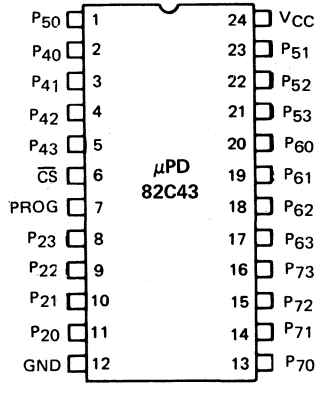
The μPD82C43 input/output expander is directly compatible with the μPD8048/80C48 family of single-chip microcomputers. Using NMOS technology the μPD82C43 provides high drive capabilities while requiring only a single +5V supply voltage.

The μPD82C43 interfaces to the μPD8048/80C48 family through a 4-bit I/O port and offers four 4-bit bi-directional static I/O ports. The ease of expansion allows for multiple μPD8243s to be added using the bus port.

The bi-directional I/O ports of the μPD82C43 act as an extension of the I/O capabilities of the μPD8048/80C48 microcomputer family. They are accessible with their own ANL, MOV, and ORL instructions.

FEATURES

- Four 4-Bit I/O Ports
- Fully Compatible with μPD8048/80C48 Microcomputer Family
- High Output Drive
- NMOS Technology
- Single +5V Supply
- Direct Extension of Resident μPD8048/80C48 I/O Ports
- Logical AND and OR Directly to Ports
- Compatible with Industry Standard 8243
- Available in a 24-Pin Plastic Package



9

FUNCTIONAL DESCRIPTION

General Operation

The I/O capabilities of the μPD8048/80C48 family can be enhanced in four 4-bit I/O port increments using one or more μPD82C43s. These additional I/O lines are addressed as ports 4-7. The following lists the operations which can be performed on ports 4-7.

- Logical AND Accumulator to Port.
- Logical OR Accumulator to Port.
- Transfer Port to Accumulator.
- Transfer Accumulator to Port.

Port 2 (P_{20}-P_{23}) forms the 4-bit bus through which the μPD82C43 communicates with the host processor. The PROG output from the μPD8048/80C48 family provides the necessary timing to the μPD82C43. There are two 4-bit nibbles involved in each data transfer. The first nibble contains the op-code and port address followed by the second nibble containing the 4-bit data. Multiple μPD82C43s can be used for additional I/O. The output lines from the μPD8048/80C48 family can be used to form the chip selects for the additional μPD82C43s.

Power On Initialization

Applying power to the μPD82C43 sets ports 4-7 to the tri-state mode and port 2 to the input mode. The state of the PROG pin at power on may be either high or low. The PROG pin must make a high-to-low transition in order to exit from the power on mode. The power on sequence is initiated any time V_{CC} drops below 1V. The table below shows how the 4-bit nibbles on Port 2 correspond to the μPD82C43 operations.

Port Address			Op-Code		
P_{21}	P_{20}	Address Code	P_{23}	P_{22}	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

For example an 0010 appearing on P_{20}-P_{23}, respectively, would result in a Write to Port 4.

Read Mode

There is one Read mode in the μPD82C43. A falling edge on the PROG pin latches the op-code and port address from input port 2. The port address and Read operation are then decoded causing the appropriate outputs to be tri-stated and the input buffers switched on. The rising edge of PROG terminates the Read operation. The port (4, 5, 6, or 7) that was selected by the port address (P_{21}-P_{20}) is returned to the tri-state mode, and port 2 is switched to the input mode.

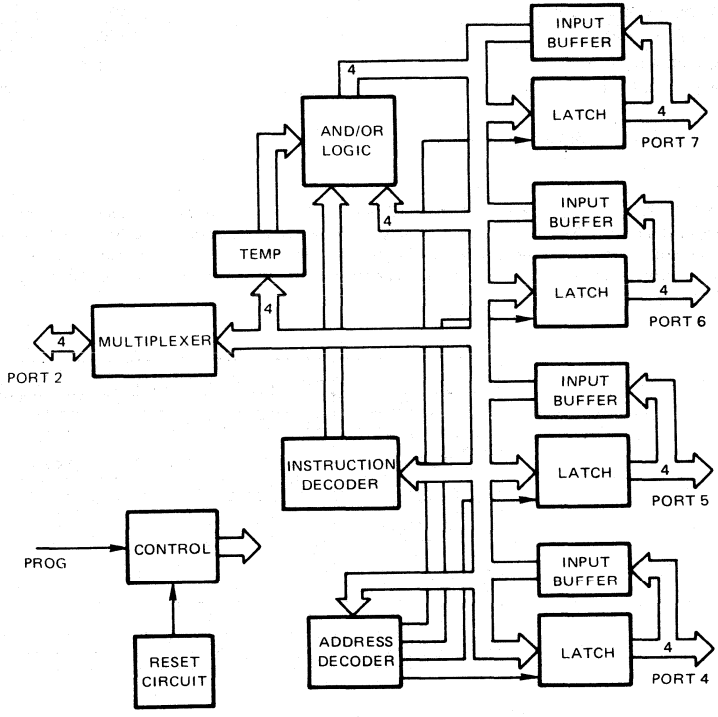
Generally, in the read mode, a port will be an input and in the write mode it will be an output. If during program operation, the μPD82C43's modes are changed, the first read pulse immediately following a write should be ignored. The subsequent read signals are valid. Reading a port will then force that port to a high impedance state.

Write Modes

There are three write modes in the μPD82C43. The MOVD P_p,A instruction from the μPD8048/80C48 family writes the new data directly to the specified port (4, 5, 6, or 7). The old data previously latched at that port is lost. The ORLD Pp,A instruction performs a logical OR between the new data and the data currently latched at the selected port. The result is then latched at that port. The final write mode uses the ANLD Pp,A instruction. It performs a logical AND between the new data and the data currently latched at the specified port. The result is latched at that port.

The data remains latched at the selected port following the logical manipulation until new data is written to that port.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
2-5 1, 21-23 17-20 13-16	P_{40}-P_{43} P_{50}-P_{53} P_{60}-P_{63} P_{70}-P_{73}	The four 4-bit static bi-directional I/O ports. They are programmable into the following modes: input mode (during a Read operation); low impedance latched output mode (after a Write operation); and the tri-state mode (following a Read operation). Data appearing on I/O lines P_{20}-P_{23} can be written directly. That data can also be logically ANDed or ORed with the previous data on those lines.
6	$\overline{CS}$	Chip Select input (active-low). When the μPD82C43 is deselected (CS = 1), output or internal status changes are inhibited.
7	PROG	Clock input pin. The control and address information are present on port lines P_{20}-P_{23} when PROG makes a high-to-low transition. Data is present on port lines P_{20}-P_{23} when PROG makes a low-to-high transition.
8-11	P_{20}-P_{23}	P_{20}-P_{23} form a 4-bit bi-directional port. Refer to PROG function for contents of P_{20}-P_{23} at the rising and falling edges of PROG. Data from a selected port is present on P_{20}-P_{23} prior to the rising edge of PROG if during a Read operation.
12	GND	The μPD8041/8741 ground potential.
24	V_{CC}	+5 volt supply.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	-0.5 to +7 Volts①
Power Dissipation	1 W

Note: ① With respect to ground.

*T_a = 25°C

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = -40°C to +85°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input High Voltage	V_{IH}	V_{CC} - 2.0		V_{CC}	V	
Output Low Voltage (Ports 4-7)	V_{OL1}			0.45	V	I_{OL} = 5 mA ①
Output Low Voltage (Port 7)	V_{OL2}			1	V	I_{OL}=20 mA
Output Low Voltage (Port 2)	V_{OL3}			0.45	V	I_{OL} = 0.6 mA
Output High Voltage (Ports 4-7)	V_{OH1}	V_{CC} - 0.5			V	I_{OH} = 240 μA
Output High Voltage (Port 2)	V_{OH2}	V_{CC} - 0.5			V	I_{OH} = 100 μA
Sum of All I_{OL} From 16 Outputs	I_{OL}			80	mA	5 mA Each Pin
Input Leakage Current (Ports 4-7)	I_{IL1}	-1		+1	μA	V_{IN} = V_{CC} to 0V
Input Leakage Current (Port 2, $\overline{CS}$, PROG)	I_{IL2}	-1		+1	μA	V_{IN} = V_{CC} to 0V
V_{CC} Supply Current	I_{CC1}			300	μA	
Power Down Supply Current	I_{CC2}			10	μA	

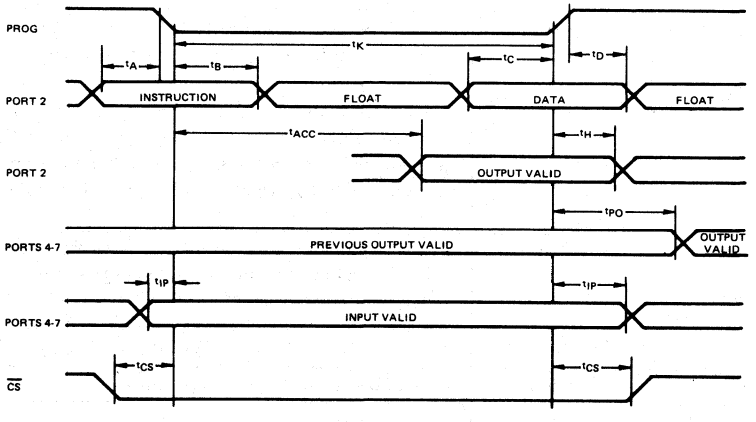
Note: ① Refer to graph of additional sink current drive.

AC CHARACTERISTICS

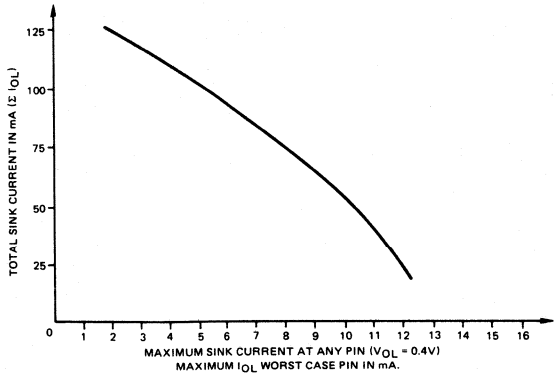
T_a = -40°C to + 85°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Code Valid Before PROG	t_A	100			ns	80 pF Load
Code Valid After PROG	t_B	60			ns	20 pF Load
Data Valid Before PROG	t_C	200			ns	80 pF Load
Data Valid After PROG	t_D	20			ns	20 pF Load
Port 2 Floating After PROG	t_H	0		150	ns	20 pF Load
PROG Negative Pulse Width	t_K	900			ns	
Ports 4-7 Valid After PROG	t_{PO}			700	ns	100 pF Load
Ports 4-7 Valid Before/After PROG	t_{LP1}	100			ns	
Port 2 Valid After PROG	t_{ACC}			750	ns	80 pF Load
$\overline{CS}$ Valid Before/After PROG	$t_{\overline{CS}}$	50			ns	

TIMING WAVEFORMS

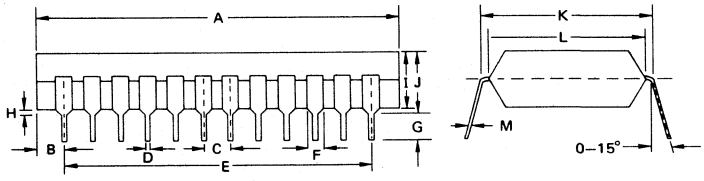


CURRENT SINKING CAPABILITY ①



Note: ① This curve plots the guaranteed worst case current sinking capability of any I/O port line versus the total sink current of all pins. The μPD82C43 is capable of sinking 5 mA (for V_{OL} = 0.4V) through each of the 16 I/O lines simultaneously. The current sinking curve shows how the individual I/O line drive increases if all the I/O lines are not fully loaded.

PACKAGE OUTLINE μPD82C43



PLASTIC

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

9

PROGRAMMABLE COMMUNICATION INTERFACES

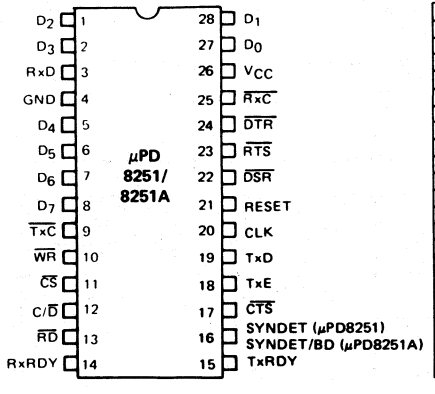
DESCRIPTION

The μPD8251 and μPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters (USARTs) are designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the 8080A or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - Five 8-Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
    - Automatic Break Detect and Handling (μPD8251A)
  - Synchronous:
    - Five 8-Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate (1X Mode) – DC to 56K Baud (μPD8251)
  – DC to 64K Baud (μPD8251A)
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080A/8085/μPD780 (Z80™)
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply, ± 10% (8251A) ± 5% (8251)
- Separate Device Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8 bits)
C/$\overline{D}$	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock (TTL)
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
SYNDET/BD	Sync Detect/Break Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

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TM: Z80 is a registered trademark of Zilog, Inc.

FUNCTIONAL DESCRIPTION

The μPD8251 and μPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters are designed specifically for 8080 microcomputer systems but work with most 8-bit processors. Operation of the μPD8251 and μPD8251A, like other I/O devices in the 8080 family, are programmed by system software for maximum flexibility.

In the receive mode, the μPD8251 or μPD8251A converts incoming serial format data into parallel data and makes certain format checks. In the transmit mode, it formats parallel data into serial form. The device also supplies or removes characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

μPD8251A FEATURES AND ENHANCEMENTS

The μPD8251A is an advanced design of the industry standard 8251 USART. It operates with a wide range of microprocessors, including the 8080, 8085, and μPD780 (Z80™). The additional features and enhancements of the μPD8251A over the μPD8251 are listed below.

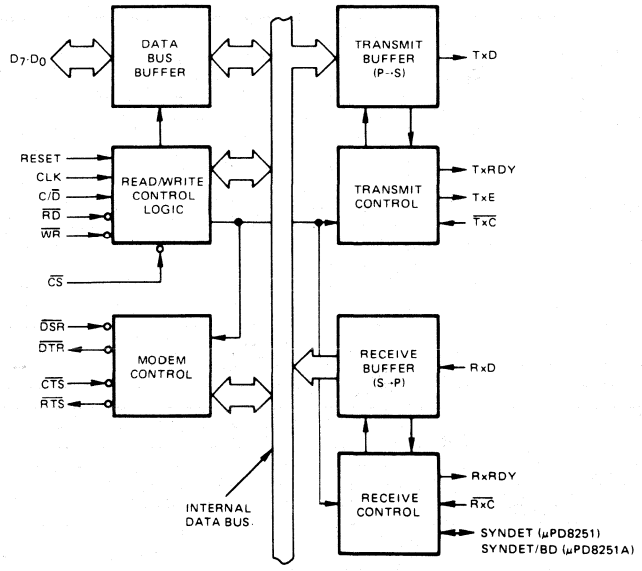
1. The data paths are double-buffered with separate I/O registers for control, status, Data In and Data Out. This feature simplifies control programming and minimizes processor overhead.
2. The Receiver detects and handles "break" automatically in asynchronous operations, which relieves the processor of this task.
3. The Receiver is prevented from starting when in "break" state by a refined Rx initialization. This also prevents a disconnected USART from causing unwanted interrupts.
4. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed.
5. The Tx Disable command is prevented from halting transmission by the Tx Enable Logic enhancement, until all data previously written has been transmitted. The same logic also prevents the transmitter from turning off in the middle of a word.
6. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through a flip-flop which clears itself upon a status read.
7. The possibility of a false sync detect is minimized by:
   - ensuring that if a double sync character is programmed, the characters be contiguously detected.
   - clearing the Rx register to all Logic 1s (V_{OH}) whenever the Enter Hunt command is issued in Sync mode.
8. The $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device as long as the μPD8251A is not selected.
9. The μPD8251A Status can be read at any time, however, the status update will be inhibited during status read.
10. The μPD8251A has enhanced AC and DC characteristics and is free from extraneous glitches, providing higher speed and improved operating margins.
11. Baud rate from DC to 64K.

BASIC OPERATION

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	μPD8251/μPD8251A → Data Bus
0	1	0	0	Data Bus → μPD8251/μPD8251A
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

™: Z80 is a registered trademark of Zilog, Inc.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltages	-0.5 to +7 Volts

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 10\%$ for 8251A and $\pm 5\%$ for 8251; GND = 0V.

PARAMETER	SYMBOL	LIMITS μPD8251 MIN	μPD8251 TYP	μPD8251 MAX	μPD8251A MIN	μPD8251A MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	0.5	0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	2.2	V_{CC}	V	
Output Low Voltage	V_{OL}			0.45		0.45	V	μPD8251: I_{OL} = 1.7 mA μPD8251A: I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			2.4		V	μPD8251: I_{OH} = -100 μA μPD8251A: I_{OH} = -400 μA
Data Bus Leakage	I_{DL}			-50		-10	μA	V_{OUT} = 0.45V
				10		10		$V_{OUT} = V_{CC}$
Input Load Current	I_{IL}			10		10	μA	At 5.5V
Power Supply Current	I_{CC}		45	80		100	mA	μPD8251A: All Outputs = Logic 1

CAPACITANCE

$T_a = 25°C$; $V_{CC} = GND = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 10% for 8251A; GND = 0V; V_{CC} = 5.0V ± 5% for 8251

PARAMETER	SYMBOL	LIMITS μPD8251 MIN	LIMITS μPD8251 MAX	LIMITS μPD8251A MIN	LIMITS μPD8251A MAX	UNIT	TEST CONDITIONS
READ							
Address Stable before $\overline{READ}$, ($\overline{CS}$, $\overline{C/D}$)	t_{AR}	50		50		ns	
Address Hold Time for $\overline{READ}$, ($\overline{CS}$, $\overline{C/D}$)	t_{RA}	5		50		ns	
$\overline{READ}$ Pulse Width	t_{RR}	430		250		ns	
Data Delay from $\overline{READ}$	t_{RD}		350		250	ns	μPD8251: C_L = 100 pF μPD8251A: C_L = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	25	200	10	100	ns	μPD8251 C_L = 100 pF C_L = 15 pF
WRITE							
Address Stable before $\overline{WRITE}$	t_{AW}	20		50		ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20		50		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		250		ns	
Data Set-Up Time for $\overline{WRITE}$	t_{DW}	200		150		ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40		30		ns	
Recovery Time Between WRITES ②	t_{RV}	6		6		t_{CY}	
OTHER TIMING							
Clock Period ③	t_{CY}	0.420	1.35	0.32	1.35	μs	
Clock Pulse Width High	$t_{\phi W}$	220	0.7t_{CY}	140	t_{CY}-90	ns	
Clock Pulse Width Low	$t_{\phi W}$			90		ns	
Clock Rise and Fall Time	$t_{R,tF}$	0	50	5	20	ns	
TxD Delay from Falling Edge of TxC	t_{DTx}		1		1	μs	
Rx Data Set-Up Time to Sampling Pulse	t_{SRx}	2		2		μs	μPD8251: C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2		2		μs	
Transmitter Input Clock Frequency 1X Baud Rate 16X Baud Rate 64X Baud Rate	f_{Tx}	DC DC DC	56 520 520		64 310 615	kHz kHz kHz	
Transmitter Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{TPW}	12 1		12 1		t_{CY} t_{CY}	
Transmitter Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{TPD}	15 3		15 3		t_{CY} t_{CY}	
Receiver Input Clock Frequency 1X Baud Rate 16X Baud Rate 64X Baud Rate	f_{Rx}	DC DC DC	56 520 520		64 310 615	kHz kHz kHz	
Receiver Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{RPW}	12 1		12 1		t_{CY} t_{CY}	
Receiver Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{RPD}	15 3		15 3		t_{CY} t_{CY}	
TxRDY Delay from Center of Data Bit	t_{Tx}		16		8	t_{CY}	μPD8251: C_L = 50 pF
RxRDY Delay from Center of Data Bit Internal SYNDET Delay from Center of Data Bit	t_{RX} t_{IS}		20 25		24 24	t_{CY} t_{CY}	
External SYNDET Set-Up Time before Falling Edge of RxC	t_{ES}	16		16		t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}		16		20	t_{CY}	μPD8251: C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}		16		8	t_{CY}	
Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	16		20		t_{CY}	

Notes: ① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.

② This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

③ The TxC and RxC frequencies have the following limitations with respect to CLK.
For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
For 16X and 64X Baud Rate, f_{TX} or $f_{Rx} \leq 1/(4.5\ t_{CY})$

④ Reset Pulse Width = 6 t_{CY} minimum.

⑤ $T_{TXRDYCCR}$ -2T_{CY} + T_ϕ + T_R + 200ns

⑥ $T_{RXRDYCLR}$ -2T_{CY} + T_ϕ + T_R + 170ns

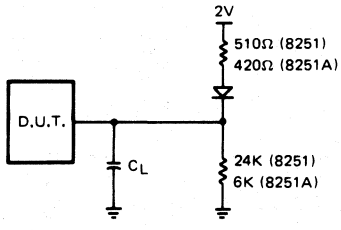
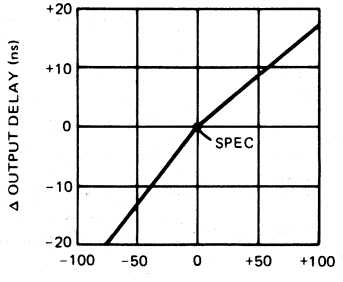


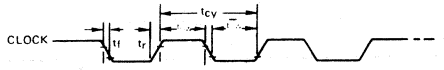
Figure 1.



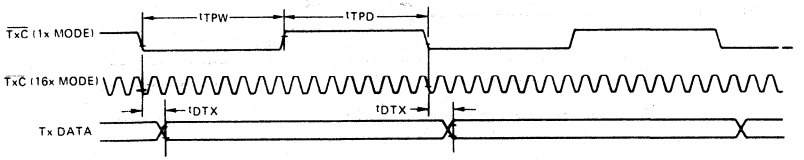
Typical Δ Output Delay Versus Δ Capacitance (pF)

TEST LOAD CIRCUIT

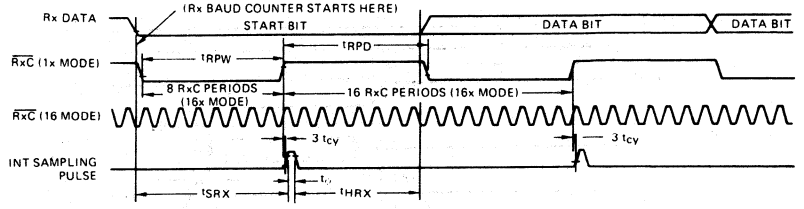
TIMING WAVEFORMS



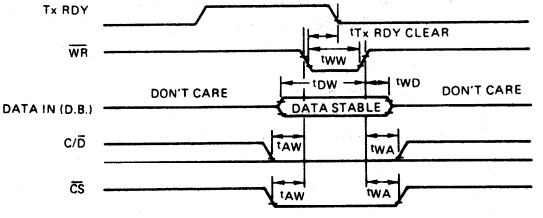
SYSTEM CLOCK INPUT



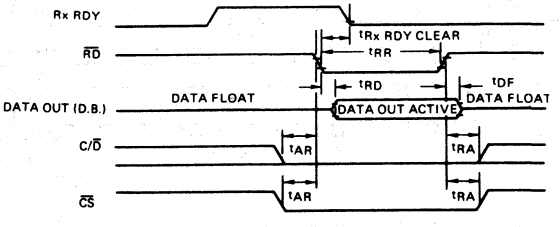
TRANSMITTER CLOCK AND DATA



RECEIVER CLOCK AND DATA



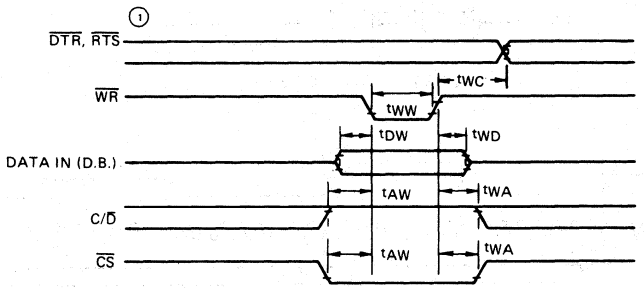
WRITE DATA CYCLE (PROCESSOR → USART)



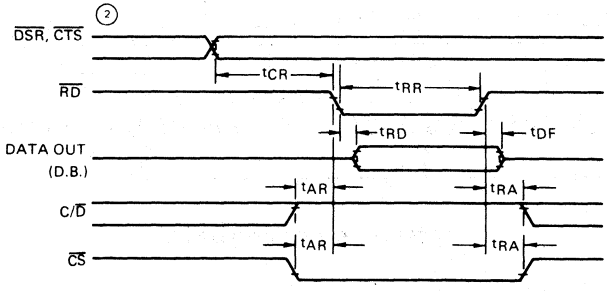
READ DATA CYCLE (PROCESSOR ← USART)

9

TIMING WAVEFORMS
(CONT.)



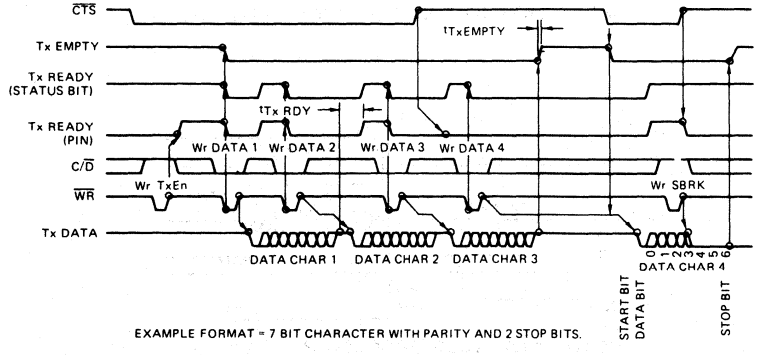
WRITE CONTROL OR OUTPUT PORT CYCLE
(PROCESSOR → USART)



READ CONTROL OR INPUT PORT CYCLE
(PROCESSOR ← USART)

NOTES: ① T_{WC} includes the response timing of a control byte.

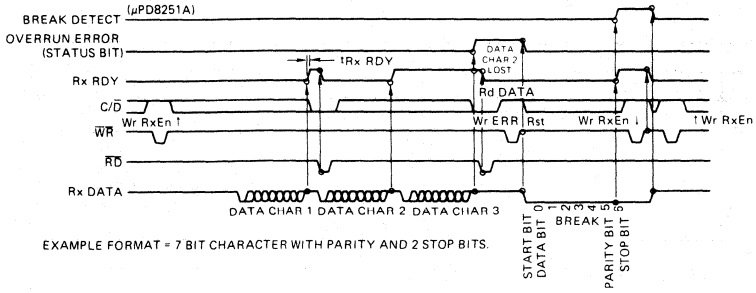
② T_{CR} includes the effect of CTS on the TxENBL circuitry



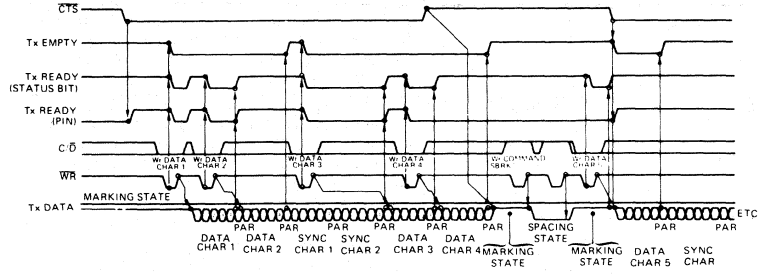
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY AND 2 STOP BITS.

TRANSMITTER CONTROL AND FLAG TIMING
(ASYNC MODE)

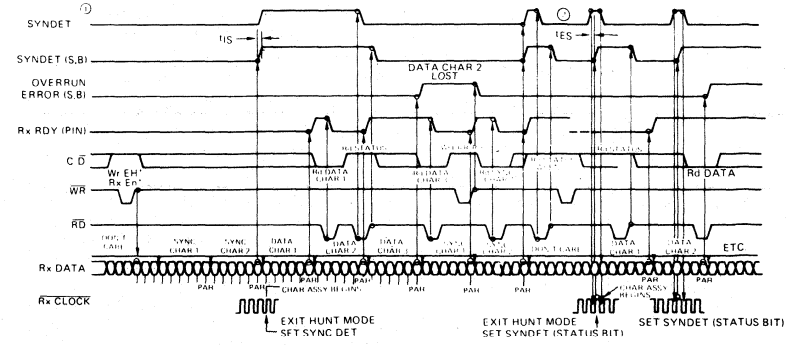
TIMING WAVEFORMS (CONT.)



RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)

Notes: ① Internal sync, 2 sync characters, 5 bits, with parity.
② External sync, 5 bits, with parity.

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PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the USART to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/ Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/ Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is 6 t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be at least 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the USART to accept the data or control word which the processor is writing out on the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the USART to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART to read from or write to the processor.
Modem Control			The μPD8251 and μPD8251A have a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

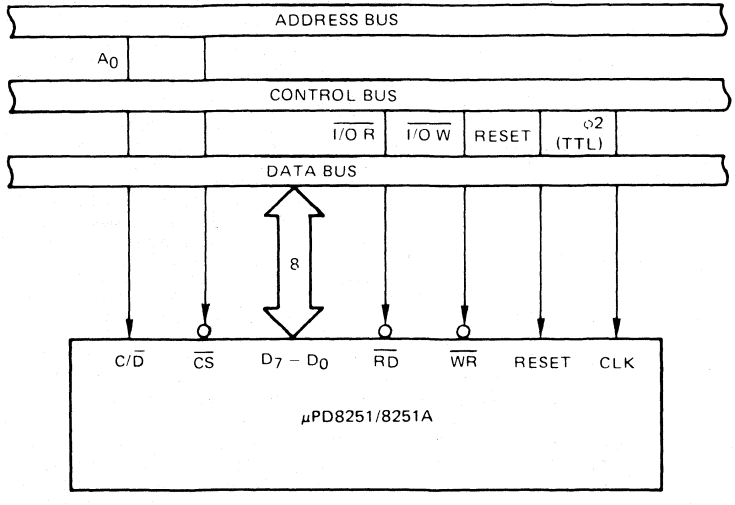
TRANSMIT BUFFER

The Transmit Buffer receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD pin.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for polled operation. Loading a character from the processor automatically resets TxRDY, on the leading edge.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

μPD8251 AND μPD8251A INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVE BUFFER

The Receive Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 and μPD8251A set the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock determines the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1.16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 and μPD8251A on the rising edge of $\overline{RxC}$. ①
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET (μPD8251)	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.
16	SYNDET/BD (μPD8251A)	Sync Detect/ Break Detect	The SYNDET/BD pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the Break Detect output will go high which all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx data returns to a logic one state or upon chip reset. The state of Break Detect can be read as a status bit.

Note: ① Since the μPD8251 and μPD8251A will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):
$\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
$\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)
$\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)

If the Baud Rate equals 300:
$\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
$\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
$\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 and μPD8251A to define the desired mode and communications format. The control words will specify the BAUD rate factor (1x, 16x, 64x), character length (5 to 8), number of STOP bits (1, 1-1/2, 2) Asynchronous or Synchronous mode, SYNDET (IN or OUT), parity, etc.

After receiving the control words, the μPD8251 and μPD8251A are ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 and μPD8251A may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 and μPD8251A may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 and μPD8251A cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new control words.

USART PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A RESET (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the μPD8251 and μPD8251A.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

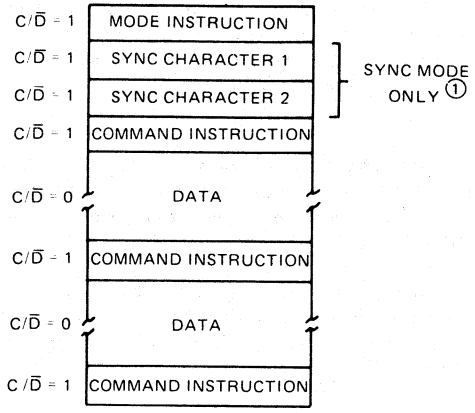
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the Synchronous or Asynchronous mode, BAUD rate factor, character length, parity, and number of stop bits. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE (1) The second SYNC character is skipped if MODE instruction has programmed the μPD8251 and μPD8251A to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the μPD8251 and μPD8251A to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 and μPD8251A can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components (one asynchronous and the other synchronous) which share the same support circuits and package. Although the format definition can be changed at will or "on the fly," the two modes will be explained separately for clarity.

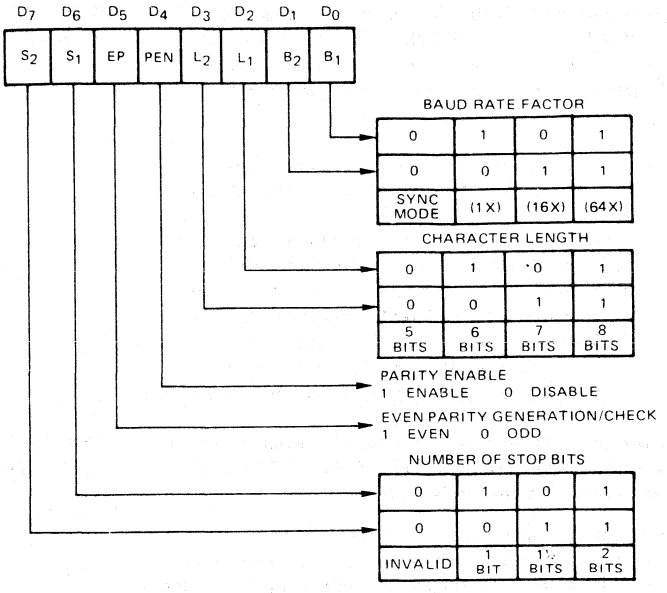
ASYNCHRONOUS TRANSMISSION

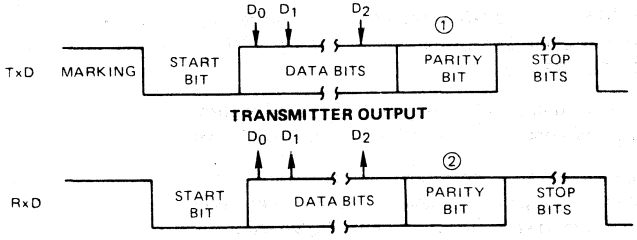
When a data character is written into the μPD8251 and μPD8251A, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}/16$ or $\overline{TxC}/64$, as defined by the Mode Instruction.

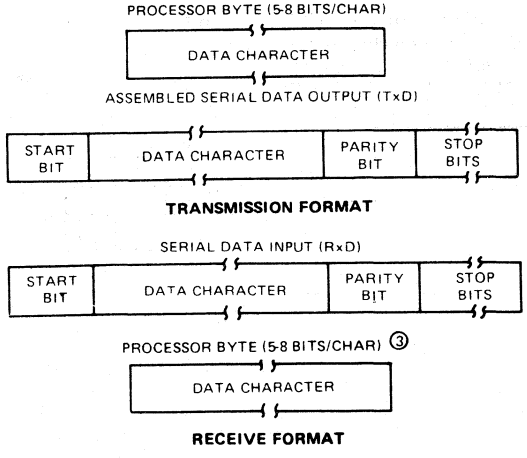
If no data characters have been loaded into the μPD8251 and μPD8251A, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and μPD8251A and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.







Notes: ① Generated by μPD8251/8251A
② Does not appear on the Data Bus.
③ If character length is defined as 5, 6, or 7 bits, the unused bits are set to "zero."

SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 and μPD8251A receive the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 and μPD8251A Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 and μPD8251A become empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

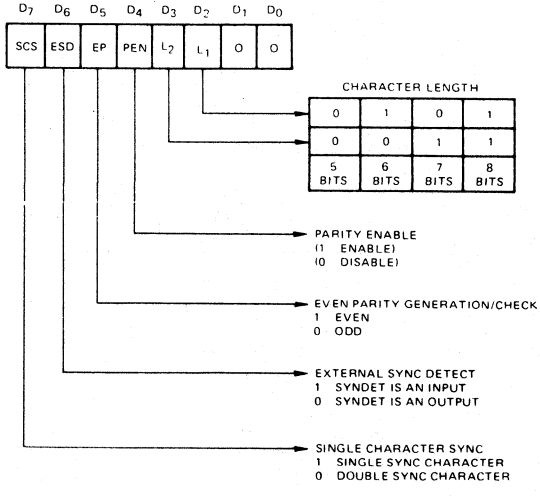
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receive Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 and μPD8251A leave the HUNT mode and are in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

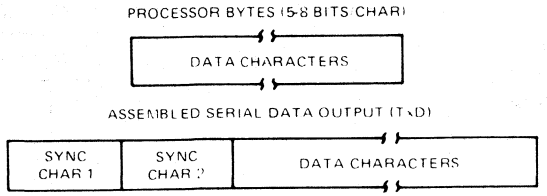
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

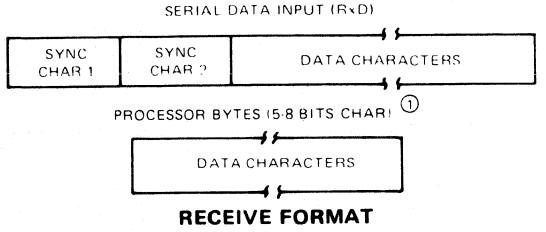
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

Note: ① If character length is defined as 5, 6 or 7 bits, the unused bits are set to "zero."

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 and μPD8251A has been specified by the Mode Instruction and the SYNC character(s) have been entered (if in SYNC mode), the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s) (as needed) are loaded, all subsequent "control writes" ($C/\overline{D}$ = 1) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 and μPD8251A to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the status of an active interface device to determine if errors have occurred or if there are other conditions which require a response from the processor. The μPD8251 and μPD8251A have features which allow the processor to read the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 and μPD8251A to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of 16 clock periods in the μPD8251 and 28 clock periods in the μPD8251A.

PARITY ERROR

When a parity error is detected, the PE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

If the processor fails to read a data character before the one following is available, the OE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

If a valid STOP bit is not detected at the end of a character, the FE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

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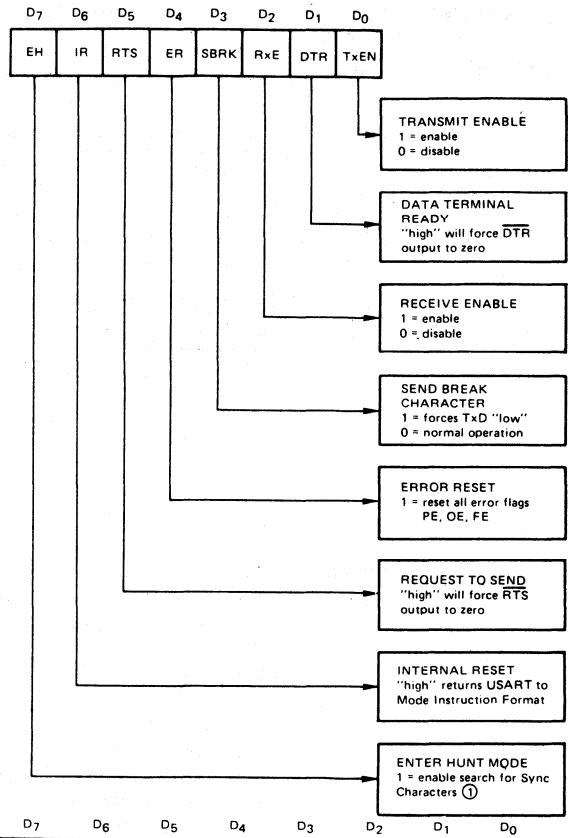
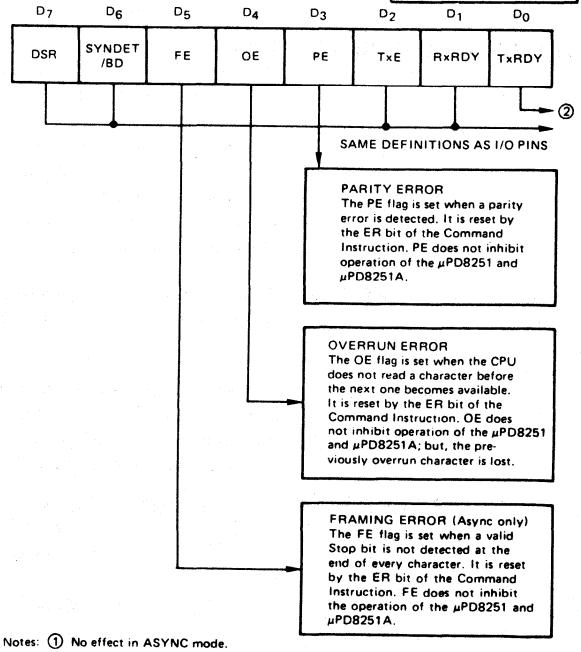
COMMAND INSTRUCTION FORMAT



STATUS READ FORMAT



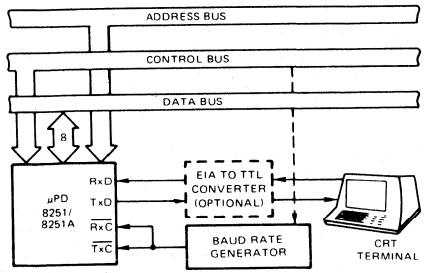
Notes: ① No effect in ASYNC mode.

② TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

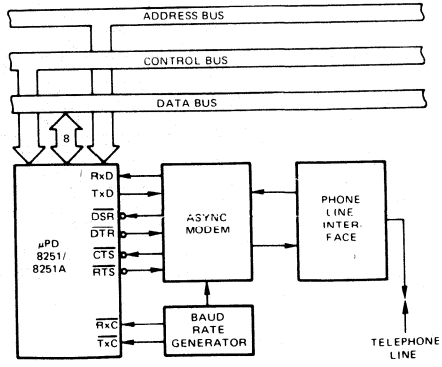
TxRDY status bit = DB Buffer Empty

TxRDY (pin 15) = DB Buffer Empty • $\overline{CTS}$ • TxEn

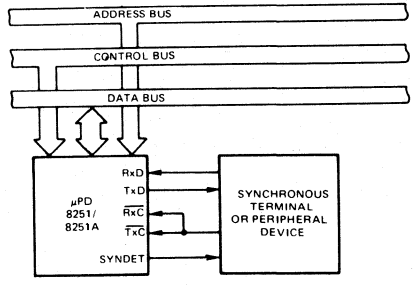
APPLICATION OF THE μPD8251 AND μPD8251A



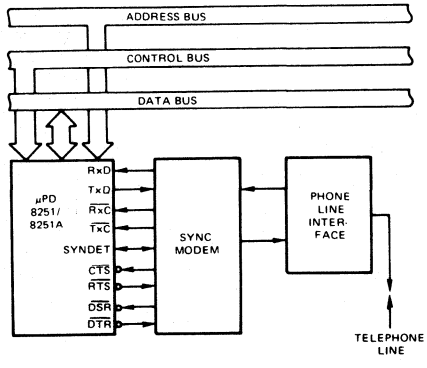
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



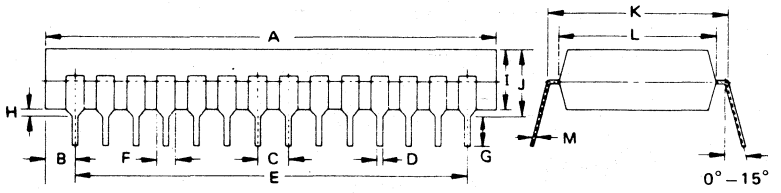
SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

9

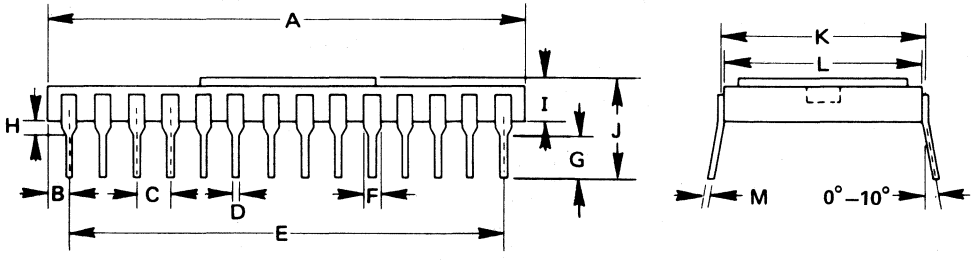
PACKAGE OUTLINES
μPD8251C
μPD8251AC



Plastic

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

μPD8251D
μPD8251AD



Ceramic

ITEM	MILLIMETERS	INCHES
A	36.2 MAX.	1.43 MAX.
B	1.59 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.46 ± 0.01	0.02 ± 0.004
E	33.02 ± 0.1	1.3 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.002

PROGRAMMABLE INTERVAL TIMER

DESCRIPTION

The NEC μPD8253-5 contains three independent, programmable, multi-modal 16-bit counter/timers. It is designed as a general purpose device, fully compatible with the 8080 family. The μPD8253-5 interfaces directly to the busses of the processor as an array of I/O ports.

The μPD8253-5 can generate accurate time delays under the control of system software. The three independent 16-bit counters can be clocked at rates from DC to 4 MHz. The system software controls the loading and starting of the counters to provide accurate multiple time delays. The counter output flags the processor at the completion of the time-out cycles.

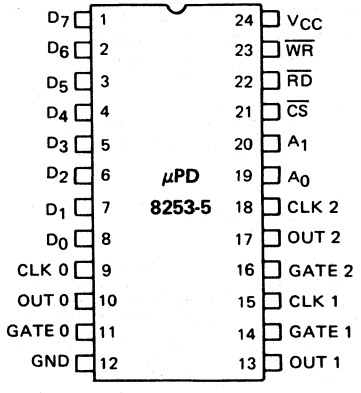
System overhead is greatly improved by relieving the software from the maintenance of timing loops. Some other common uses for the μPD8253-5 in microprocessor based systems are:

- Programmable Baud Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller
- NEC Now Supplies μPD8253-5 to all μPD8253 Requirements

FEATURES

- Three Independent 16-Bit Counters
- Clock Rate: DC to 4 MHz
- Count Binary or BCD
- Single +5 Volt Supply, ±10%
- 24 Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8-Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0, A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

9

FUNCTIONAL DESCRIPTION

Data Bus Buffer

The 3-state, 8-bit, bi-directional Data Bus Buffer interfaces the μPD8253-5 to the 8080AF/8085A microprocessor system. It will transmit or receive data in accordance with the INput or OUTput instructions executed by the processor. There are three basic functions of the Data Bus Buffer.

1. Program the modes of the μPD8253-5.
2. Load the count registers.
3. Read the count values.

Read/Write Logic

The Read/Write Logic controls the overall operation of the μPD8253-5 and is governed by inputs received from the processor system bus.

Control Word Register

Two bits from the address bus of the processor, A_0 and A_1, select the Control Word Register when both are at a logic "1" (active-high logic). When selected, the Control Word Register stores data from the Data Bus Buffer in a register. This data is then used to control:

1. The operational MODE of the counters.
2. The selection of BCD or Binary counting.
3. The loading of the count registers.

$\overline{RD}$ (Read)

This active-low signal instructs the μPD8253-5 to transmit the selected counter value to the processor.

$\overline{WR}$ (Write)

This active-low signal instructs the μPD8253-5 to receive MODE information or counter input data from the processor.

A_1, A_0

The A_1 and A_0 inputs are normally connected to the address bus of the processor. They control the one-of-three counter selection and address the control word register to select one of the six operational MODES.

$\overline{CS}$ (Chip Select)

The μPD8253-5 is enabled when an active-low signal is applied to this input. Reading or writing from this device is inhibited when the chip is disabled. The counter operation, however, is not affected.

Counters #0, #1, #2

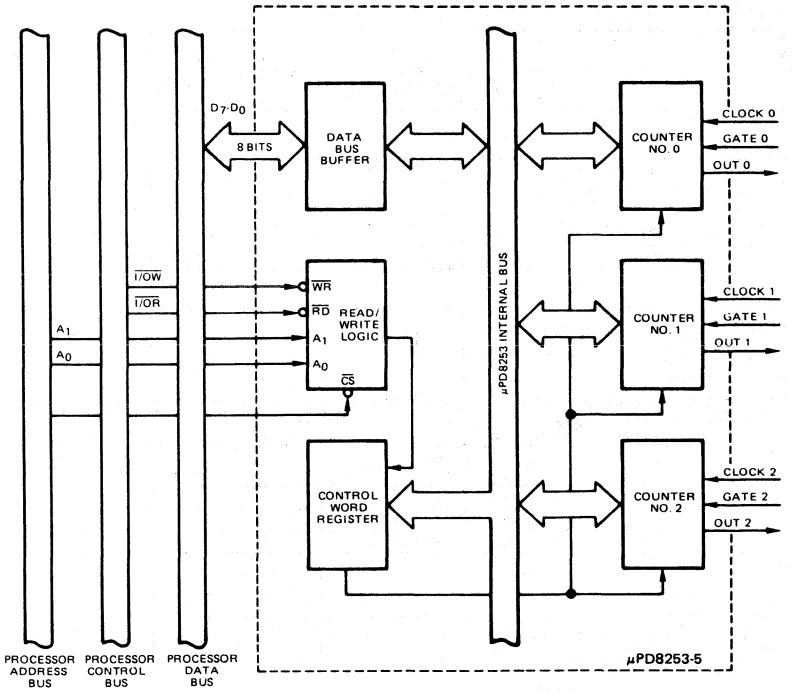
The three identical, 16-bit down counters are functionally independent allowing for separate MODE configuration and counting operation. They function as Binary or BCD counters with their gate, input and output line configuration determined by the operational MODE data stored in the Control Word Register. The system software overhead time can be reduced by allowing the control word to govern the loading of the count data.

The programmer, with READ operations, has access to each counter's contents. The μPD8253-5 contains the commands and logic to read each counter's contents while still counting without disturbing its operation.

The following is a table showing how the counters are manipulated by the input signals to the Read/Write Logic.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	FUNCTION
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation, 3-State
1	X	X	X	X	Disable, 3-State
0	1	1	X	X	No-Operation, 3-State

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts (1)

Note: (1) With respect to ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{IL}			±10	μA	$V_{IN} = V_{CC}$ to 0 V
Output Float Leakage Current	I_{OFL}			±10	μA	$V_{OUT} = V_{CC}$ to 0 V
V_{CC} Supply Current	I_{CC}			140	mA	

CAPACITANCE

$T_a = 25°C$; $V_{CC} = GND = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Input/Output Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}.

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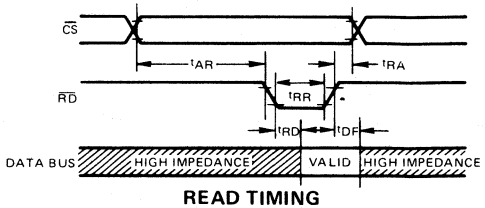
AC CHARACTERISTICS ①

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; GND = 0V

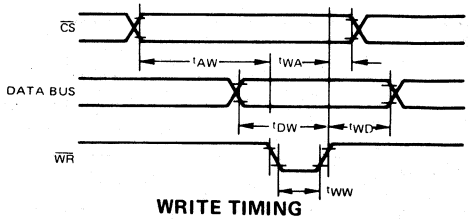
PARAMETER	SYMBOL	LIMITS μPD8253-5 MIN	LIMITS μPD8253-5 TYP	LIMITS μPD8253-5 MAX	UNIT	TEST CONDITIONS
READ						
Address Stable Before $\overline{READ}$	t_{AR}	0			ns	
Address Hold Time for $\overline{READ}$	t_{RA}	0			ns	
$\overline{READ}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{READ}$	t_{RD}			170	ns	CL = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	25		100	ns	CL = 150 pF
WRITE						
Address Stable Before $\overline{WRITE}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	0			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	250			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	0			ns	
Recovery Time Between $\overline{WRITES}$	t_{RV}	1			μs	
CLOCK AND GATE TIMING						
Clock Period	t_{CLK}	250		DC	ns	
High Pulse Width	t_{PWH}	160			ns	
Low Pulse Width	t_{PWL}	90			ns	
Gate Pulse Width High	t_{GW}	150			ns	
Gate Set Up Time to Clock ↑	t_{GS}	100			ns	
Gate Hold Time After Clock ↑	t_{GH}	50			ns	
Low Gate Width	t_{GL}	100			ns	
Output Delay from Clock ↓	t_{OD}			300	ns	CL = 150 pF
Output Delay from Gate	t_{ODG}			300	ns	CL = 150 pF

Note: ① AC Timing Measured at V_{OH} = 2.2V; V_{OL} = 0.8V.

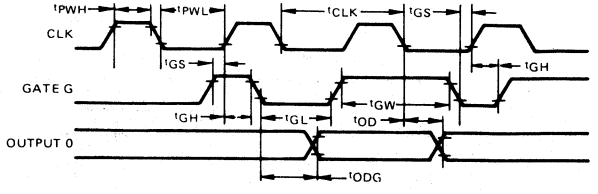
TIMING WAVEFORMS



READ TIMING



WRITE TIMING



CLOCK AND GATE TIMING

PROGRAMMING THE μPD8253-5

The programmer can select any of the six operational MODES for the counters using system software. Individual counter programming is accomplished by loading the CONTROL WORD REGISTER with the appropriate control word data (A_0, A_1 = 11).

CONTROL WORD FORMAT

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

SC – Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Invalid

RL – Read/Load

RL1	RL0	
0	0	Counter Latching Operation
1	0	Read/Load Most Significant Byte Only
0	1	Read/Load Least Significant Byte Only
1	1	Read/Load Least Significant Byte First, Then Most Significant Byte

BCD

0	Binary Counter, 16-Bits
1	BCD Counter, 4-Decades

M-Mode

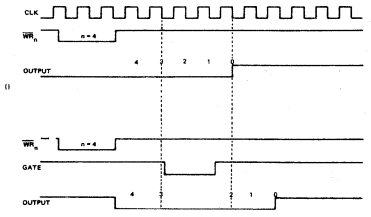
M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

OPERATIONAL MODES ①

Each of the three counters can be individually programmed with different operating MODES by appropriately formatted Control Words. The following is a summary of the MODE operations.

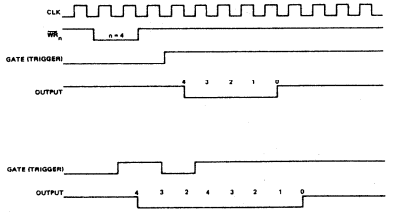
Mode 0: Interrupt on Terminal Count

The initial MODE set operation forces the OUTPUT low. When the specified counter is loaded with the count value, it will begin counting. The OUTPUT will remain low until the terminal count sets it high. It will remain in the high state until the trailing edge of the second $\overline{WR}$ pulse loads in COUNT data. If data is loaded during the counting process, the first $\overline{WR}$ stops the count. Counting starts with the new count data triggered by the falling clock edge after the second $\overline{WR}$. If a GATE pulse is asserted while counting, the count is terminated for the duration of GATE. The falling edge of CLK following the removal of GATE restarts counting from the terminated point.



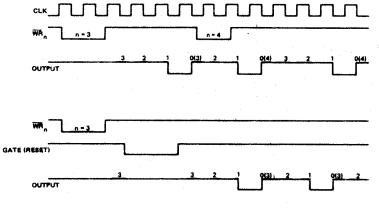
Mode 1: Programmable One-Shot

The OUTPUT is set low by the falling edge of CLOCK following the trailing edge of GATE. The OUTPUT is set high again at the terminal count. The output pulse is not affected if new count data is loaded while the OUTPUT is low. The new data will be loaded on the rising edge of the next trigger pulse. The assertion of a trigger pulse while OUTPUT is low, resets and retriggers the One-Shot. The OUTPUT will remain low for the full count value after the rising edge of TRIGGER.



Mode 2: Rate Generator

The RATE GENERATOR is a variable modulus counter. The OUTPUT goes low for one full CLOCK period as shown in following timing diagram. The count data sets the time between OUTPUT pulses. If the count register is reloaded between output pulses the present period will not be affected. The subsequent period will reflect the new value. The OUTPUT will remain high for the duration of the asserted GATE input. Normal operation resumes on the falling CLOCK edge following the rising edge of GATE.



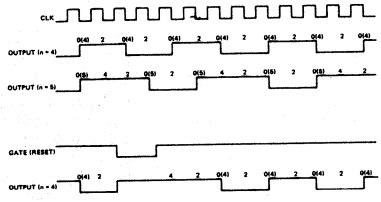
Note: ① All internal counter events occur at the falling edge of the associated clock in all modes of operation.

OPERATIONAL MODES (Cont.)

Mode 3: Square Wave Generator

MODE 3 resembles MODE 2 except the OUTPUT will be high for half of the count and low for the other half (for even values of data). For odd values of count data the OUTPUT will be high one clock cycle longer than when it is low (High Period → $\frac{N+1}{2}$ clock cycles; Low Period → $\frac{N-1}{2}$ clock periods, where N is the decimal value of count data). If the count register is reloaded with a new value during counting, the new value will be reflected immediately after the output transition of the current count.

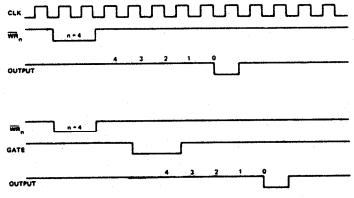
The OUTPUT will be held in the high state while GATE is asserted. Counting will start from the full count data after the GATE has been removed.



Mode 4: Software Triggered Strobe

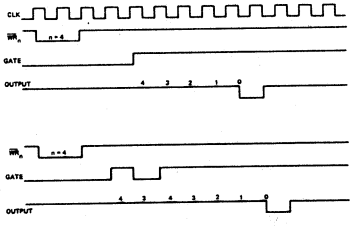
The OUTPUT goes high when MODE 4 is set, and counting begins after the second byte of data has been loaded. When the terminal count is reached, the OUTPUT will pulse low for one clock period. Changes in count data are reflected in the OUTPUT as soon as the new data has been loaded into the count registers. During the loading of new data, the OUTPUT is held high and counting is inhibited.

The OUTPUT is held high for the duration of GATE. The counters are reset and counting begins from the full data value after GATE is removed.



Mode 5: Hardware Triggered Strobe

Loading MODE 5 sets OUTPUT high. Counting begins when count data is loaded and GATE goes high. After terminal count is reached, the OUTPUT will pulse low for one clock period. Subsequent trigger pulses will restart the counting sequence with the OUTPUT pulsing low on terminal count following the last rising edge of the trigger input (Reference bottom half of timing diagram).



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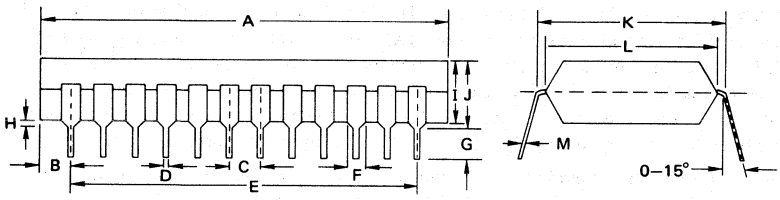
PACKAGE OUTLINE
μPD8253-5C



Plastic

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

PROGRAMMABLE PERIPHERAL INTERFACES

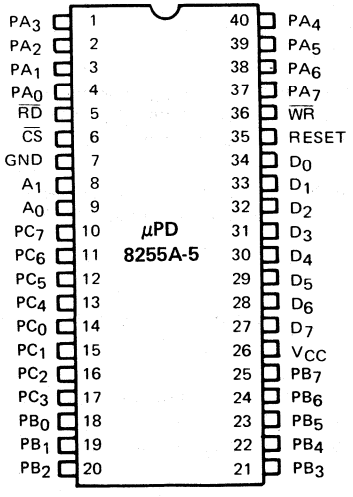
DESCRIPTION

The μPD8255A-5 is a general purpose programmable INPUT/OUTPUT device designed for use with the 8080A/8085A microprocessors. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bi-directional Bus mode, (MODE 2), uses the 8 lines of Port A for a bi-directional bus, and five lines from Port C for bus control signals. The μPD8255A-5 is packaged in 40-pin plastic dual-in-line packages.

FEATURES

- Fully Compatible with the 8080A/8085 Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 4 mA Darlington Drive Outputs for Printers and Displays
- LSI Drastically Reduces System Package Count
- Standard 40-Pin Dual-In-Line Plastic and Ceramic Packages

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

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FUNCTIONAL DESCRIPTION

General

The μPD8255A-5 Programmable Peripheral Interface (PPI) is designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the μPD8255A-5. The μPD8255A-5 is functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, 8-bit Data Bus Buffer (D_0-D_7) of the μPD8255A-5 can be directly interfaced to the processor's system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255A-5 for communication with the 8080A/8085A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255A-5 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9

Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255A-5. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C (PC_7-PC_4)
Group II – Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents cannot be read back to the processor.

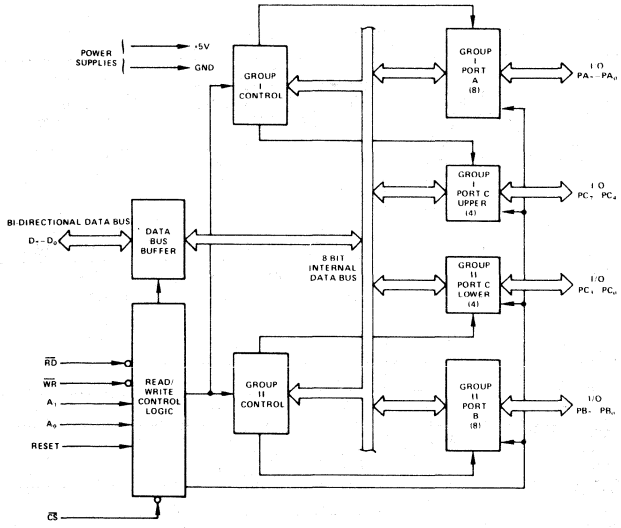
Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255A-5 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255A-5 are further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.
Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with Ports A and B.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output Voltages ①	-0.5 to +7 Volts
All Input Voltages ①	-0.5 to +7 Volts
Supply Voltages ①	-0.5 to +7 Volts

Note: ① With respect to V_{SS}

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS μPD8255A-5 MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	②
Output High Voltage	V_{OH}	2.4			V	③
Darlington Drive Current	I_{OH} ①	-1		-4	mA	$V_{OH} = 1.5V$, $R_{EXT} = 750\Omega$
Power Supply Current	I_{CC}			120	mA	$V_{CC} = +5V$, Output Open
Input Leakage Current	I_{LIH}			10	μA	$V_{IN} = V_{CC}$
Input Leakage Current	I_{LIL}			-10	μA	$V_{IN} = 0.4V$
Output Leakage Current	I_{LOH}			±10	μA	$V_{OUT} = V_{CC}$; $\overline{CS} = 2.0V$
Output Leakage Current	I_{LOL}			-10	μA	$V_{OUT} = 0.4V$, $\overline{CS} = 2.0V$

Notes: ① Any set of eight (8) outputs from either Port A, B, or C can source 4 mA into 1.5V.

② I_{OL} = 2.5 mA for DB Port; 1.7 mA for Peripheral Ports.

③ I_{OH} = −400 μA for dB Port; −200 μs for Peripheral Ports.

CAPACITANCE

$T_a = 25°C$; $V_{CC} = V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	$f_c = 1$ MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

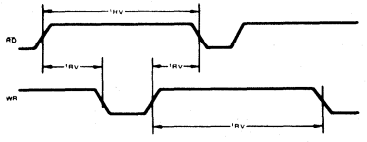
T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{SS} = 0V

AC CHARACTERISTICS

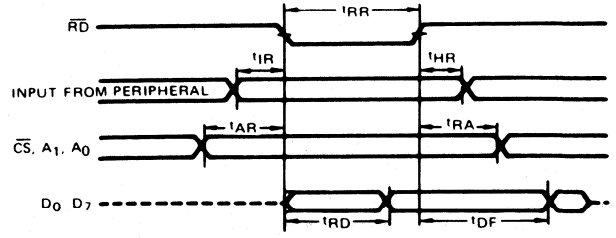
PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Address Stable Before $\overline{READ}$	t_{AR}	0		ns	
Address Stable After $\overline{READ}$	t_{RA}	0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	250		ns	
Data Valid From $\overline{READ}$	t_{RD}		170	ns	8255: C_L = 100 pF 8255A-5: C_L = 150 pF
Data Float After $\overline{READ}$	t_{DF}		100	ns	C_L = 100 pF
		10		ns	C_L = 15 pF
Time Between $\overline{READS}$ and/ $\overline{WRITES}$	t_{RV}	850		ns	②
WRITE					
Address Stable Before $\overline{WRITE}$	t_{AW}	0		ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	250		ns	
Data Valid to $\overline{WRITE}$ (T.E.)	t_{DW}	100		ns	
Data Valid After $\overline{WRITE}$	t_{WD}	0		ns	
OTHER TIMING					
$\overline{WR}$ = 0 To Output	t_{WB}		350	ns	8255: C_L = 50 pF 8255A-5: C_L =150 pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0		ns	
Peripheral Data After $\overline{RD}$	t_{HR}	0		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	300		ns	
$\overline{STB}$ Pulse Width	t_{ST}	350		ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	0		ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150		ns	
$\overline{ACK}$ = 0 To Output	t_{AD}		300	ns	8255: C_L = 50 pF 8255A-5: C_L = 150 pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}		250	ns	8255 { C_L = 50 pF
		20			C_L = 15 pF
$\overline{WR}$ = 1 To OBF = 0	t_{WOB}		650	ns	
$\overline{ACK}$ = 0 To OBF = 1	t_{AOB}		350	ns	
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}		300	ns	8255: C_L = 50 pF
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}		300	ns	
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}		400	ns	
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}		300	ns	8255A-5: C_L = 150 pF
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}		350	ns	
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}		850	ns	

Note: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

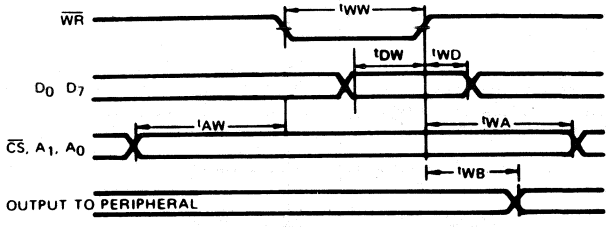
②



TIMING WAVEFORMS
MODE 0

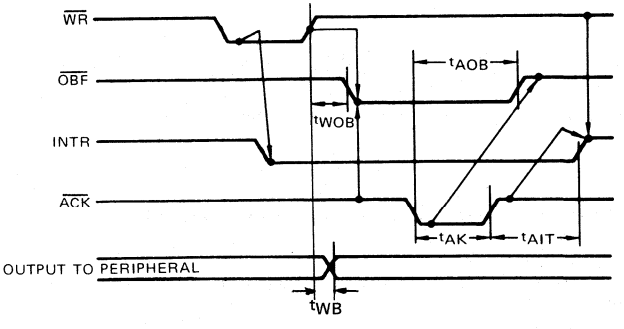


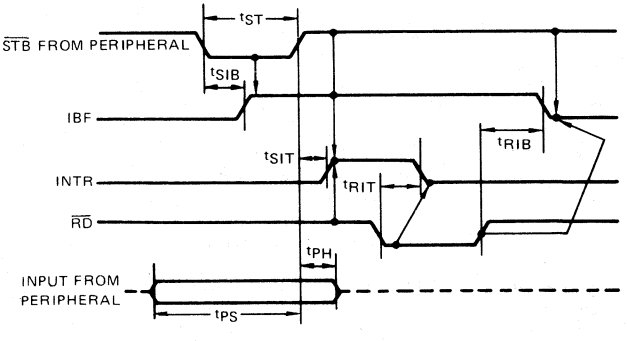
BASIC INPUT (READ)



BASIC OUTPUT (WRITE)

MODE 1





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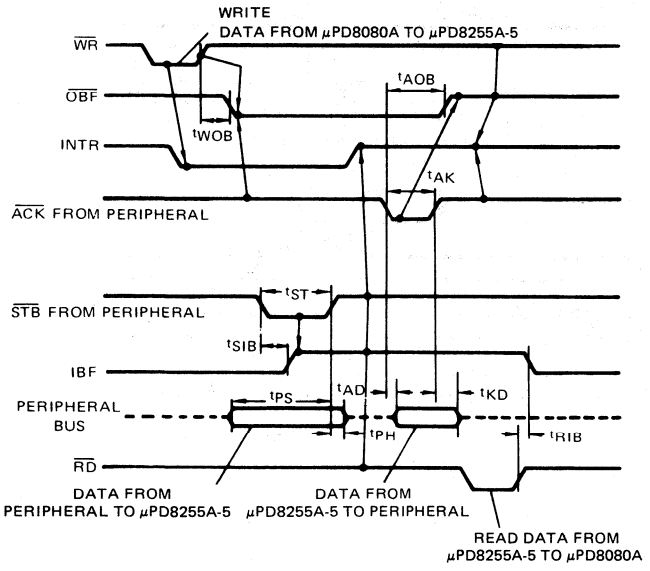
TIMING WAVEFORMS (CONT.)

MODE 2



Note: ① Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

② When the μPD8255A-5 is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

MODES

The μPD8255A-5 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

16 different configurations in MODE 0

Two 8-bit ports and two 4-bit ports

Inputs are not latched

Outputs are latched

MODE 1

MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C.

Two I/O Groups (I and II)

Both groups contain an 8-bit data port and a 4-bit control/data port

Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.

An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})

Both inputs and outputs are latched

An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

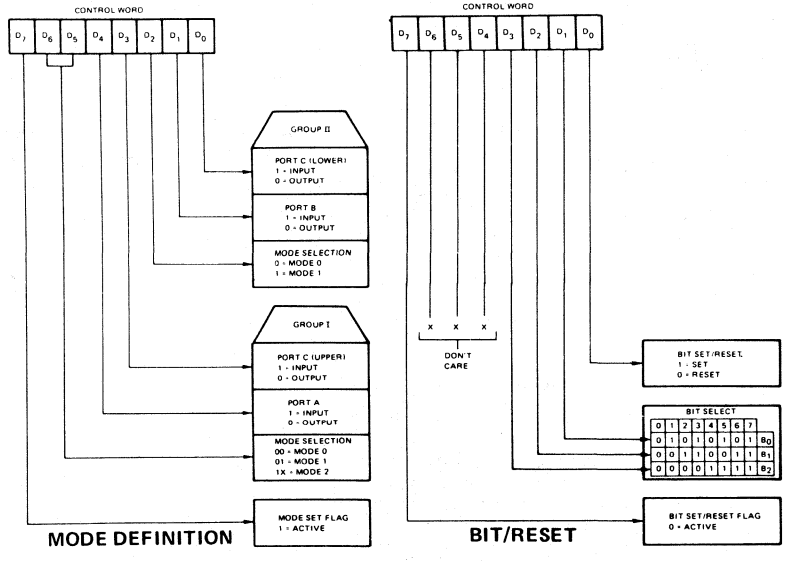
INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

NOTES: ① X means "DO NOT CARE."
② All conditions not listed are illegal and should be avoided.

FORMATS



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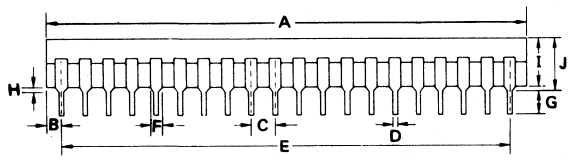
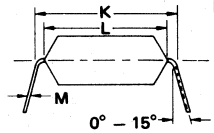
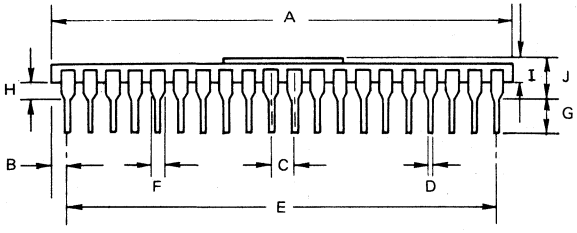
PACKAGE OUTLINE
μPD8255AC/D-5

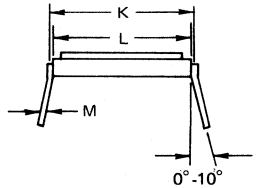




Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$





Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

PROGRAMMABLE DMA CONTROLLER

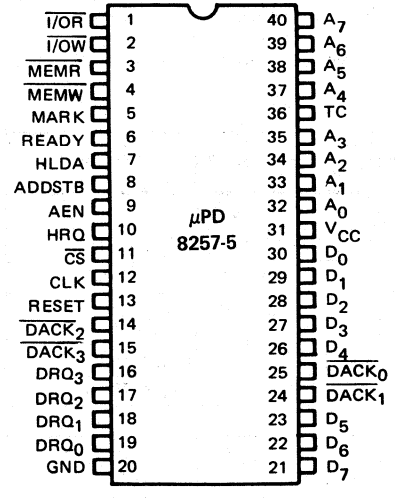
DESCRIPTION

The μPD8257-5 is a programmable four-channel Direct Memory Access (DMA) controller. It is designed to simplify high speed transfers between peripheral devices and memories. Upon a peripheral request, the μPD8257-5 generates a sequential memory address, thus allowing the peripheral to read or write data directly to or from memory. Peripheral requests are prioritized within the μPD8257-5 so that the system bus may be acquired by the generation of a single HOLD command to the 8080A. DMA cycle counts are maintained for each of the four channels, and a control signal notifies the peripheral when the preprogrammed member of DMA cycles has occurred. Output control signals are also provided which allow simplified sectored data transfers and expansion to other μPD8257-5 devices for systems requiring more than four DMA channels.

FEATURES

- NEC Now Supplies μPD8257-5 to μPD8257 Requirements
- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Automatic Load Mode
- Single TTL Clock
- Single +5V Supply ±10%
- Expandable
- 40 Pin Plastic Dual-In-Line Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus
A_7-A_0	Address Bus
$\overline{I/OR}$	I/O $\overline{Read}$
$\overline{I/OW}$	I/O $\overline{Write}$
$\overline{MEMR}$	Memory $\overline{Read}$
$\overline{MEMW}$	Memory $\overline{Write}$
CLK	Clock Input
RESET	Reset Input
READY	Ready
HRQ	Hold Request (to 8080A)
HLDA	Hold Acknowledge (from 8080A)
AEN	Address Enable
ADSTB	Address Strobe
TC	Terminal Count
MARK	Modulo 128 Mark
DRQ_3-DRQ_0	DMA Request Input
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA Acknowledge Out
$\overline{CS}$	Chip Select
V_{CC}	+5 Volts
GND	Ground

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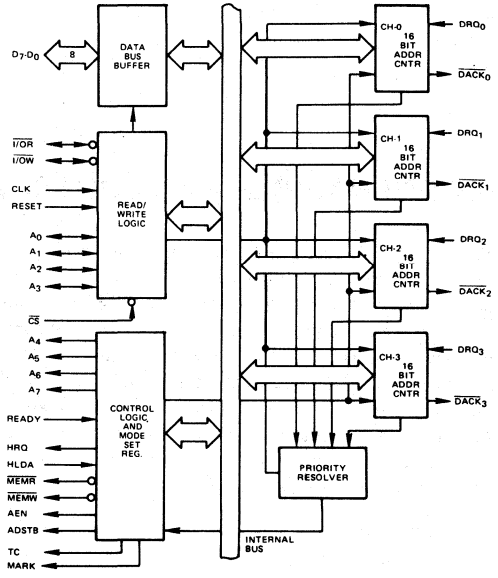
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin ..... -0.5 to +7 Volts ①
Power Dissipation ..... 1 Watt

Note: ① With Respect to Ground

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$ GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Low Voltage	V_{IL}	-0.5		0.8	Volts	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	Volts	
Output Low Voltage	V_{OL}			0.45	Volts	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	Volts	I_{OH} = -150 μA for AB, DB and AEN I_{OH} = -80 μA for others
HRQ Output High Voltage	V_{HH}	3.3		V_{CC}	Volts	I_{OH} = -80 μA
V_{CC} Current Drain	I_{CC}			120	mA	
Input Leakage	I_{IL}			10	μA	$V_{IN} = V_{CC}$
Output Leakage During Float	I_{OFL}			10	μA	V_{OUT} ①

Note: ① $V_{CC} > V_{OUT} >$ GND + 0.45V

CAPACITANCE

$T_a = 25°C$; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

AC CHARACTERISTICS PERIPHERAL (SLAVE) MODE

BUS PARAMETERS

$T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$; GND = 0V ①

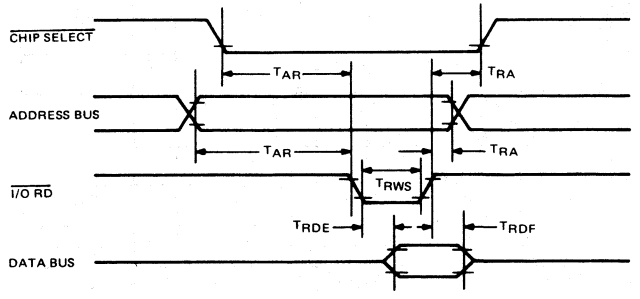
PARAMETER	SYMBOL	LIMITS μPD8257-5 MIN	LIMITS μPD8257-5 TYP	LIMITS μPD8257-5 MAX	UNIT	TEST CONDITIONS
READ						
Adr or $\overline{CS}\downarrow$ Setup to $\overline{Rd}\downarrow$	T_{AR}	0			ns	
Adr or $\overline{CS}\uparrow$ Hold from $\overline{Rd}\uparrow$	T_{RA}	0			ns	
Data Access from $\overline{Rd}\downarrow$	T_{RDE}	0		170	ns	C_L = 100 pF
DB→Float Delay from $\overline{Rd}\uparrow$	T_{RDF}			100	ns	C_L = 100 pF
		20			ns	C_L = 15 pF
$\overline{Rd}$ Width	T_{RW}	250			ns	
WRITE						
Adr Setup to $\overline{Wr}\downarrow$	T_{AW}	20			ns	
Adr Hold from $\overline{Wr}\uparrow$	T_{WA}	0			ns	
Data Setup to $\overline{Wr}\downarrow$	T_{DW}	200			ns	
Data Hold from $\overline{Wr}\uparrow$	T_{WD}	0			ns	
Wr Width	T_{WWS}	200			ns	
OTHER TIMING						
Reset Pulse Width	T_{RSTW}	300			ns	
Power Supply ↑(V_{CC}) Setup to Reset↓	T_{RSTD}	500			μs	
Signal Rise Time	T_r			20	ns	
Signal Fall Time	T_f			20	ns	
Reset to First $\overline{IOWR}$	T_{RSTS}	2			t_{CY}	

Note: ① All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V.

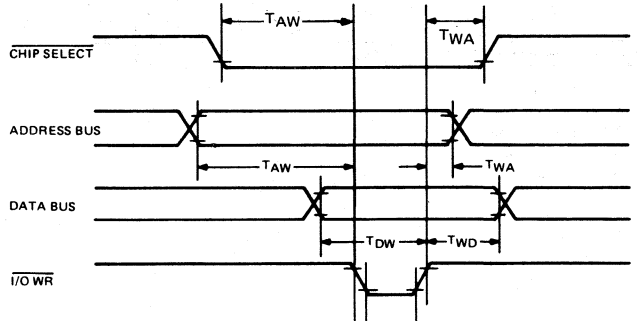
②, Data for comparison only.

TIMING WAVEFORMS PERIPHERAL (SLAVE) MODE

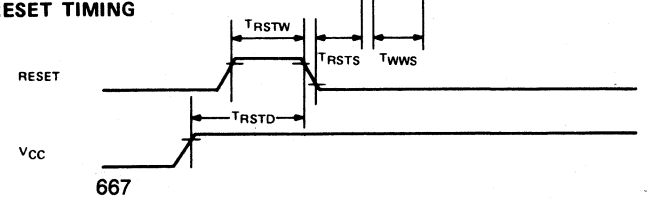
READ TIMING



WRITE TIMING



RESET TIMING



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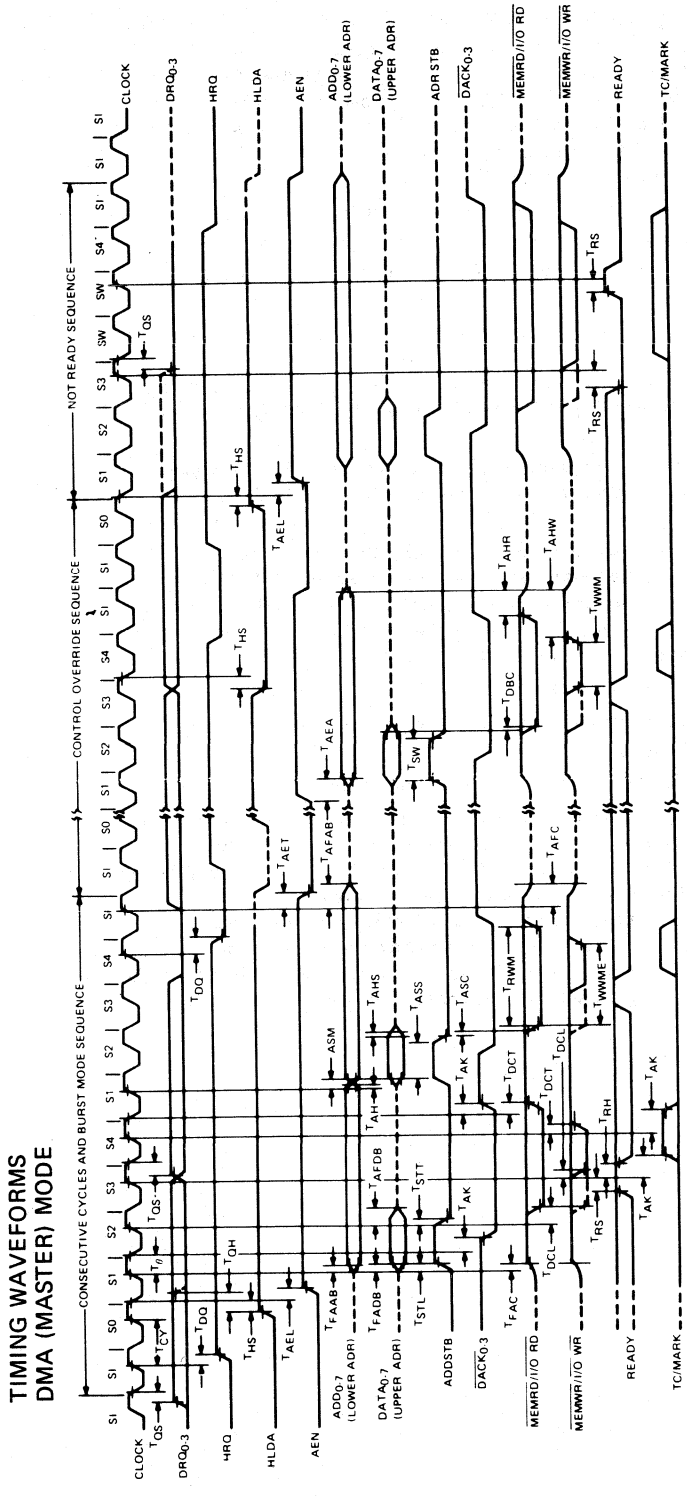
AC CHARACTERISTICS
DMA (MASTER) MODE

T_a = 0°C to 70°C; V_{CC} = +5V ± 10%; GND = 0V

PARAMETER	SYMBOL	LIMITS μPD8257-5 MIN	LIMITS μPD8257-5 MAX	UNIT	TEST CONDITIONS
Cycle Time (Period)	T_{CY}	0.250	4	μs	
Clock Active (High)	T_θ	80	.8T_{CY}	ns	
DRQ↑ Setup to θ↓ (SI, S4)	T_{QS}	30			
DRQ↓ Hold from HLDA↑	T_{QH}	0			④
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 2.0V)	T_{DQ}		160	ns	①
HRQ↑ or ↓ Delay from θ↑ (SI, S4) (measured at 3.3V)	T_{DQ1}		250	ns	③
HLDA↑ or ↓Setup to θ↓ (SI, S4)	T_{HS}	100		ns	
AEN↑ Delay from θ↓ (S1)	T_{AEL}		250	ns	①
AEN↓ Delay from θ↑ (SI)	T_{AET}		200	ns	①
Adr (AB) (Active) Delay from AEN↑ (S1)	T_{AEA}	20		ns	④
Adr (AB) (Active) Delay from θ↑ (S1)	T_{FAAB}		250	ns	②
Adr (AB) (Float) Delay from θ↑ (SI)	T_{AFAB}		150	ns	②
Adr (AB) (Stable) Delay from θ↑ (S1)	T_{ASM}		250	ns	②
Adr (AB) (Stable) Hold from θ↑ (S1)	T_{AH}	T_{ASM}-50			②
Adr (AB) (Valid) Hold from $\overline{Rd}$↑ (S1, SI)	T_{AHR}	60		ns	④
Adr (AB) (Valid) Hold from $\overline{Wr}$↑ (S1, SI)	T_{AHW}	300		ns	④
Adr (DB) (Active) Delay from θ↑ (S1)	T_{FADB}		250	ns	②
Adr (DB) (Float) Delay from θ↑ (S2)	T_{AFDB}	T_{STT}+20	170	ns	②
Adr (DB) Setup to Adr Stb↓ (S1-S2)	T_{ASS}	100		ns	④
Adr (DB) (Valid) Hold from Adr Stb↓ (S2)	T_{AHS}	50		ns	④
Adr Stb↑ Delay from θ↑ (S1)	T_{STL}		200	ns	①
Adr Stb↓ Delay from θ↑ (S2)	T_{STT}		140	ns	①
Adr Stb Width (S1-S2)	T_{SW}	T_{CY}-100		ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr Stb↓ (S2)	T_{ASC}	70		ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr (DB) (Float) (S2)	T_{DBC}	20		ns	④
DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark ↑ Delay from θ↑ (S3) and TC/Mark ↓ Delay from θ↑ (S4)	T_{AK}		250	ns	① ⑤
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from θ↑ (S2) and $\overline{Wr}$↓ Delay from θ↑ (S3)	T_{DCL}		200	ns	② ⑥
$\overline{Rd}$↑ Delay from θ↓ (S1, SI) and $\overline{Wr}$↑ Delay from θ↑ (S4)	T_{DCT}		200	ns	② ⑦
$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑ (S1)	T_{FAC}		250	ns	②
$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑ (SI)	T_{AFC}		150	ns	②
$\overline{Rd}$ Width (S2-S1 or SI)	T_{RWM}	$2T_{CY}$+ T_θ-50		ns	④
$\overline{Wr}$ Width (S3-S4)	T_{WWM}	T_{CY}-50		ns	④
$\overline{Wr}$ (Ext) Width (S2-S4)	T_{WWME}	$2T_{CY}$-50		ns	④
READY Set Up Time to θ↑ (S3, Sw)	T_{RS}	30		ns	
READY Hold Time from θ↑ (S3, Sw)	T_{RH}	20		ns	

Notes: ① Load = 1 TTL
② Load = 1 TTL + 50 pF
③ Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V
④ Tracking Specification
⑤ ΔT_{AK} <50 ns
⑥ ΔT_{DGL} <50 ns
⑦ ΔT_{DCT} <50 ns
⑧ Data for comparison only

TIMING WAVEFORMS
DMA (MASTER) MODE



FUNCTIONAL DESCRIPTION

The μPD8257-5 is a programmable, Direct Memory Address (DMA) device. When used with an 8212 I/O port device, it provides a complete four-channel DMA controller for use in 8080A/8085A based systems. Once initialized by an 8080A/8085A CPU, the μPD8257-5 will block transfer up to 16,364 bytes of data between memory and a peripheral device without any attention from the CPU, and it will do this on all 4-DMA channels. After receiving a DMA transfer request from a peripheral, the following sequence of events occurs within the μPD8257-5.

- It acquires control of the system bus (placing 8080A/8085A in hold mode).
- Resolves priority conflicts if multiple DMA requests are made.
- A 16-bit memory address word is generated with the aid of an 8212 in the following manner:

  The μPD8257-5 outputs the least significant eight bits (A_0-A_7) which go directly onto the address bus.

  The μPD8257-5 outputs the most significant eight bits (A_8-A_{15}) onto the data bus where they are latched into an 8212 and then sent to the high order bits on the address bus.
- The appropriate memory and I/O read/write control signals are generated allowing the peripheral to receive or deposit a data byte directly from or to the appropriate memory location.

Block transfer of data (e.g., a sector of data on a floppy disk) either to or from a peripheral may be accomplished as long as the peripheral maintains its DMA Request (DRQ_n). The μPD8257-5 retains control of the system bus as long as DRQ_n remains high or until the Terminal Count (TC) is reached. When the Terminal Count occurs, TC goes high, informing the CPU that the operation is complete.

There are three different modes of operation:

- DMA read, which causes data to be transferred from memory to a peripheral;
- DMA write, which causes data to be transferred from a peripheral to memory; and
- DMA verify, which does not actually involve the transfer of data.

The DMA read and write modes are the normal operating conditions for the μPD8257-5. The DMA verify mode responds in the same manner as read/write except no memory or I/O read/write control signals are generated, thus preventing the transfer of data. The peripheral gains control of the system bus and obtains DMA Acknowledgements for its requests, thus allowing it to access each byte of a data block for check purposes or accumulation of a CRC (Cylic Redundancy Code) checkword. In some applications it is necessary for a block of DMA read or write cycles to be followed by a block of DMA verify cycles to allow the peripheral to verify its newly acquired data.

DMA OPERATION

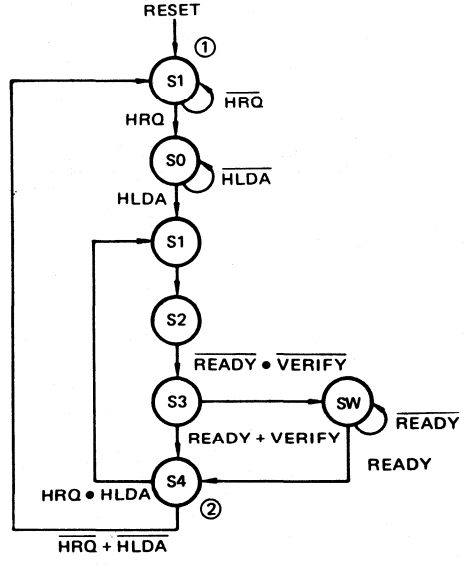
Internally the μPD8257-5 contains six different states (S0, S1, S2, S3, S4 and SW). The duration of each state is determined by the input clock. In the idle state, (S1), no DMA operation is being executed. A DMA cycle is started upon receipt of one or more DMA Requests (DRQ_n), then the μPD8257-5 enters the S0 state. During state S0 a Hold Request (HRQ) is sent to the 8080A/8085A and the μPD8257-5 waits in S0 until the 8080A/8085A issues a Hold Acknowledge (HLDA) back. During S0, DMA Requests are sampled and DMA priority is resolved (based upon either the fixed or priority scheme). After receipt of HLDA, the DMA Acknowledge line ($\overline{DACK}_n$) with the highest priority is driven low, selecting that particular peripheral for the DMA cycle. The DMA Request line (DRQ_n) must remain high until either a DMA Acknowledge ($\overline{DACK}_n$) or both $\overline{DACK}_n$ and TC (Terminal Count) occur, indicating the end of a block or sector transfer (burst model).

The DMA cycle consists of four internal states; S1, S2, S3 and S4. If the access time of the memory or I/O device is not fast enough to return a Ready command to the μPD8257-5 after it reaches state S3, then a Wait state is initiated (SW). One or more than one Wait state occurs until a Ready signal is received, and the μPD8257-5 is allowed to go into state S4. Either the extended write option or the DMA Verify mode may eliminate any Wait state.

If the μPD8257-5 should lose control of the system bus (i.e., HLDA goes low) then the current DMA cycle is completed, the device goes into the S1 state, and no more DMA cycles occur until the bus is reacquired. Ready setup time (t_{RS}), write setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) should all be carefully observed during the handshaking mode between the μPD8257-5 and the 8080A/8085A.

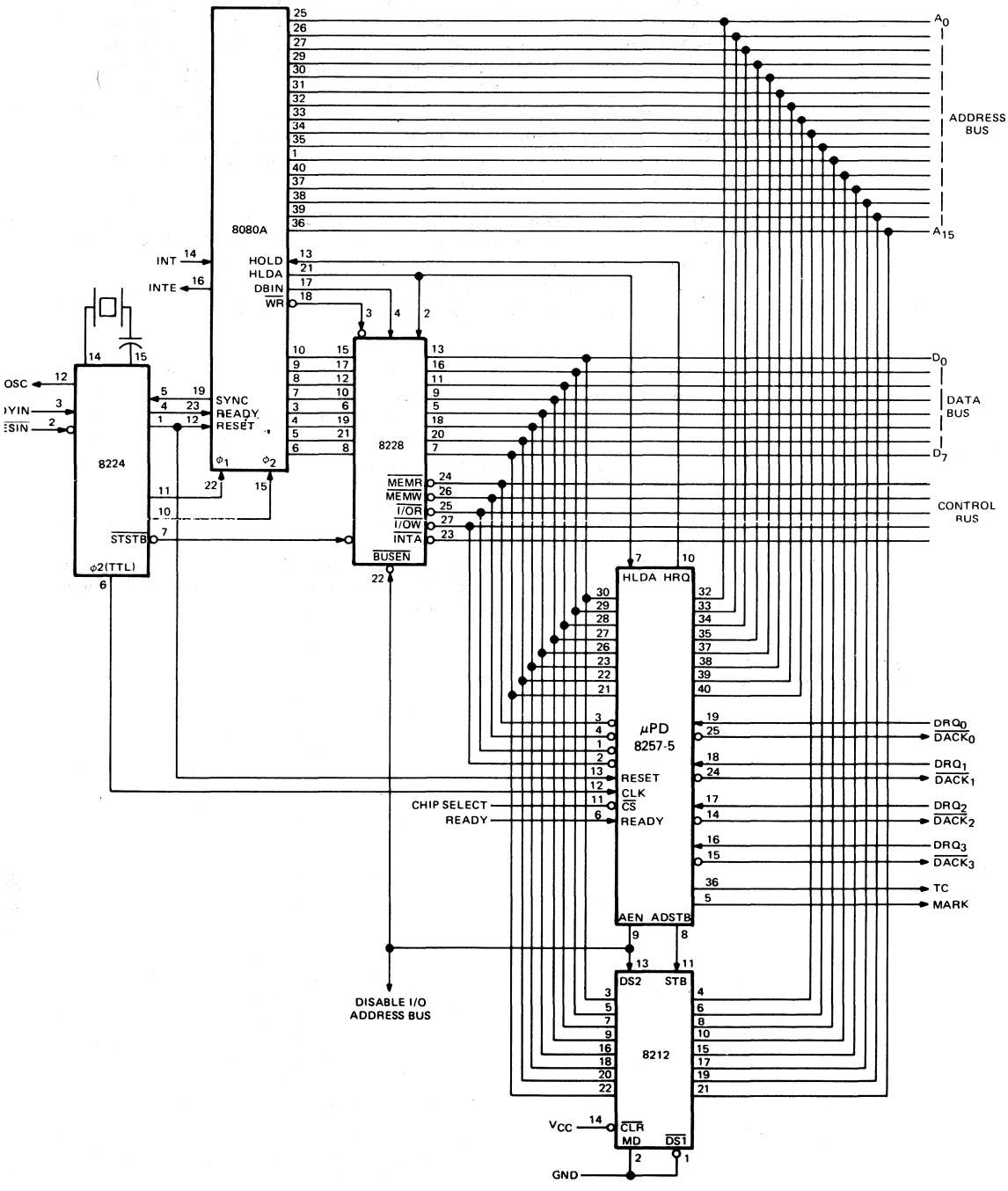
During DMA write cycles, the I/O Read ($\overline{I/O\ R}$) output is generated at the beginning of state S2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S2 and the I/O Write ($\overline{I/O\ W}$) goes low at the beginning of state S3. No Read or Write control signals are generated during DMA verify cycles.

DMA OPERATION STATE DIAGRAM

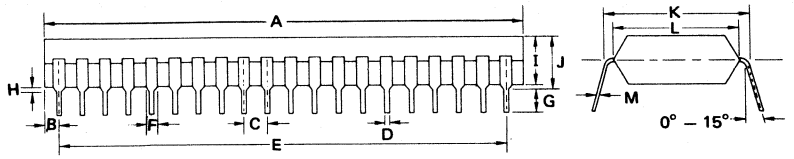


Notes: ① HRQ is set if DRQ_n is active.
② HRQ is reset if DRQ_n is not active.

TYPICAL μPD8257-5
SYSTEM INTERFACE SCHEMATIC



PACKAGE OUTLINE
μPD8257C-5



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

9

PROGRAMMABLE INTERRUPT CONTROLLER

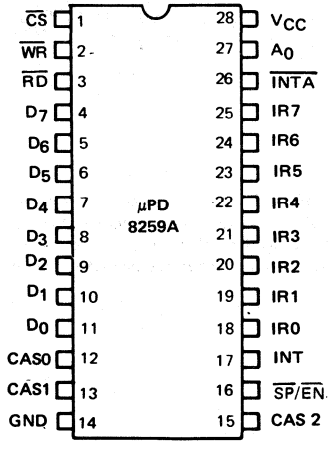
DESCRIPTION

The NEC μPD8259A is a programmable interrupt controller directly compatible with the 8080A/8085A/8086/8088 microprocessors. It can service eight levels of interrupts and contains on-chip logic to expand interrupt capabilities up to 64 levels with the addition of other μPD8259As. The user is offered a selection of priority algorithms to tailor the priority processing to meet his system requirements. These can be dynamically modified during operation, expanding the versatility of the system.
The μPD8259A is completely upward compatible with the μPD8259-5, so software written for the μPD8259-5 will run on the μPD8259A.

FEATURES

- Eight Level Priority Controller
- Programmable Base Vector Address
- Expandable to 64 Levels
- Programmable Interrupt Modes (Algorithms)
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- Full Compatibility with 8080A/8085A/8086/8088
- Available in 28-Pin Plastic and Ceramic Packages

PIN CONFIGURATION

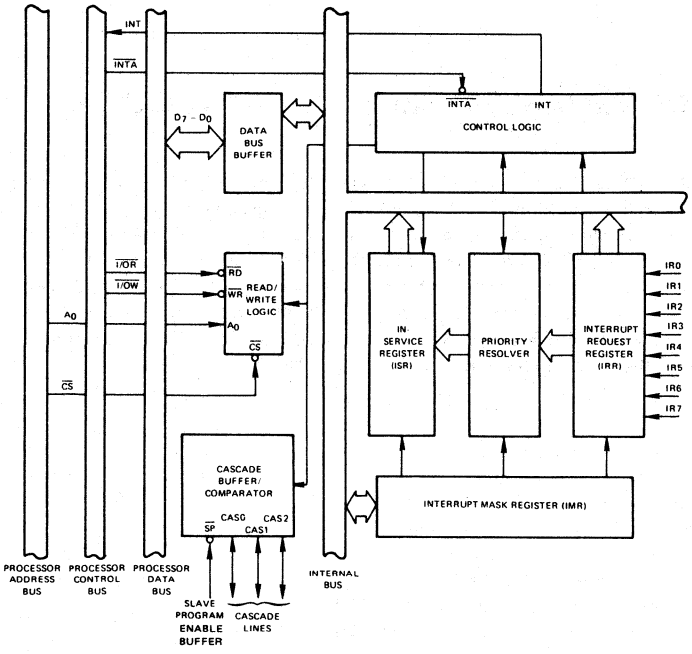


PIN NAMES

$D_7 - D_0$	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
CAS2 – CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Program Input/ Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 – IR7	Interrupt Request Inputs
$\overline{CS}$	Chip Select

9

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1W

Note: ① With respect to ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupt request register and in-service register store the in-coming interrupt request signals appearing on the IR0-7 lines (refer to functional block diagram). The inputs requesting service are stored in the IRR while the interrupts actually being serviced are stored in the ISR.

A positive transition on an IR input sets the corresponding bit in the Interrupt Request Register, and at the same time the INT output of the μPD8259 is set high. The IR input line must remain high until the first $\overline{\text{INTA}}$ input has been received. Multiple, non-masked interrupts occurring simultaneously can be stored in the IRR. The incoming $\overline{\text{INTA}}$ sets the appropriate ISR bit (determined by the programmed interrupt algorithm) and resets the corresponding IRR bit. The ISR bit stays high-active during the interrupt service subroutine until it is reset by the programmed End-of-Interrupt (EOI) command.

PRIORITY RESOLVER

The priority resolver decides the priority of the interrupt levels in the IRR. When the highest priority interrupt is determined it is loaded into the appropriate bit of the In-Service register by the first $\overline{\text{INTA}}$ pulse.

DATA BUS BUFFER

The 3-state, 8-bit, bi-directional data bus buffer interfaces the μPD8259 to the processor's system bus. It buffers the Control Word and Status Data transfers between the μPD8259 and the processor bus.

READ/WRITE LOGIC

The read/write logic accepts processor data and stores it in its Initialization Command Word (ICW) and Operation Command Word (OCW) registers. It also controls the transfer of the Status Data to the processor's data bus.

CHIP SELECT ($\overline{\text{CS}}$)

The μPD8259 is enabled when an active-low signal is received at this input. Reading or writing of the μPD8259 is inhibited when it is not selected.

WRITE ($\overline{\text{WR}}$)

This active-low signal instructs the μPD8259 to receive Command Data from the processor.

READ ($\overline{\text{RD}}$)

When an active-low signal is received on the $\overline{\text{RD}}$ input, the status of the Interrupt Request Register, In-Service Register, Interrupt Mask Register or binary code of the Interrupt Level is placed on the data bus.

INTERRUPT (INT)

The interrupt output from the μPD8259 is directly connected to the processor's INT input. The voltage levels of this output are compatible with the 8080A/8085A/8086/8088.

INTERRUPT MASK REGISTER (IMR)

The interrupt mask register stores the bits for the individual interrupt bits to be masked. The IMR masks the data in the ISR. Lower priority lines are not affected by masking a higher priority line.

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

$\overline{INTA}$ pulses cause the μPD8259A to put vectoring information on the bus. The number of pulses depends upon whether the μPD8259A is in μPD8085A mode or 8086/8088 mode.

A_0

A_0 is usually connected to the processor's address bus. Together with $\overline{WR}$ and $\overline{RD}$ signals it directs the loading of data into the command register or the reading of status data. The following table illustrates the basic operations performed. Note that it is divided into three functions: Input, Output and Bus Disable distinguished by the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs.

μPD8259A BASIC OPERATION						
A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	PROCESSOR INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or IR → Data Bus ①
1			0	1	0	IMR → Data Bus
						PROCESSOR OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	Data Bus → OCW2
0	0	1	1	0	0	Data Bus → OCW3
0	1	X	1	0	0	Data Bus → ICW1
1	X	X	1	0	0	Data Bus → OCW1, ICW2, ICW3 ②
						DISABLE FUNCTION
X	X	X	1	1	0	Data Bus → 3-State
X	X	X	X	X	1	Data Bus → 3-State

Notes: ① The contents of OCW2 written prior to the READ operation governs the selection of the IRR, ISR or Interrupt Level.

② The sequencer logic on the μPD8259A aligns these commands in the proper order.

CASCADE BUFFER/COMPARATOR. (For Use in Multiple μPD8259 Array.)

The IDs of all μPD8259As are buffered and compared in the cascade buffer/comparator. The master μPD8259A sends the ID of the interrupting slave device along the CAS0, 1, 2 lines to all slave devices. The cascade buffer/comparator compares its preprogrammed ID to the CAS0, 1, 2 lines. The next two $\overline{INTA}$ pulses strobe the preprogrammed, 2 byte CALL routine address onto the data bus from the slave whose ID matches the code on the CAS0, 1, 2 lines.

SLAVE PROGRAM ($\overline{SP}$). (For Use in Multiple μPD8259A Array.)

The interrupt capability can be expanded to 64 levels by cascading multiple μPD8259As in a master-plus-slaves array. The master controls the slaves through the CAS0, 1, 2 lines. The $\overline{SP}$ input to the device selects the CAS0-2 lines as either outputs ($\overline{SP}$=1) for the master or as inputs ($\overline{SP}$=0) for the slaves. For one device only the $\overline{SP}$ must be set to a logic "1" since it is functioning as a master.

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5V	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Interrupt Output-High Voltage	V_{OH-INT}	2.4			V	I_{OH} = -400 μA
		3.5			V	I_{OH} = -100 μA
Input Leakage Current for IR_{0-7}	I_{IL} (IR_{0-7})			-300	μA	V_{IN} = 0V
				10	μA	V_{IN} = V_{CC}
Input Leakage Current for other Inputs	I_{IL}			10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LOL}			- 10	μA	V_{OUT} = 0.45 V
Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Supply Current	I_{CC}			85	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured Pins Returned to V_{SS}

AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5V ± 10% (μPD8259A)

PARAMETER	SYMBOL	μPD8259A MIN	μPD8259A MAX	UNIT	TEST CONDITIONS
AO/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	t_{AHRL}	0		ns	
AO/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	t_{RHAX}	0		ns	
$\overline{RD}$ Pulse Width	t_{RLRH}	235		ns	
AO/$\overline{CS}$ Setup to $\overline{WR}$↓	t_{AHWL}	0		ns	
AO/$\overline{CS}$ Hold after $\overline{WR}$↑	t_{WHAX}	0		ns	
$\overline{WR}$ Pulse Width	t_{WLWH}	290		ns	
Data Setup to $\overline{WR}$↑	t_{DVWH}	240		ns	
Data Hold after $\overline{WR}$↑	t_{WHDX}	0		ns	
Interrupt Request Width (Low)	t_{JLJH}	100		ns	①
Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave Only)	t_{CVIAL}	55		ns	
End of $\overline{RD}$ to Next Command	t_{RHRL}	160		ns	
End of $\overline{WR}$ to Next Command	t_{WHRL}	190		ns	

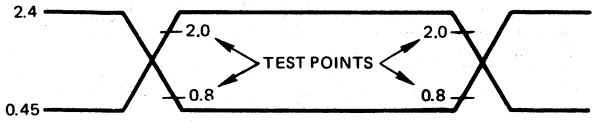
Note: ① This is the low time required to clear the input latch in the edge triggered mode.

PARAMETER	SYMBOL	μPD8259A MIN	μPD8259A MAX	UNIT	TEST CONDITIONS
Data Valid from $\overline{RD}$/$\overline{INTA}$↓	t_{RLDV}		200	ns	C of Data Bus = 100 pF
Data Float after $\overline{RD}$/$\overline{INTA}$↑	t_{RHDZ}		100	ns	C of Data Bus Max Test C = 100 pF Min Test C = 15 pF
Interrupt Output Delay	t_{JHIH}		350	ns	
Cascade Valid from First $\overline{INTA}$↓ (Master Only)	t_{IALCV}		565	ns	C_{INT} = 100 pF
Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓	t_{RLEL}		125	ns	$C_{CASCADE}$ = 100 pF
Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑	t_{RHEH}		150	ns	
Data Valid from Stable Address	t_{AHDV}		200	ns	
Cascade Valid to Valid Data	t_{CVDV}		300	ns	

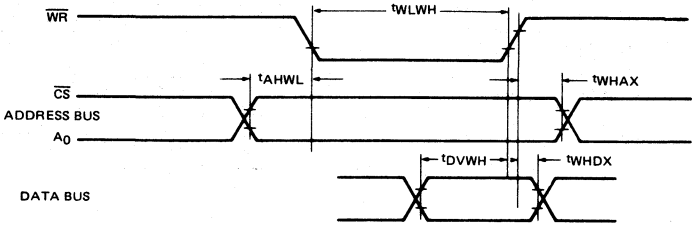
AC CHARACTERISTICS (CONT.)

TIMING WAVEFORMS

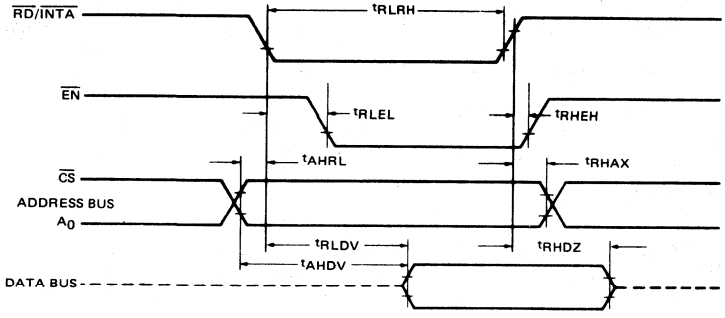
INPUT WAVEFORMS FOR AC TESTS



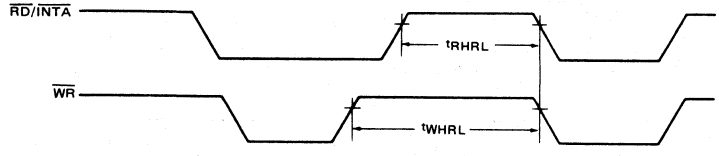
WRITE MODE



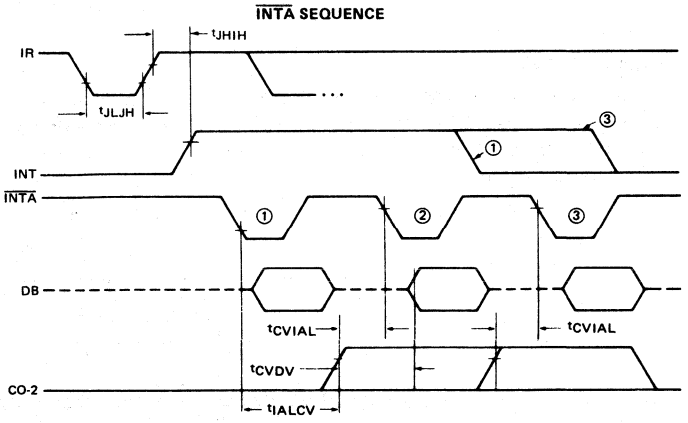
READ/INTA MODE



OTHER TIMING



TIMING WAVEFORMS (CONT.)



DETAILED OPERATIONAL DESCRIPTION

The sequence used by the μPD8259A to handle an interrupt depends upon whether an 8080A/8085A or 8086/8088 CPU is being used.

The following sequence applies to 8080A/8085A systems:

The μPD8259A derives its versatility from programmable interrupt modes and the ability to jump to any memory address through programmable CALL instructions. The following sequence demonstrates how the μPD8259A interacts with the processor.

1. An interrupt or interrupts appearing on IR_{0-7} sets the corresponding IR bit(s) high. This in turn sets the corresponding IRR bit(s) high.
2. Once the IRR bit(s) has been set, the μPD8259A will resolve the priorities according to the preprogrammed interrupt algorithm. It then issues an INT signal to the processor.
3. The processor group issues an $\overline{INTA}$ to the μPD8259A when it receives the INT.
4. The $\overline{INTA}$ input to the μPD8259A from the processor group sets the highest priority ISR bit and resets the corresponding IRR bit. The $\overline{INTA}$ also signals the μPD8259A to issue an 8-bit CALL instruction op-code (11001101) onto its Data bus lines.
5. The CALL instruction code instructs the processor group to issue two more $\overline{INTA}$ pulses to the μPD8259A.
6. The two $\overline{INTA}$ pulses signal the μPD8259A to place its preprogrammed interrupt vector address onto the Data bus. The first $\overline{INTA}$ releases the low-order 8-bits of the address and the second $\overline{INTA}$ releases the high-order 8-bits.
7. The μPD8259A's CALL instruction sequence is complete. A preprogrammed EOI (End-of-Interrupt) command is issued to the μPD8259A at the end of an interrupt service routine to reset the ISR bit and allow the μPD8259A to service the next interrupt.

For 8086/8088 systems the first three steps are the same as described above, then the following sequence occurs:

4. During the first $\overline{INTA}$ from the processor, the μPD8259A does not drive the data bus. The highest priority ISR bit is set and the corresponding IRR bit is reset.
5. The μPD8259A puts vector onto the data bus on the second $\overline{INTA}$ pulse from the 8086/8088.
6. There is no third $\overline{INTA}$ pulse in this mode. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse, or it remains set until an EOI command is issued.

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8080A/8085A MODE

INTERRUPT SEQUENCE

For these processors, the μPD8259A is controlled by three $\overline{\text{INTA}}$ pulses. The first $\overline{\text{INTA}}$ pulse will cause the μPD8259A to put the CALL op-code onto the data bus. The second and third $\overline{\text{INTA}}$ pulses will cause the upper and lower address of the interrupt vector to be released on the bus.

FIRST $\overline{\text{INTA}}$

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

SECOND $\overline{\text{INTA}}$

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

THIRD $\overline{\text{INTA}}$

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

In this mode only two $\overline{\text{INTA}}$ pulses are sent to the μPD8259A. After the first $\overline{\text{INTA}}$ pulse, the μPD8259A does not output a CALL but internally sets priority resolution. If it is a master, it sets the cascade lines. The interrupt vector is output to the data bus on the second $\overline{\text{INTA}}$ pulse.

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

INITIALIZATION COMMAND WORDS

ICW1 AND ICW2

A_5-A_{15}. *Page starting address of service routines.* In an 8085A system, the 8 request levels generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the μPD8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the μPD8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval maintains compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an MCS-86 system, T7-T3 are inserted in the five most significant bits of the vectoring byte and the μPD8259A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address Interval) has no effect.

LTIM: If LTIM = 1, then the μPD8259A operates in the level interrupt mode. Edge detect logic on the interrupt inputs is disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only μPD8259A in the system. If SNGL = 1 no ICW3 is issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

ICW3

This word is read only when there is more than one μPD8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then releases byte 1 of the call sequence (for 8085A system) and enables the corresponding slave to release bytes 2 and 3 (for 8086/8088 only byte 2) through the cascade lines.

b. In the slave mode (either when SP = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the CALL sequence (or just byte 2 for 8086/8088) are released by it on the Data Bus.

ICW4

SFNM: If SFNM = 1 the special fully nested mode is programmed.

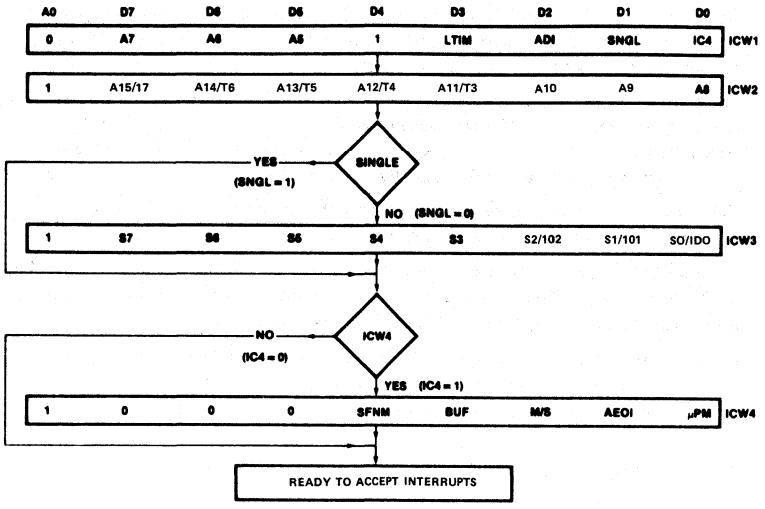
BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the μPD8259A is programmed to be a master, M/S = 0 means the μPD8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the μPD8259A for 8085A system operation, μPM = 1 sets the μPD8259A for 8086 system operation.

INITIALIZATION SEQUENCE



OPPERATIONAL COMMAND WORDS (OCW's) ②

Once the μPD8259A has been programmed with Initialization Command Words, it can be programmed for the appropriate interrupt algorithm by the Operation Command Words. Interrupt algorithms in the μPD8259A can be changed at any time during program operation by issuing another set of Operation Command Words. The following sections describe the various algorithms available and their associated OCW's.

INTERRUPT MASKS

The individual Interrupt Request input lines are maskable by setting the corresponding bits in the Interrupt Mask Register to a logic "1" through OCW1. The actual masking is performed upon the contents of the In-Service Register (e.g., if Interrupt Request line 3 is to be masked, then only bit 3 of the IMR is set to logic "1." The IMR in turn acts upon the contents of the ISR to mask bit 3). Once the μPD8259A has acknowledged an interrupt, i.e., the μPD8259A has sent an INT signal to the processor and the system controller has sent it an $\overline{\text{INTA}}$ signal, the interrupt input, although it is masked, inhibits lower priority requests from being acknowledged. There are two means of enabling these lower priority interrupt lines. The first is by issuing an End-of-Interrupt (EOI) through Operation Command Word 2 (OCW2), thereby resetting the appropriate ISR bit. The second approach is to select the Special Mask Mode through OCW3. The Special Mask Mode (SMM) and End-of-Interrupt (EOI) will be described in more detail further on.

FULLY NESTED MODE

The fully nested mode is the μPD8259A's basic operating mode. It will operate in this mode after the initialization sequence, without requiring Operation Command Words for formatting. Priorities are set IR_0 through IR_7, with IR_0 the highest priority. After the interrupt has been acknowledged by the processor and system controller, only higher priorities will be serviced. Upon receiving an INTA, the priority resolver determines the priority of the interrupt, sets the corresponding IR bit, and outputs the vector address to the Data bus. The EOI command resets the corresponding ISR bits at the end of its service routines.

Notes: ① Reference Figure 2
② Reference Figure 3

9

ROTATING PRIORITY MODE COMMANDS

The two variations of Rotating Priorities are the Auto Rotate and Specific Rotate modes. These two modes are typically used to service interrupting devices of equivalent priorities.

1. Auto Rotate Mode

   Programming the Auto Rotate Mode through OCW2 assigns priorities 0-7 to the interrupt request input lines. Interrupt line IR_0 is set to the highest priority and IR_7 to the lowest. Once an interrupt has been serviced it is automatically assigned the lowest priority. That same input must then wait for the devices ahead of it to be serviced before it can be acknowledged again. The Auto Rotate Mode is selected by programming OCW2 in the following way (refer to Figure 3): set Rotate Priority bit "R" to a logic "1"; program EOI to a logic "1" and SEOI to a logic "0." The EOI and SEOI commands are discussed further on. The following is an example of the Auto Rotate Mode with devices requesting interrupts on lines IR_2 and IR_5.

   Before Interrupts are Serviced:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	1	0	0
							→	Highest Priority
Priority Status Register	IR_7	IR_6	IR_5	IR_4	IR_3	IR_2	IR_1	IR_0

   According to the Priority Status Register, IR_2 has a higher priority than IR_5 and will be serviced first.

   After Servicing:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	0	0	0
							→	Highest Priority
Priority Status Register	IR_2	IR_1	IR_0	IR_7	IR_6	IR_5	IR_4	IR_3

   At the completion of IR_2's service routine the corresponding In-Service Register bit, IS_2 is reset to "0" by the preprogrammed EOI command. IR_2 is then assigned the lowest priority level in the Priority Status Register. The μPD8259A is now ready to service the next highest interrupt, which in this case, is IR_5.

2. Specific Rotate Mode

   The priorities are set by programming the lowest level through OCW2. The μPD8259A then automatically assigns the highest priority. If, for example, IR_3 is set to the lowest priority (bits L_2, L_1, L_0 form the binary code of the bottom priority level), then IR_4 will be set to the highest priority. The Specific Rotate Mode is selected by programming OCW2 in the following manner: set Rotate Priority bit "R" to a logic "1," program EOI to a logic "0," SEOI to a logic "1" and L_2, L_1, L_0 to the lowest priority level. If EOI is set to a logic "1," the ISR bit defined by L_2, L_1, L_0 is reset.

OPERATIONAL COMMAND WORDS (CONT.)

END-OF-INTERRUPT (EOI) AND SPECIFIC END-OF-INTERRUPT (SEOI)

The End-of-Interrupt or Specific End-of-Interrupt command must be issued to reset the appropriate In-Service Register bit before the completion of a service routine. Once the ISR bit has been reset to logic "0," the μPD8259A is ready to service the next interrupt.

Two types of EOIs are available to clear the appropriate ISR bit depending on the μPD8259A's operating mode.

1. Non-Specific End-of-Interrupt (EOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is preserved (e.g., fully nested mode), the particular ISR bit to be reset at the completion of the service routine can be determined. A non-specific EOI command automatically resets the highest priority ISR bit of those set. The highest priority ISR bit must necessarily be the interrupt being serviced and must necessarily be the service subroutine returned from.

2. Specific End-of-Interrupt (SEOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is not preserved (e.g., rotating priority mode) the last serviced interrupt level may not be known. In these modes a Specific End-of-Interrupt must be issued to clear the ISR bit at the completion of the interrupt service routine. The SEOI is programmed by setting the appropriate bits in OCW3 (Figure 2) to logic "1"s. Both the EOI and SEOI bits of OCW3 must be set to a logic "1" with L_2, L_1, L_0 forming the binary code of the ISR bit to be reset.

SPECIAL MASK MODE

Setting up an interrupt mask through the Interrupt Mask Register (refer to Interrupt Mask Register section) by setting the appropriate bits in OCW1 to a logic "1" inhibits lower priority interrupts from being acknowledged. In applications requiring that the lower priorities be enabled while the IMR is set, the Special Mask Mode can be used. The SMM is programmed in OCW3 by setting the appropriate bits to a logic "1." Once the SMM is set, the μPD8259A remains in this mode until it is reset. The Special Mask Mode does not affect the higher priority interrupts.

POLLED MODE

In Poll Mode the processor must be instructed to disable its interrupt input (INT). Interrupt service is initiated through software by a Poll Command. Poll Mode is programmed by setting the Poll Mode bit in OCW3 (P = 1), during a $\overline{WR}$ pulse. The following $\overline{RD}$ pulse is then considered as an interrupt acknowledge. If an interrupt input is present, that $\overline{RD}$ pulse sets the appropriate ISR bit and reads the interrupt priority level. Poll Mode is a one-time operation and must be programmed through OCW3 before every read. The word strobed onto the Data bus during Poll Mode is of the form:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I	X	X	X	X	W_2	W_1	W_0

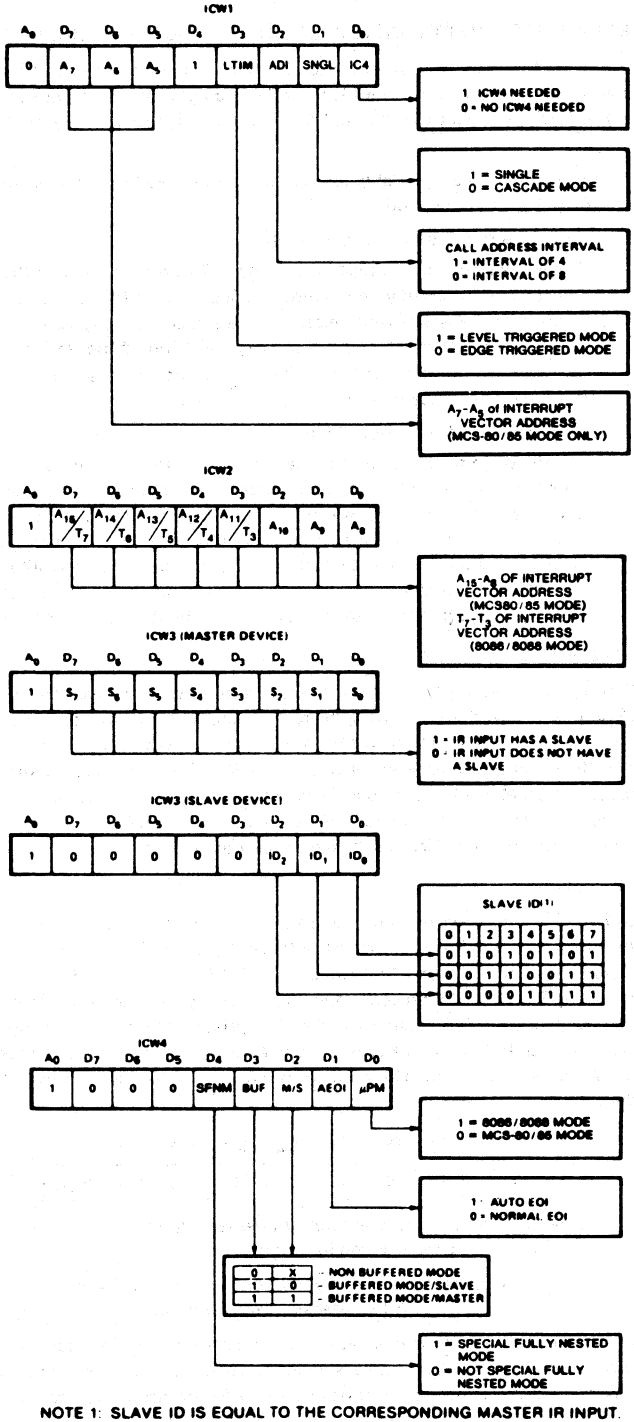
where: I = 1 if there is an interrupt requesting service
= 0 if there are no interrupts

$W_{2\text{-}0}$ forms the binary code of the highest priority level of the interrupts requesting service

Poll Mode can be used when an interrupt service routine is common to several interrupt inputs. The $\overline{INTA}$ sequence is no longer required, thus saving in ROM space. Poll Mode can also be used to expand the number of interrupts beyond 64.

9

INITIALIZATION COMMAND WORD FORMAT



NOTE 1: SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT.

READING μPD8259 STATUS

The following major registers' status is available to the processor by appropriately formatting OCW3 and issuing $\overline{RD}$ command.

INTERRUPT REQUEST REGISTER (8-BITS)

The Interrupt Request Register stores the interrupt levels awaiting acknowledgement. The highest priority in-service bit is reset once it has been acknowledged. (Note that the Interrupt Mask Register has no effect on the IRR.) A WR command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. The bits which determine whether the IRR and ISR are being read from are RIS and ERIS. To read contents of the IRR, ERIS must be logic "1" and RIS a logic "0."

IN-SERVICE REGISTER (8-BITS)

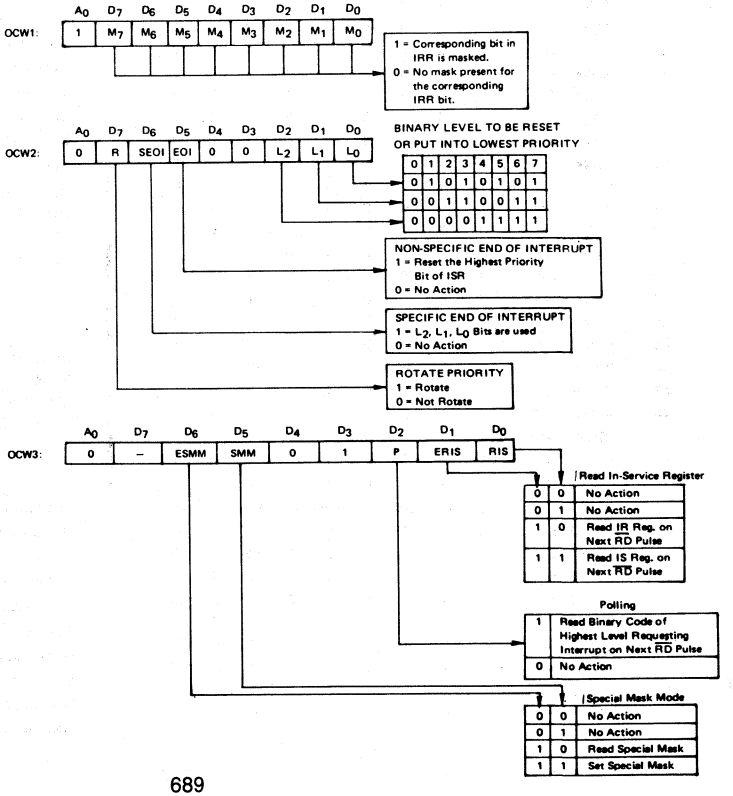
The In-Service Register stores the priorities of the interrupt levels being serviced. Assertion of an End-of-Interrupt (EOI) updates the ISR to the next priority level. A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. Both ERIS and RIS should be set to a logic "1."

INTERRUPT MASK REGISTER (8-BITS)

The Interrupt Mask Register holds mask data modifying interrupt levels. To read the IMR status a $\overline{WR}$ pulse preceding the $\overline{RD}$ is not necessary. The IMR data is available to the data bus when $\overline{RD}$ is asserted with A_0 at a logic "1."

A single OCW3 is sufficient to enable successive status reads providing it is of the same register. A status read is over-ridden by the Poll Mode when bits P and ERIS of OCW3 are set to a logic "1."

OPERATION COMMAND WORD FORMAT



SUMMARY OF 8259A INSTRUCTION SET

Inst. #	Mnemonic		A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description
1	ICW1	A	0	A7	A6	A5	1	0	1	1	0	Format = 4, single, edge triggered
2	ICW1	B	0	A7	A6	A5	1	1	1	1	0	Format = 4, single, level triggered
3	ICW1	C	0	A7	A6	A5	1	0	1	0	0	Format = 4, not single, edge triggered
4	ICW1	D	0	A7	A6	A5	1	1	1	0	0	Format = 4, not single, level triggered
5	ICW1	E	0	A7	A6	0	1	0	0	1	0	Format = 8, single, edge triggered
6	ICW1	F	0	A7	A6	0	1	1	0	1	0	Format = 8, single, level triggered
7	ICW1	G	0	A7	A6	0	1	0	0	0	0	Format = 8, not single, edge triggered
8	ICW1	H	0	A7	A6	0	1	1	0	0	0	Format = 8, not single, level triggered
9	ICW1	I	0	A7	A6	A5	1	0	1	1	1	Format = 4, single, edge triggered
10	ICW1	J	0	A7	A6	A5	1	1	1	1	1	Format = 4, single, level triggered
11	ICW1	K	0	A7	A6	A5	1	0	1	0	1	Format = 4, not single, edge triggered
12	ICW1	L	0	A7	A6	A5	1	1	1	0	1	Format = 4, not single, level triggered
13	ICW1	M	0	A7	A6	0	1	0	0	1	1	Format = 8, single, edge triggered
14	ICW1	N	0	A7	A6	0	1	1	0	1	1	Format = 8, single, level triggered
15	ICW1	O	0	A7	A6	0	1	0	0	0	1	Format = 8, not single, edge triggered
16	ICW1	P	0	A7	A6	0	1	1	0	0	1	Format = 8, not single, level triggered
17	ICW2		1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization
18	ICW3	M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master
19	ICW3	S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave
20	ICW4	A	1	0	0	0	0	0	0	0	0	No action, redundant
21	ICW4	B	1	0	0	0	0	0	0	0	1	Non-buffered mode, no AEOI, 8086/8088
22	ICW4	C	1	0	0	0	0	0	0	1	0	Non-buffered mode, AEOI, 80/85
23	ICW4	D	1	0	0	0	0	0	0	1	1	Non-buffered mode, AEOI, 8086/8088
24	ICW4	E	1	0	0	0	0	0	1	0	0	No action, redundant
25	ICW4	F	1	0	0	0	0	0	1	0	1	Non-buffered mode, no AEOI, 8086/8088
26	ICW4	G	1	0	0	0	0	0	1	1	0	Non-buffered mode, AEOI, 80/85
27	ICW4	H	1	0	0	0	0	0	1	1	1	Non-buffered mode, AEOI, 8086/8088
28	ICW4	I	1	0	0	0	0	1	0	0	0	Buffered mode, slave, no AEOI, 80/85
29	ICW4	J	1	0	0	0	0	1	0	0	1	Buffered mode, slave, no AEOI, 8086/8088
30	ICW4	K	1	0	0	0	0	1	0	1	0	Buffered mode, slave, AEOI, 80/85
31	ICW4	L	1	0	0	0	0	1	0	1	1	Buffered mode, slave, AEOI, 8086/8088
32	ICW4	M	1	0	0	0	0	1	1	0	0	Buffered mode, master, no AEOI, 80/85
33	ICW4	N	1	0	0	0	0	1	1	0	1	Buffered mode, master, no AEOI, 8086/8088
34	ICW4	O	1	0	0	0	0	1	1	1	0	Buffered mode, master, AEOI, 80/85
35	ICW4	P	1	0	0	0	0	1	1	1	1	Buffered mode, master AEOI, 8086, 8088
36	ICW4	NA	1	0	0	0	1	0	0	0	0	Fully nested mode, 8085A, non-buffered, no AEOI
37	ICW4	NB	1	0	0	0	1	0	0	0	1	ICW4 NB through ICW4 ND are identical to ICW4 B through ICW4 D with the addition of Fully Nested Mode
38	ICW4	NC	1	0	0	0	1	0	0	1	0	
39	ICW4	ND	1	0	0	0	1	0	0	1	1	
40	ICW4	NE	1	0	0	0	1	0	1	0	0	Fully Nested Mode, 80/85, non-buffered, no AEOI
41	ICW4	NF	1	0	0	0	1	0	1	0	1	ICW4 NF through ICW4 NP are identical to ICW4 F through ICW4 P with the addition of Fully Nested Mode
42	ICW4	NG	1	0	0	0	1	0	1	1	0	
43	ICW4	NH	1	0	0	0	1	0	1	1	1	
44	ICW4	NI	1	0	0	0	1	1	0	0	0	
45	ICW4	NJ	1	0	0	0	1	1	0	0	1	
46	ICW4	NK	1	0	0	0	1	1	0	1	0	
47	ICW4	NL	1	0	0	0	1	1	0	1	1	
48	ICW4	NM	1	0	0	0	1	1	1	0	0	
49	ICW4	NN	1	0	0	0	1	1	1	0	1	
50	ICW4	NO	1	0	0	0	1	1	1	1	0	
51	ICW4	NP	1	0	0	0	1	1	1	1	1	
52	OCW1		1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask register, read mark register
53	OCW2	E	0	0	0	1	0	0	0	0	0	Non-specific EOI
54	OCW2	SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI, L0-L2 code of IS FF to be reset
55	OCW2	RE	0	1	0	1	0	0	0	0	0	Rotate on Non-Specific EOI
56	OCW2	RSE	0	1	1	1	0	0	L2	L1	L0	Rotate on Specific EOI L0-L2 code of line
57	OCW2	R	0	1	0	0	0	0	0	0	0	Rotate in Auto EOI (set)
58	OCW2	CR	0	0	0	0	0	0	0	0	0	Rotate in Auto EOI (clear)
59	OCW2	RS	0	1	1	0	0	0	L2	L1	L0	Set Priority Command
60	OCW3	P	0	0	0	0	0	1	1	0	0	Poll mode
61	OCW3	RIS	0	0	0	0	0	1	0	1	1	Read IS register

SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

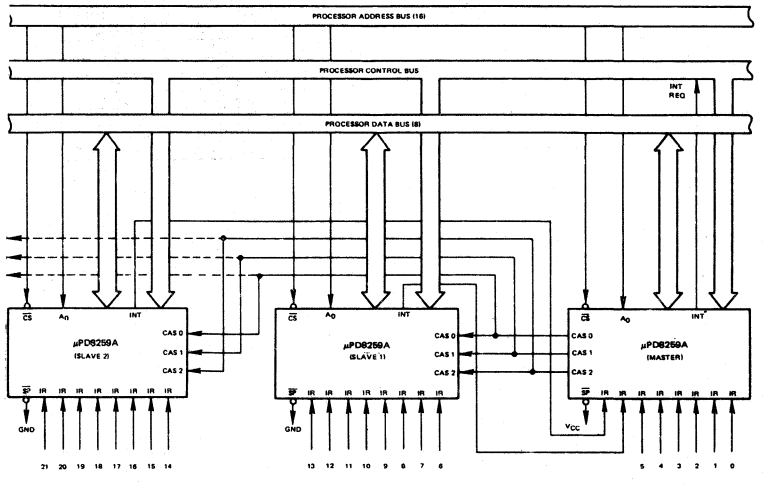
	A_0	D_4	D_3				
OCW1	1	X	X	M_7-M_0			IMR (Interrupt Mask Register) $\overline{WR}$ loads IMR data while $\overline{RD}$ reads status
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action
				0	0	1	Non-Specific End-of-Interrupt
				0	1	0	No Action
				0	1	1	Specific-End-of-Interrupt L_2, L_1, L_0 forms binary representation of level to be reset.
				1	0	0	No Action
				1	0	1	Rotate Priority at End-of-Interrupt (Auto Mode)
				1	1	0	Rotate Priority, L_2, L_1, L_0 specifies bottom priority without End-of-Interrupt
				1	1	1	Rotate Priority at End-of-Interrupt (Specific Mode). L_2, L_1, L_0 specifies bottom priority, and its In-Service Register bit is reset.
OCW3	0	0	1	ESMM	SMM		
				0	0		Special Mask not affected
				0	1		
				1	0		Reset Special Mask
				1	1		Set Special Mask
				ERIS	RIS		
				0	0		No Action
				0	1		
				1	0		Read IR Register Status
				1	1		Read IS Register Status

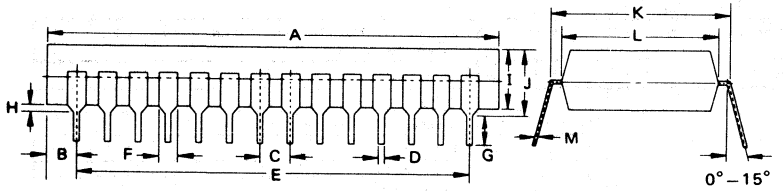
LOWER MEMORY INTERRUPT VECTOR ADDRESS

	INTERVAL = 4								INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	A_5	1	1	1	0	0	A_7	A_6	1	1	1	0	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0	A_7	A_6	1	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0	A_7	A_6	1	0	1	0	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0	A_7	A_6	1	0	0	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0	A_7	A_6	0	1	1	0	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0	A_7	A_6	0	1	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0	A_7	A_6	0	0	1	0	0	0
IR_0	A_7	A_6	A_5	0	0	0	0	0	A_7	A_6	0	0	0	0	0	0

FIGURE 4

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259A's.

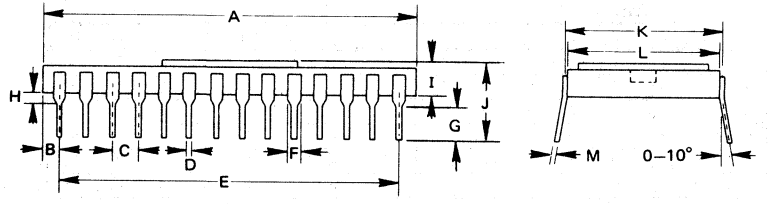




PACKAGE OUTLINE
μPD8259AC

Plastic

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



μPD8259AD

Ceramic

ITEM	MILLIMETERS	INCHES
A	36.2 MAX.	1.43 MAX.
B	1.59 MAX.	0.06 MAX.
C	2.54 ± 0.1	0.1 ± 0.004
D	0.46 ± 0.01	0.02 ± 0.004
E	33.02 ± 0.1	1.3 ± 0.004
F	1.02 MIN.	0.04 MIN.
G	3.2 MIN.	0.13 MIN.
H	1.0 MIN.	0.04 MIN.
I	3.5 MAX.	0.14 MAX.
J	4.5 MAX.	0.18 MAX.
K	15.24 TYP.	0.6 TYP.
L	14.93 TYP.	0.59 TYP.
M	0.25 ± 0.05	0.01 ± 0.002

PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

DESCRIPTION

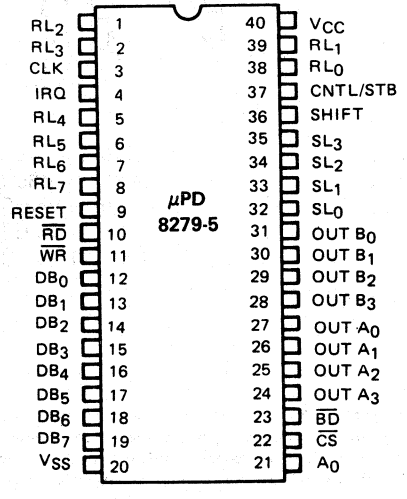
The μPD8279-5 is a programmable keyboard and display Input/Output device. It provides the user with the ability to display data on alphanumeric segment displays or simple indicators. The display RAM can be programmed as 16 x 8 or a dual 16 x 4 and loaded or read by the host processor. The display can be loaded with right or left entry with an auto-increment of the display RAM address.

The keyboard interface provides a scanned signal to a 64 contact key matrix expandable to 128. General sensors or strobed keys may also be used. Keystrokes are stored in an 8 character FIFO and can be either 2 key lockout or N key rollover. Keyboard entries generate an interrupt to the processor.

FEATURES

- Programmable by Processor
- 32 HEX or 16 Alphanumeric Displays
- 64 Expandable to 128 Keyboard
- Simultaneous Keyboard and Display
- 8 Character Keyboard – FIFO
- 2 Key Lockout or N Key Rollover
- Contact Debounce
- Programmable Scan Timer
- Interrupt on Key Entry
- Single +5 Volt Supply, ±10%
- Fully Compatible with 8080A, 8085A, μPD780 (Z80™)
- Available in 40 Pin Plastic Package

PIN CONFIGURATION



PIN NAMES

DB_{0-7}	Data Bus (Bi-directional)
CLK	Clock Input
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Buffer Address
IRQ	Interrupt Request Output
SL_{0-3}	Scan Lines
RL_{0-7}	Return Lines
SHIFT	Shift Input
CNTL/STB	Control/Strobe Input
OUT A_{0-3}	Display (A) Outputs
OUT B_{0-3}	Display (B) Outputs
$\overline{BD}$	Bland Display Output

9

TM: Z80 is a registered trademark of Zilog, Inc.

μPD8279-5

FUNCTIONAL DESCRIPTION

The μPD8279-5 has two basic functions: 1) to control displays to output and 2) to control a keyboard for input. Its specific purpose is to unburden the host processor from monitoring keys and refreshing displays. The μPD8279-5 is designed to directly interface the microprocessor bus. The microprocessor must program the operating mode to the μPD8279-5, these modes are as follows:

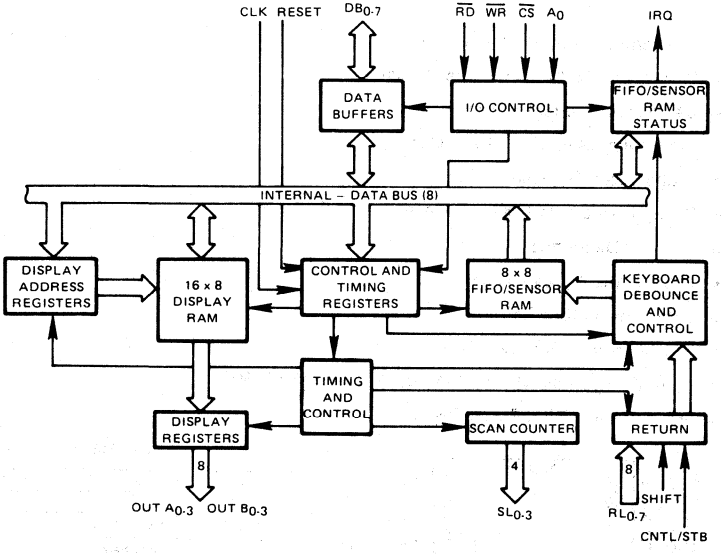
Output Modes

- 8 or 16 Character Display
- Right or Left Entry

Input Modes

- Scanned Keyboard with Encoded 8 x 8 x 4 Key Format or Decoded 4 x 8 x 8 Scan Lines.
- Scanned Sensor Matrix with Encoded 8 x 8 or Decoded 4 x 8 Scan Lines.
- Strobed Input.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.5 to +7 Volts①
All Input Voltages	-0.5 to +7 Volts①
Supply Voltages	-0.5 to +7 Volts①
Power Dissipation	1W

Note: ① With respect to V_{SS}

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN IDENTIFICATION

PIN			DESCRIPTION
NO.	SYMBOL	NAME	
1, 2, 5, 6, 7, 8, 38, 39	RL_{0-7}	Return Lines	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
3	CLK	Clock	Clock from system used to generate internal timing.
4	IRQ	Interrupt Request	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
9	Reset	Reset Input	A high signal on this pin resets the μPD8279-5.
10	$\overline{RD}$	Read Input	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
11	$\overline{WR}$	Write Input	
12-19	DB_{0-7}	Data Bus	Bi-Directional data bus. All data and commands between the processor and the μPD8279-5 are transmitted on these lines.
20	V_{SS}	Ground Reference	Power Supply Ground
21	A_0	Buffer Address	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
22	$\overline{CS}$	Chip Select	Chip Select. A low on this pin enables the interface functions to receive or transmit.
23	$\overline{BD}$	Blank Display Output	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.
24-27	$OUT\ A_{0-3}$	Display A Outputs	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4-bit ports may be blanked independently. These two ports may also be considered as one 8-bit port.
28-31	$OUT\ B_{0-3}$	Display B Outputs	
32-35	SL_{0-3}	Scan Lines	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
36	Shift	Shift Input	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
37	CNTL/STB	Control/ Strobe Input	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in Strobed input mode (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
40	V_{CC}	+5V Input	Power Supply Input

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage for Return Lines	V_{IL1}	-0.5		1.4	V	
Input Low Voltage (Others)	V_{IL2}	-0.5		0.8	V	
Input High Voltage for Return Lines	V_{IH1}	2.2			V	
Input High Voltage (Others)	V_{IH2}	2.0			V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage on Interrupt Line	IRQ Pin	+3.5			V	I_{OH} = -50μA
		+2.4			V	I_{OH} = -400μA
	OTHERS	+2.4			V	I_{OH} = -400μA
Input Current on Shift, Control and Return Lines	I_{IL1}			+10	μA	V_{IN} = V_{CC}
				-100	μA	V_{IN} = 0V
Input Leakage Current (Others)	I_{IL2}			±10	μA	V_{IN} = V_{CC} to 0V
Output Float Leakage	I_{OFL}			±10	μA	V_{OUT} = V_{CC} to 0V
Power Supply Current	I_{CC}			120	mA	

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}	5		10	pF	V_{IN} = V_{CC}
Output Capacitance	C_{OUT}	10		20	pF	V_{OUT} = V_{CC}

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

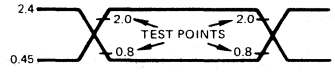
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable Before $\overline{READ}$	t_{AR}	0			ns	
Address Hold Time for $\overline{READ}$	t_{RA}	0			ns	
$\overline{READ}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{READ}$	t_{RD}			150	ns	C_L = 150 pF
Address to Data Valid	t_{AD}			250	ns	C_L = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	10		100	ns	
Read Cycle Time	t_{RCY}	1			μs	
WRITE						
Address Stable Before $\overline{WRITE}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	0			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	250			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	0			ns	
Write Cycle Time		1μs				
OTHER						
Clock Pulse Width	$t_{\phi W}$	120			ns	
Clock Period	t_{CY}	320			ns	

GENERAL TIMING

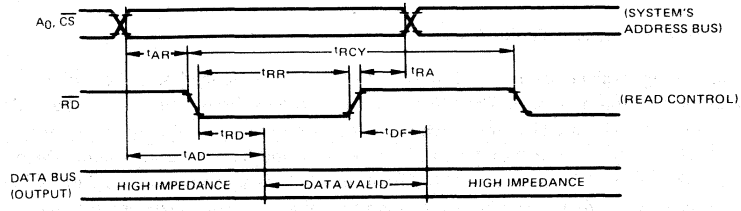
Keyboard Scan Time:	5.1 ms	Digit-on Time:	480 μs
Keyboard Debounce Time:	10.3 ms	Blanking Time:	160 μs
Key Scan Time:	80 μs	Internal Clock Cycle:	10 μs
Display Scan Time:	10.3 ms		

TIMING WAVEFORMS

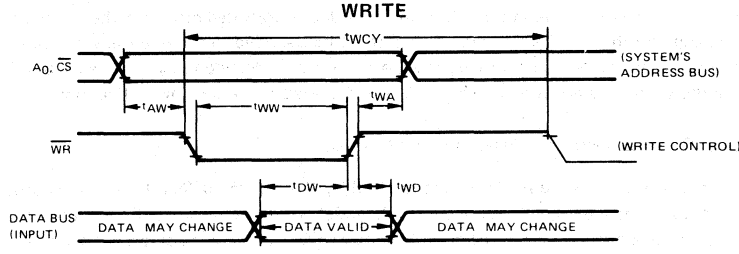
INPUT FOR AC TESTS



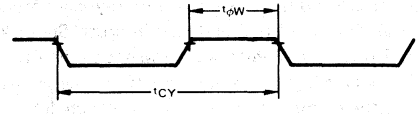
READ



WRITE



CLOCK INPUT



9

OPERATIONAL DESCRIPTION

The following is a description of each section of the μPD8279-5. See the block diagram for functional reference.

I/O Control and Data Buffers

Communication to and from the μPD8279-5 is performed by selecting $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$. The type of information written or read by the processor is selected by A_0. A logic 0 states that information is data while a 1 selects command or status. $\overline{RD}$ and $\overline{WR}$ select the direction by which the transfer occurs through the Data Buffers. When the chip is deselected ($\overline{CS}$ = 1) the bi-directional Data Buffers are in a high impedance state thus enabling the μPD8279-5 to be tied directly to the processor data bus.

Timing Registers and Timing Control

The Timing Registers store the display and keyboard modes and other conditions programmed by the processor. The timing control contains the timing counter chain. One counter is a divide by N scaler which may be programmed to match the processor cycle time. The scaler must take a value between 2 and 31 in binary. A value which scales the internal frequency to 100 KHz gives a 5.1 ms scan time and 10.3 ms switch debounce. The other counters divide down to make key, row matrix and display scans.

Scan Counter

The scan counter can operate in either the encoded or decoded mode. In the encoded mode, the counter provides a count which must be decoded to provide the scan lines. In the decoded mode, the counter provides a 1 out of 4 decoded scan. In the encoded mode the scan lines are active high and in the decoded mode they are active low.

Return Buffers, Keyboard Debounce and Control

The eight return lines are buffered and latched by the return buffers. In the keyboard mode these lines are scanned sampling for key closures in each row. If the debounce circuit senses a closure, about 10 ms are timed out and a check is performed again. If the switch is still pressed, the address of the switch matrix plus the status of shift and control are written into the FIFO. In the scanned sensor mode, the contents of return lines are sent directly to the sensor RAM (FIFO) each key scan. In the strobed mode, the transfer takes place on the rising edge of CNTL/STB.

FIFO/Sensor RAM and Status

This section is a dual purpose 8 x 8 RAM. In strobe or keyboard mode it is a FIFO. Each entry is pushed into the FIFO and read in order. Status keeps track of the number of entries in the FIFO. Too many reads or writes to the FIFO will be treated as an error condition. The status logic generates an IRQ whenever the FIFO has an entry. In the sensor mode the memory is a sensor RAM which detects changes in the status of a sensor. If a change occurs, the IRQ is generated until the change is acknowledged.

Display Address Registers and Display RAM

The Display Address Register contains the address of the word being read or written by the processor, as well as the word being displayed. This address may be programmed to auto-increment after each read or write. The display RAM may be read by the processor any time after the mode and address is set. Data entry to the display RAM may be set to either right or left entry.

COMMAND OPERATION

The commands programmable to the μPD8279-5 via the data bus with $\overline{CS}$ active (0) and A_0 high are as follows:

Keyboard/Display Mode Set

0	0	0	D	D	K	K	K

MSB LSB

Display Mode:

DD

0	0	8-8-bit character display – Left entry
0	1 ①	16-8 bit character display – Left entry
1	0	8-8 bit character display – Right entry
1	1	16-8 bit character display – Right entry

Note: ① Power on default condition

Keyboard Mode:

KKK

0	0	0	Encoded Scan – 2 Key Lockout
0	0	1	Decoded Scan – 2 Key Lockout
0	1	0	Encoded Scan – N Key Rollover
0	1	1	Decoded Scan – N Key Rollover
1	0	0	Encoded Scan-Sensor Matrix
1	0	1	Decoded Scan-Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

0	0	1	P	P	P	P	P

Where PPPPP is the prescaler value between 2 and 31 this prescaler divides the external clock by PPPPP to develop its internal frequency. After reset, a default value of 31 is generated.

Read FIFO/Sensor RAM

0	1	0	A1	X	A	A	A

$A_0 = 0$

A_1 is the auto-increment flag. AAA is the row to be read by the processor. The read command is accomplished with ($\overline{CS} \cdot RD \cdot \overline{A0}$) by the processor. If A_1 is 1, the row select counter will be incremented after each read. Note that auto-incrementing has no effect on the display.

Read Display RAM

0	1	1	A1	A	A	A	A

$A_0 = 0$

Where A_1 is the auto-increment flag and AAAA is the character which the processor is about to read.

Write Display RAM

1	0	0	A1	A	A	A	A

where AAAA is the character the processor is about to write.

Display Write Inhibit Blanking

1	0	1	X	IW A	IW B	BL A	BL B

Where IWA and IWB are Inhibit Writing nibble A and B respectively, and BLA, BLB are blanking. When using the display as a dual 4-bit, it is necessary to mask one of the 4-bit halves to eliminate interaction between the two halves. This is accomplished with the IW flags. The BL flags allow the programmer to blank either half of the display independently. To blank a display formatted as a single 8-bit, it is necessary to set both BLA and BLB. Default after a reset is all zeros. All signals are active high (1).

Clear

1	1	0	C_D	C_D	C_D	C_F	C_A

C_D	C_D	C_D	
1	0	X	All zeros
1	1	0	AB = 20_{16}
1	1	1	All ones
0	X	X	Disable clear display

This command is used to clear the display RAM, the FIFO, or both. The C_D options allow the user the ability to clear the display RAM to either all zeros or all ones.

C_F clears the FIFO.
C_A clears all.

Clearing the display takes one complete display scan. During this time the processor can't write to the display RAM.

C_F will set the FIFO empty flag and reset IRQ. The sensor matrix mode RAM pointer will then be set to row 0.

C_A is equivalent to C_F and C_D. The display is cleared using the display clear code specified and resets the internal timing logic to synchronize it.

End Interrupt/Error Mode Set

1	1	1	E	X	X	X	X

In the sensor matrix mode, this instruction clears IRQ and allows writing into RAM.

In N key rollover, setting the E bit to 1 allows for operating in the special Error mode. See Description of FIFO status.

FIFO Status

D_U	S/E	O	U	F	N	N	N

Where: D_U = Display Unavailable because a clear display or clear all command is in progress.
S/E = Sensor Error flag due to multiple closure of switch matrix.
O = FIFO Overrun since an attempt was made to push too many characters into the FIFO.
U = FIFO Underrun. An indication that the processor tried to read an empty FIFO.
F = FIFO Full Flag.
NNN = The Number of characters presently in the FIFO.

The FIFO Status is Read with A_0 high and $\overline{CS}$, $\overline{RD}$ active low.

The Display not available is an indication that the C_D or C_A command has not completed its clearing. The S/E flags are used to show an error in multiple closures has occurred. The O or U, overrun or underrun, flags occur when too many characters are written into the FIFO or the processor tries to read an empty FIFO. F is an indication that the FIFO is full and NNN is the number of characters in the FIFO.

Data Read

Data can be read during A_0 = 0 and when $\overline{CS}$, $\overline{RD}$ are active low. The source of the data is determined by the Read Display or Read FIFO commands.

Data Write

Data is written to the chip when A_0, $\overline{CS}$, and $\overline{WR}$ are active low. Data will be written into the display RAM with its address selected by the latest Read or Write Display command.

COMMAND OPERATION (CONT.)

Data Format

CNTL	SH	SCAN	RET

In the Scanned Key mode, the characters in the FIFO correspond to the above format where CNTL and SH are the most significant bits and the SCAN and return lines are the scan and column counters.

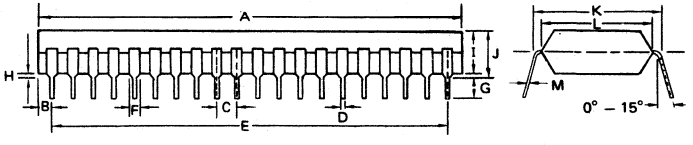
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

In the Sensor Matrix mode, the data corresponds directly to the row of the sensor RAM being scanned. Shift and control (SH, CNTL) are not used in this mode.

Control Address Summary

A_0	MSB			DATA				LSB	
1	0	0	0	D	D	K	K	K	Keyboard Display Mode Set
1	0	0	1	P	P	P	P	P	Load Program Clock
0	0	1	0	A_1	X	A	A	A	Read FIFO/Sensor RAM
0	0	1	1	A_1	A	A	A	A	Read Display RAM
1	1	0	0	A_1	A	A	A	A	Write Display RAM
1	1	0	1	X	IW A	IW B	BL A	BL B	Display Write Inhibit/Blanking
1	1	1	0	C_D	C_D	C_D	C_F	C_A	Clear
1	1	1	1	E	X	X	X	X	End Interrupt/Error Mode Set
1	D_U	S/E	O	U	F	N	N	N	FIFO Status

PACKAGE OUTLINE μPD8279-5C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$

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8279-5DS-REV1-1-82-CAT

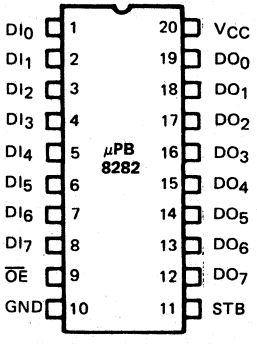
OCTAL LATCH

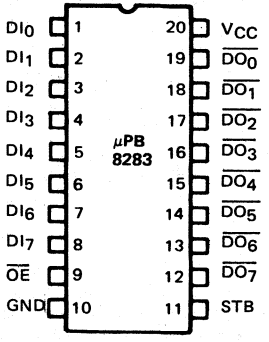
DESCRIPTION

The μPB8282/8283 are 8-bit latches with tri-state output buffers. The 8282 is non-inverting and the 8283 inverts the input data. These devices are ideal for demuxing the address/data buses on the 8085A/8086 microprocessors.
The 8282/8283 are fabricated using NEC's Schottky bipolar process.

FEATURES

- Supports 8080, 8085A, 8048, 8086 Family Systems
- Transparent During Active Strobe
- Fully Parallel 8-Bit Data Register and Buffer
- High Output Drive Capability (32 mA) for Driving the System Data Bus
- Tri-State Outputs
- 20-Pin Package





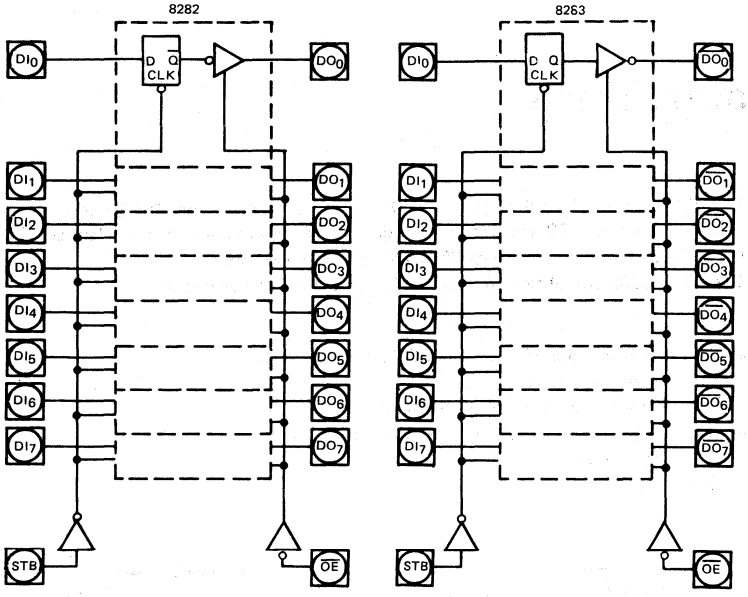
PIN NAMES

DI_0-DI_7	DATA IN
DO_0DO_7	DATA OUT
$\overline{OE}$	OUTPUT ENABLE
STB	STROBE

FUNCTIONAL DESCRIPTION

The μPB8282/8283 are 8-bit latches with tri-state output buffers. Data on the inputs is latched into the data latches on a high to low transition of the STB line. When STB is high, the latches appear transparent. The $\overline{OE}$ input enables the latched data to be transferred to the output pins. When $\overline{OE}$ is high, the outputs are put in the tri-state condition. $\overline{OE}$ will not cause transients to appear on the data outputs.

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to 5.5V
T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Conditions: V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Clamp Voltage	V_C		−1	V	I_C = −5 mA
Power Supply Current	I_{CC}		160	mA	
Forward Input Current	I_F		−0.2	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	V_R = 5.25V
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 32 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −5 mA
Output Off Current	I_{OFF}		±50	μA	V_{OFF} = 0.45 to 5.25V
Input Low Voltage	V_{IL}		0.8	V	V_{CC}=5.0V①
Input High Voltage	V_{IH}	2.0		V	V_{CC}=5.0V①
Input Capacitance	C_{IN}		12	pF	V_{BIAS}=2.5V, V_{CC}=5V, T_a=25°C, F=1 MHz

Note: ① Output Loading I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF

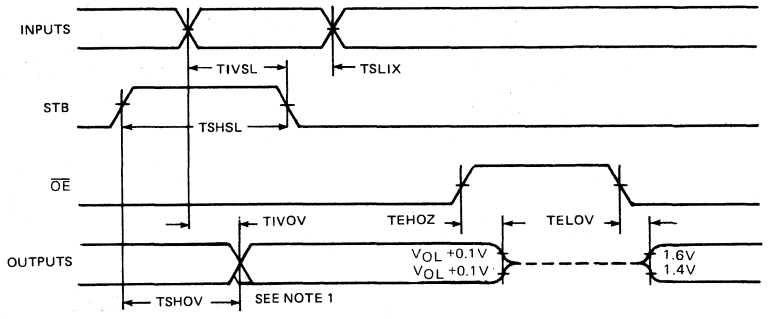
AC CHARACTERISTICS

Conditions: V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

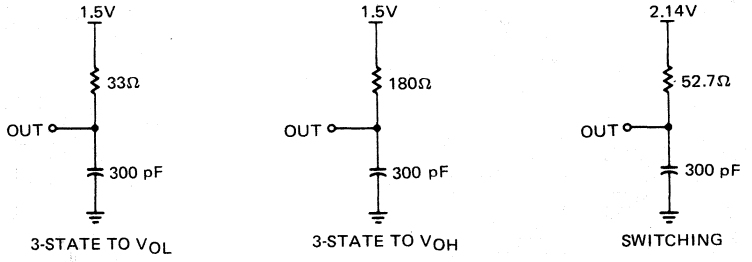
Loading: Outputs – I_{OL} = 32 mA, I_{OH} = –5 mA, C_L = 300 pF

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input to Output Delay	TIVOV	5		
—Inverting			22	ns
—Non-Inverting		5	30	ns
STB to Output Delay	TSHOV			
—Inverting		10	40	ns
—Non-Inverting		10	45	ns
Output Disable Time	TEHOZ	5	22	ns
Output Enable Time	TELOV	10	30	ns
Input to STB Setup Time	TIVSL	0		ns
Input to STB Hold Time	TSLIX	25		ns
STB High Time	TSHSL	15		ns
Input, Output Rise Time	T_{ILIH}, T_{OLOH}		20	ns
Input, Output Fall Time	T_{IHIL}, T_{OHOL}		12	nw

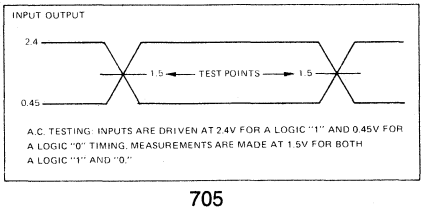
TIMING WAVEFORMS



Note: Output may be momentarily invalid following the high going into STB transition.



AC TESTING INPUT, OUTPUT WAVEFORM



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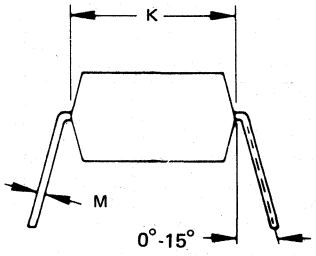
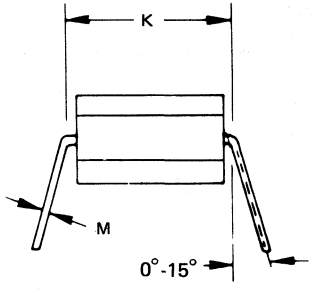


Plastic

ITEM	MILLIMETERS	INCHES
A	26.7 MAX.	1.05 MAX.
B	1.05	0.041
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	22.86	0.9
F	1.4	0.055
F'	1.1	0.043
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	3.55	0.14
J	5.08 MAX.	0.2 MAX.
K	7.62	0.3
L	6.4	0.25
M	0.25 + 0.10 − 0.05	0.01 + 0.004 −0.002
R	1.0R	0.04R

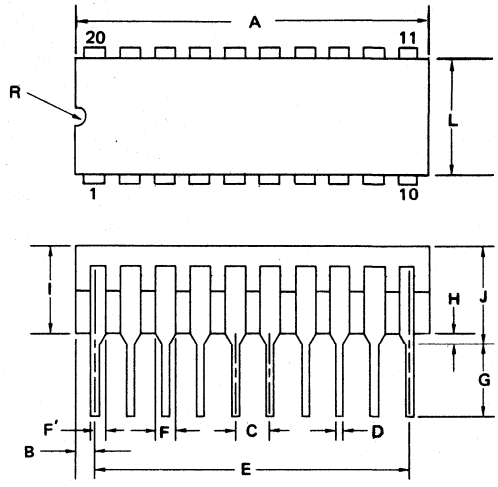


Cerdip

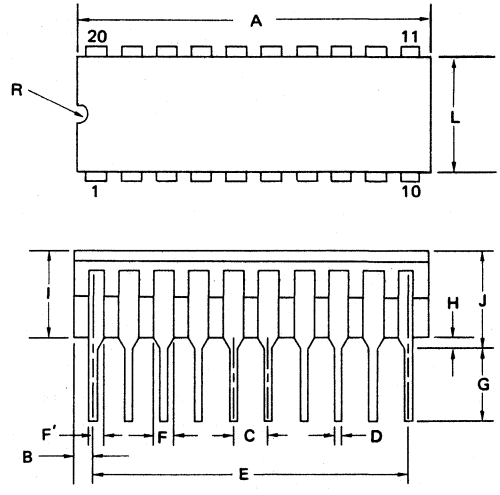
ITEM	MILLIMETERS	INCHES
A	26.7 MAX.	1.05 MAX.
B	0.7	0.028
C	2.54	0.1
D	0.46 ± 0.1	0.018 ± 0.004
E	22.86	0.9
F	1.4	0.055
F'	0.9	0.035
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.32 MAX.	0.17 MAX.
J	5.08 MAX.	0.2 MAX.
K	7.62	0.3
L	6.8	0.27
M	0.25 + 0.10 − 0.05	0.01 + 0.004 −0.002
R	0.8R	0.03R

PACKAGE OUTLINES

μPB8282C
μPB8283C



μPB8282D
μPB8283D



8282/8283DS/REV1/-1-82-CAT

CLOCK GENERATOR AND DRIVER FOR 8086/8088 MICROPROCESSORS

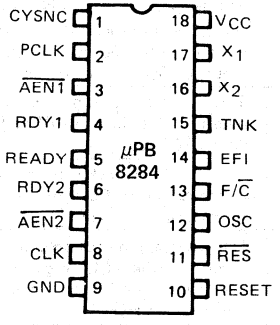
DESCRIPTION

The μPB8284 is a clock generator and driver for the 8086 and 8088 microprocessors This bipolar driver provides the microprocessor with a reset signal and also provides properly synchronized READY timing. A TTL clock is also provided for peripheral devices.

FEATURES

- Generate System Clock for the 8086 and 8088
- Frequency Source can be a Crystal or a TTL Signal
- MOS Level Output for the Processor
- TTL Level Output for Peripheral Devices
- Power-Up Reset for the Processor
- READY Synchronization
- +5V Supply
- 18 Pin Package

PIN CONFIGURATION



PIN NAMES

X_1, X_2	Crystal Connections
TANK	For Overtone Crystal
F/$\overline{C}$	Clock Source Select
EFI	External Clock Input
CSYNC	Clock Synchronization Input
RDY1, RDY2	Ready Signal from Multibus™* Systems
$\overline{AEN1}$, $\overline{AEN2}$	Address Enable Qualifiers for the two RDY Signals
$\overline{RES}$	Reset Input
RESET	Synchronized Reset Output
OSC	Oscillator Output
CLK	MOS Clock for the Processor
PCLK	TTL Clock for Peripherals
READY	Synchronized Ready Output

*TM - Multibus is a trademark of Intel Corporation.

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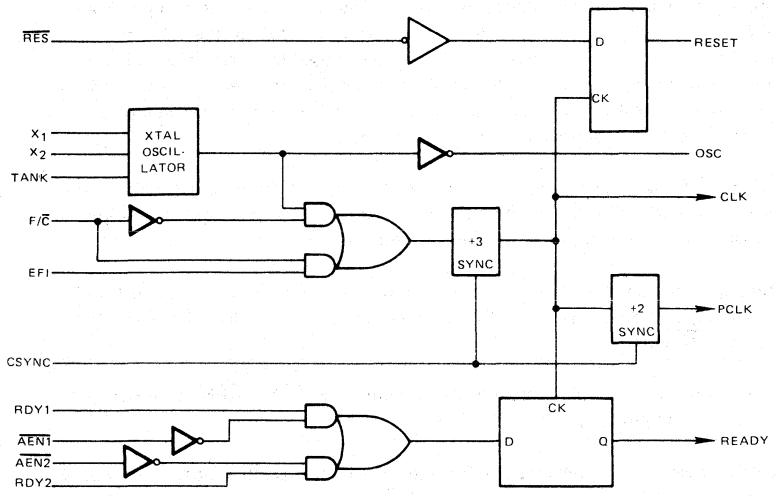
PIN IDENTIFICATION

NO.	SYMBOL	NAME	FUNCTION
1	CSYNC	Clock Synchronization	An active high signal which allows multiple 8284s to be synchronized. When CYSNC is low, the internal counters count and when high the counters are reset. CYSNC should be grounded when the internal oscillator is used.
2	PCLK	Peripheral Clock	A TTL level clock for use with peripheral devices. This clock is one-half the frequency of CLK.
3, 7	$\overline{AEN1}$, $\overline{AEN2}$	Address Enable	This active low signal is used to qualify its respective RDY inputs. If there is only one bus to interface to, $\overline{AEN}$ inputs are to be grounded.
4, 6	RDY1, RDY2	Bus Ready	This signal is sent to the 8284 from a peripheral device on the bus to indicate that data has been received or data is available to be read.
5	READY	Ready	The READY signal to the microprocessor is synchronized by the RDY inputs to the processor CLK. READY is cleared after the guaranteed hold time to the processor has been met.
8	CLK	Processor Clock	This is the MOS level clock output of 33% duty cycle to drive the microprocessor and bipolar support devices (8288) connected to the processor. The frequency of CLK is one third of the crystal or EFI frequency.
10	RESET	Reset	This is used to initialize the processor. Its input is derived from an RC connection to a Schmitt trigger input for power up operation.
11	$\overline{RES}$	Reset In	This Schmitt trigger input is used to determine the timing of RESET out via an RC circuit.
12	OSC	Oscillator Output	This TTL level clock is the output of the oscillator circuit running at the crystal frequency.
13	F/$\overline{C}$	Frequency Crystal Select	F/$\overline{C}$ is a strapping option used to determine where CLK is generated. A high is for the EFI input, and a low is for the crystal.
14	EFI	External Frequency In	A square wave in at three times the CLK output. A TTL level clock to generate CLK.
16, 17	X_1, X_2	Crystal In	A crystal is connected to these inputs to generate the processor clock. The crystal chosen is three times the desired CLK output.
15	TNK	Tank	This is used for overtone type crystals. (See diagram below.)
18	VCC	VCC	+5V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Conditions: T_a = 0°C to 70°C; V_{CC} = 5V ± 10%

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Forward Input Current	I_F		-0.5	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C		-1.0	V	I_C = -5 mA
Power Supply Current	I_{CC}		140	mA	
Input Low Voltage	V_{IL}		0.8	V	V_{CC} = 5.0V
Input High Voltage	V_{IH}	2.0		V	V_{CC} = 5.0V
Reset Input High Voltage	V_{IHR}	2.6		V	V_{CC} = 5.0V
Output Low Voltage	V_{OL}		0.45	V	5 mA = I_{OL}
Output High Voltage CLK Other Outputs	V_{OH}	4 2.4		V V	-1 mA, -1 mA } I_{OH}
$\overline{RES}$ Input Hysteresis	V_{IHR}-V_{ILR}	0.25		V	V_{CC} = 5.0V

FUNCTIONAL DESCRIPTION

The clock generator can provide the system clock from either a crystal or an external TTL source. There is an internal divide by three counter which receives its input from either the crystal or TTL source (EFI Pin) depending on the state of the F/$\overline{C}$ input strapping. There is also a clear input (C SYNC) which is used for either inhibiting the clock, or synchronizing it with an external event (or perhaps another clock generator chip). Note that if the TTL input is used, the crystal oscillator section can still be used for an independent clock source, using the OSC output.

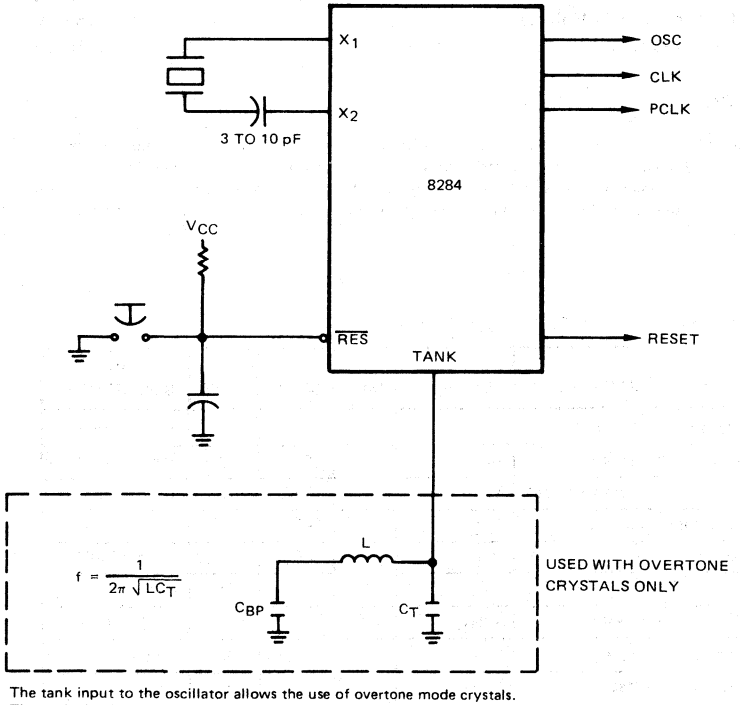
For driving the MOS output level, there is a 33% duty cycle MOS output (CLK) for the microprocessor, and a TTL output (PCLK) with a 50% duty cycle for use as a peripheral clock signal. This clock is at one half of the processor clock speed.

Reset timing is provided by a Schmitt Trigger input ($\overline{RES}$) and a flip-flop to synchronize the reset timing to the falling edge of CLK. Power-on reset is provided by a simple RC circuit on the $\overline{RES}$ input.

There are two READY inputs, each with its own qualifier ($\overline{AEN1}$, $\overline{AEN2}$). The unused $\overline{AEN}$ signal should be tied low.

The READY logic in the 8284 synchronizes the RDY1 and RDY2 asynchronous inputs to the processor clock to insure proper set up time, and to guarantee proper hold time before clearing the ready signal.

TANK INSERT CIRCUIT DIAGRAM



The tank input to the oscillator allows the use of overtone mode crystals. The tank circuit shunts the crystal's fundamental and high overtone frequencies and allows the third harmonic to oscillate. The external LC network is connected to the TANK input and is AC coupled to ground.

AC CHARACTERISTICS

Conditions: $T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

TIMING REQUIREMENTS

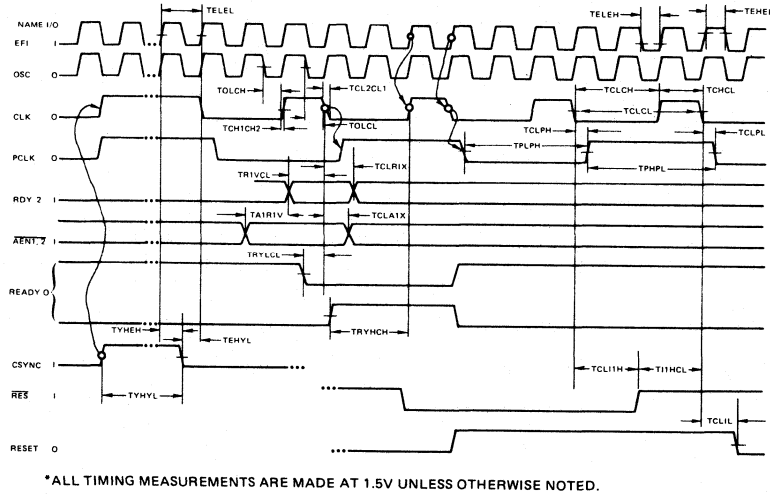
PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
External Frequency High Time	TEHEL	13		ns	90%-90% V_{IN}
External Frequency Low Time	TELEH	13		ns	10%-10% V_{IN}
EFI Period	TELEL	TEHEL + TELEH + δ		ns	①
XTAL Frequency		12	25	MHz	
RDY1, RDY2 Set-Up to CLK	TR1VCL	35		ns	
RDY1, RDY2 Hold to CLK	TCLR1X	0		ns	
AEN1, AEN2 Set-Up to RDY1, RDY2	TA1VR1V	15		ns	
AEN1, AEN2 Hold to CLK	TCLA1X	0		ns	
CSYNC Set-Up to EFI	TYHEH	20		ns	
CSYNC Hold to EFI	TEHYL	20		ns	
CSYNC Width	TYHYL	2 TELEL		ns	
RES Set-Up to CLK	TI1HCL	65		ns	②
RES Hold to CLK	TCLI1H	20		ns	②

TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
CLK Cycle Period	TCLCL	125		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2.0		ns	Figure 1 and Figure 2
CLK Low Time	TCLCH	(2/3 TCLCL) −15.0		ns	Figure 1 and Figure 2
CLK Rise and Fall Time	TCH1CH2 TCL2CL1		10	ns	1.0V to 3.5V
PCLK High Time	TPHPL	TCLCL −20		ns	
PCLK Low Time	TPLPH	TCLCL −20		ns	
Ready Inactive to CLK ④	TRYLCL	−8		ns	Figure 3 and Figure 4
Ready Active to CLK ③	TRYHCH	(2/3 TCLCL) −15.0		ns	Figure 3 and Figure 4
CLK To Reset Delay	TCLIL		40	ns	
CLK to PCLK High Delay	TCLPH		22	ns	
CLK to PCLK Low Delay	TCLPL		22	ns	
OSC to CLK High Delay	TOLCH	−5	12	ns	
OSC to CLK Low Delay	TOLCL	2	22	ns	

Notes: ① δ = EFI rise (5 ns max) + EFI fall (5 ns max).
② Set up and hold only necessary to guarantee recognition at next clock.
③ Applies only to T3 and TW states.
④ Applies only to T2 states.

TIMING WAVEFORMS*



*ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

AC TEST CIRCUITS

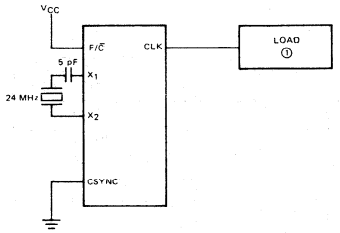


FIGURE 1
CLOCK HIGH AND LOW TIME

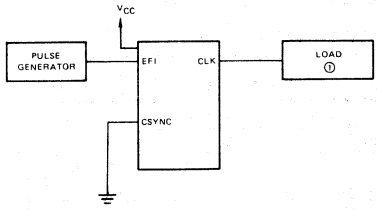


FIGURE 2
CLOCK HIGH AND LOW TIME

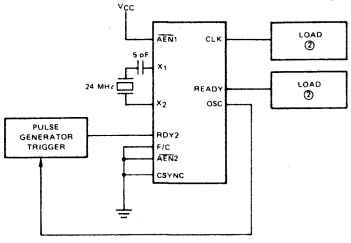


FIGURE 3
READY TO CLK

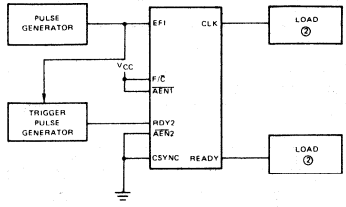
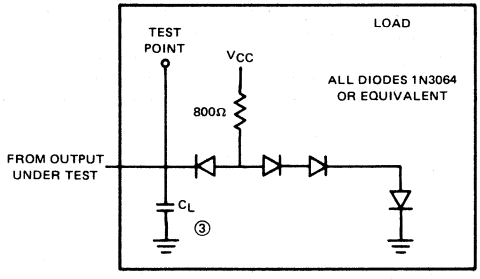


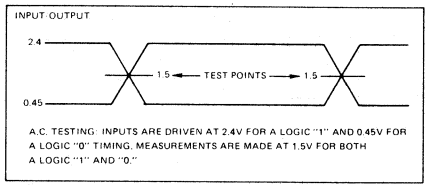
FIGURE 4
READY TO CLK



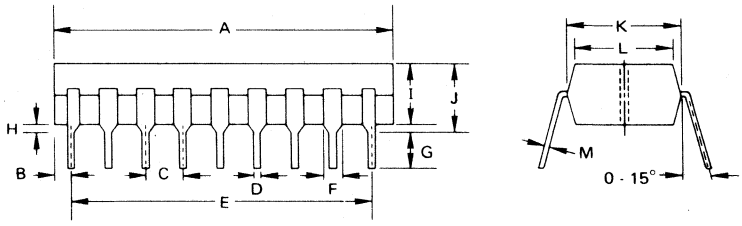
OUTPUT

NOTES: ① C_L = 100 pF
② C_L = 30 pF
③ C_L INCLUDES PROBE AND JIG CAPACITANCE

AC TESTING INPUT, OUTPUT WAVEFORM



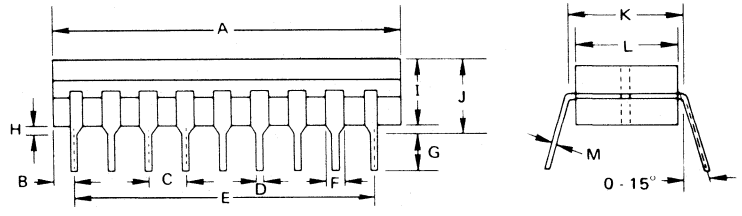
PACKAGE OUTLINES
μPB8284C



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN
H	0.5 MIN.	0.02 MIN
I	4.6 MAX.	0.18 MAX
J	5.1 MAX.	0.2 MAX
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPB8284D



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN
H	0.5 MIN.	0.02 MIN
I	4.6 MAX.	0.18 MAX
J	5.1 MAX.	0.2 MAX
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

9

CLOCK GENERATOR AND DRIVER FOR 8086/8088 MICROPROCESSORS

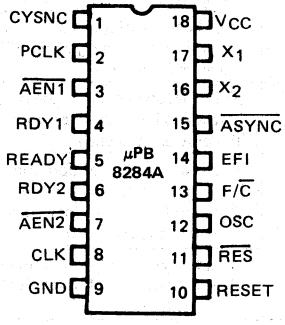
DESCRIPTION

The μPB8284A is a clock generator and driver for the 8066 and 8088 microprocessors. This bipolar driver provides the microprocessor with a reset signal and also provides properly synchronized READY timing. A TTL clock is also provided for peripheral devices.

FEATURES

- Generate System Clock for the 8086 and 8088
- Frequency Source can be a Crystal or a TTL Signal
- MOS Level Output for the Processor
- TTL Level Output for Peripheral Devices
- Power-Up Reset for the Processor
- READY Synchronization
- +5V Supply
- 18 Pin Package

PIN CONFIGURATION



PIN NAMES

X_1, X_2	Crystal Connections
TANK	For Overtone Crystal
F/C	Clock Source Select
EFI	External Clock Input
CSYNC	Clock Synchronization Input
RDY1, RDY2	Ready Signal from Multibus™* Systems
AEN1, AEN2	Address Enable Qualifiers for the two RDY Signals
RES	Reset Input
RESET	Synchronized Reset Output
OSC	Oscillator Output
CLK	MOS Clock for the Processor
PCLK	TTL Clock for Peripherals
READY	Synchronized Ready Output

*TM - Multibus is a trademark of Intel Corporation.

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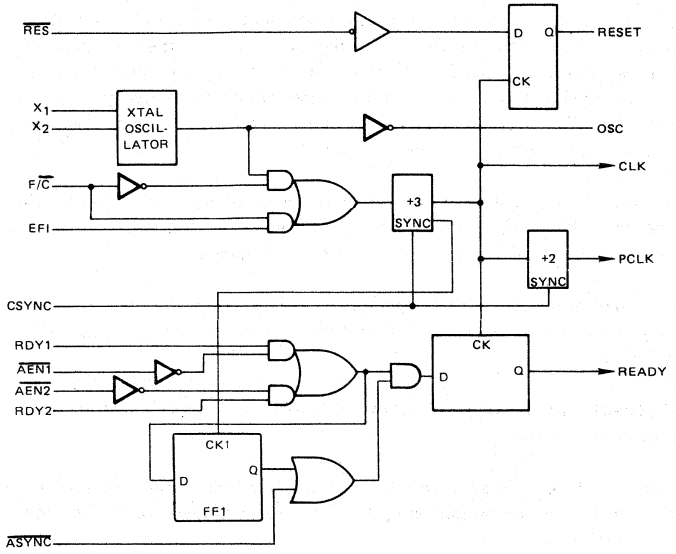
PIN IDENTIFICATION

NO.	SYMBOL	NAME	FUNCTION
1	CSYNC	Clock Synchronization	An active high signal which allows multiple 8284s to be synchronized. When CYSNC is low, the internal counters count and when high the counters are reset. CYSNC should be grounded when the internal oscillator is used.
2	PCLK	Peripheral Clock	A TTL level clock for use with peripheral devices. This clock is one-half the frequency of CLK.
3, 7	$\overline{AEN1}$, $\overline{AEN2}$	Address Enable	This active low signal is used to qualify its respective RDY inputs. If there is only one bus to interface to, $\overline{AEN}$ inputs are to be grounded.
4, 6	RDY1, RDY2	Bus Ready	This signal is sent to the 8284 from a peripheral device on the bus to indicate that data has been received or data is available to be read.
5	READY	Ready	The READY signal to the microprocessor is synchronized by the RDY inputs to the processor CLK. READY is cleared after the guaranteed hold time to the processor has been met.
8	CLK	Processor Clock	This is the MOS level clock output of 33% duty cycle to drive the microprocessor and bipolar support devices (8288) connected to the processor. The frequency of CLK is one third of the crystal or EFI frequency.
10	RESET	Reset	This is used to initialize the processor. Its input is derived from an RC connection to a Schmitt trigger input for power up operation.
11	$\overline{RES}$	Reset In	This Schmitt trigger input is used to determine the timing of RESET out via an RC circuit.
12	OSC	Oscillator Output	This TTL level clock is the output of the oscillator circuit running at the crystal frequency.
13	F/$\overline{C}$	Frequency Crystal Select	F/$\overline{C}$ is a strapping option used to determine where CLK is generated. A high is for the EFI input, and a low is for the crystal.
14	EFI	External Frequency In	A square wave in at three times the CLK output. A TTL level clock to generate CLK.
16, 17	X_1, X_2	Crystal In	A crystal is connected to these inputs to generate the processor clock. The crystal chosen is three times the desired CLK output.
15	$\overline{ASYNC}$	Asynchronous Input	Ready Synchronization Select. $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, 2 stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH, a single stage of READY synchronization is provided.
18	VCC	VCC	+5V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Conditions: $T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Forward Input Current	I_F		-0.5	mA	$V_F = 0.45V$
Reverse Input Current	I_R		50	μA	$V_R = 5.25V$
Input Forward Clamp Voltage	V_C		-1.0	V	$I_C = -5$ mA
Power Supply Current	I_{CC}		140	mA	
Input Low Voltage	V_{IL}		0.8	V	$V_{CC} = 5.0V$
Input High Voltage	V_{IH}	2.0		V	$V_{CC} = 5.0V$
Reset Input High Voltage	V_{IHR}	2.6		V	$V_{CC} = 5.0V$
Output Low Voltage	V_{OL}		0.45	V	5 mA = I_{OL}
Output High Voltage CLK Other Outputs	V_{OH}	4 2.4		V V	-1 mA -1 mA } I_{OH}
$\overline{RES}$ Input Hysteresis	V_{IHR}-V_{ILR}	0.25		V	$V_{CC} = 5.0V$

9

FUNCTIONAL DESCRIPTION

The clock generator can provide the system clock from either a crystal or an external TTL source. There is an internal divide by three counter which receives its input from either the crystal or TTL source (EFI Pin) depending on the state of the F/$\overline{C}$ input strapping. There is also a clear input (C SYNC) which is used for either inhibiting the clock, or synchronizing it with an external event (or perhaps another clock generator chip). Note that if the TTL input is used, the crystal oscillator section can still be used for an independent clock source, using the OSC output.

For driving the MOS output level, there is a 33% duty cycle MOS output (CLK) for the microprocessor, and a TTL output (PCLK) with a 50% duty cycle for use as a peripheral clock signal. This clock is at one half of the processor clock speed.

Reset timing is provided by a Schmitt Trigger input ($\overline{RES}$) and a flip-flop to synchronize the reset timing to the falling edge of CLK. Power-on reset is provided by a simple RC circuit on the $\overline{RES}$ input.

There are two READY inputs, each with its own qualifier ($\overline{AEN1}$, $\overline{AEN2}$). The unused $\overline{AEN}$ signal should be tied low.

The READY logic in the 8284A synchronizes the RDY1 and RDY2 asynchronous inputs to the processor clock to insure proper set up time, and to guarantee proper hold time before clearing the ready signal.

AC CHARACTERISTICS

Conditions: T_a = 0°C to 70°C; V_{CC} = 5V ± 10%

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
External Frequency High Time	TEHEL	13		ns	90%-90% V_{IN}
External Frequency Low Time	TELEH	13		ns	10%-10% V_{IN}
EFI Period	TELEL	TEHEL + TELEH + δ		ns	(1)
XTAL Frequency		12	25	MHz	
RDY1, RDY2 Set-Up to CLK	TR1VCL	35		ns	
RDY1, RDY2 Hold to CLK	TCLR1X	0		ns	
AEN1, AEN2 Set-Up to RDY1, RDY2	TA1VR1V	15		ns	
AEN1, AEN2 Hold to CLK	TCLA1X	0		ns	
CSYNC Set-Up to EFI	TYHEH	20		ns	
CSYNC Hold to EFI	TEHYL	20		ns	
CSYNC Width	TYHYL	2 TELEL		ns	
RES Set-Up to CLK	TI1HCL	65		ns	(2)
RES Hold to CLK	TCLI1H	20		ns	(2)
RDY1, RDY2 Active Set-Up to CLK	t_{R1VCH}	35		ns	$\overline{ASYNC}$ = LOW
RDY1, RDY2 Inactive Set-Up to CLK	t_{R1VCL}	35		ns	
$\overline{ASYNC}$ Set-Up to CLK	t_{AYVCL}	50		ns	
$\overline{ASYNC}$ Hold to CLK	t_{CLAYX}	0		ns	
Input Rise Time	t_{ILIH}		20	ns	From 0.8V to 2.0V
Input Fall Time	t_{IHIL}		12	ns	From 2.0V to 0.8V

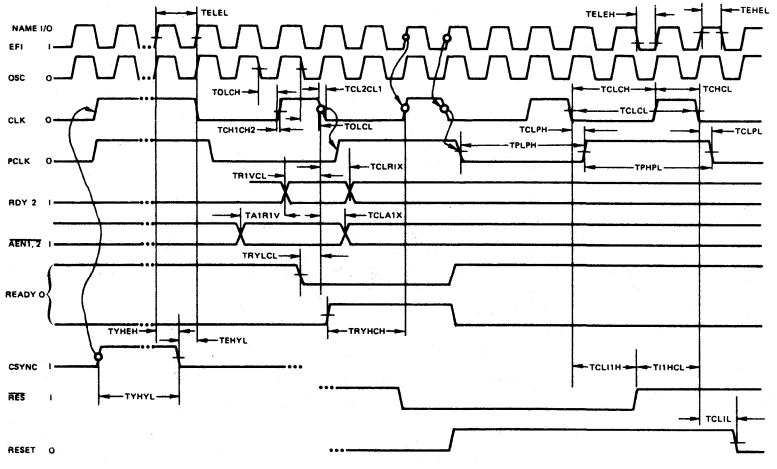
AC CHARACTERISTICS (CONT.)

TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
CLK Cycle Period	TCLCL	125		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2.0		ns	Figure 3 and Figure 4
CLK Low Time	TCLCH	(2/3 TCLCL) −15.0		ns	Figure 3 and Figure 4
CLK Rise and Fall Time	TCH1CH2 TCL2CL1		10	ns	1.0V to 3.5V
PCLK High Time	TPHPL	TCLCL −20		ns	
PCLK Low Time	TPLPH	TCLCL −20		ns	
Ready Inactive to CLK (4)	TRYLCL	−8		ns	Figure 5 and Figure 6
Ready Active to CLK (3)	TRYHCH	(2/3 TCLCL) −15.0		ns	Figure 5 and Figure 6
CLK To Reset Delay	TCLIL		40	ns	
CLK to PCLK High Delay	TCLPH		22	ns	
CLK to PCLK Low Delay	TCLPL		22	ns	
OSC to CLK High Delay	TOLCH	−5	12	ns	
OSC to CLK Low Delay	TOLCL	2	22	ns	
Output Rise Time (except CLK)	t_{OLOH}		20	ns	From 0.8V to 2.0V
Output Fall Time (except CLK)	t_{OHOL}		12	ns	From 2.0V to 0.8V

Notes:
(1) δ = EFI rise (5 ns max) + EFI fall (5 ns max).
(2) Set up and hold only necessary to guarantee recognition at next clock.
(3) Applies only to T3 and TW states.
(4) Applies only to T2 states.

TIMING WAVEFORM*



*ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

9

AC TEST CIRCUITS

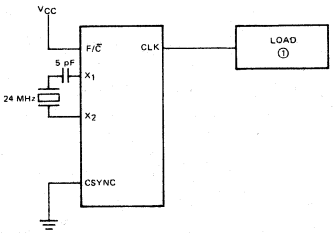


FIGURE 1
CLOCK HIGH AND LOW TIME

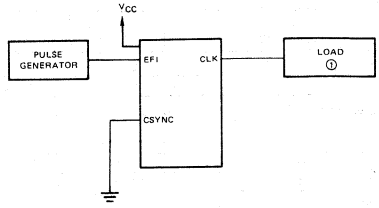


FIGURE 2
CLOCK HIGH AND LOW TIME

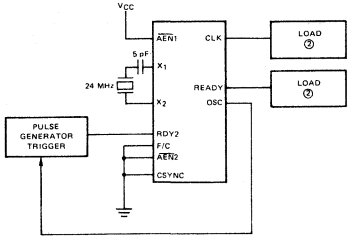


FIGURE 3
READY TO CLK

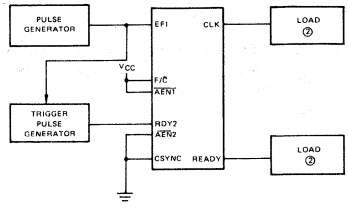
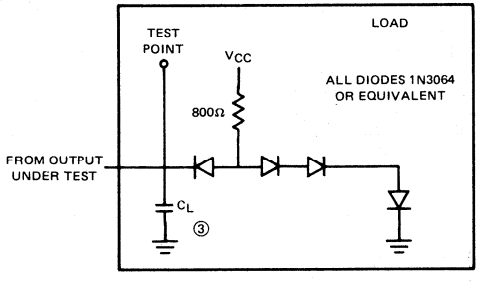


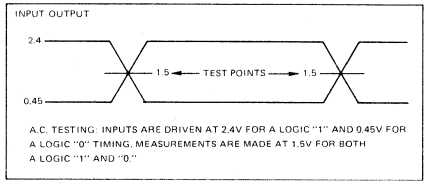
FIGURE 4
READY TO CLK



OUTPUT

NOTES: ① C_L = 100 pF
② C_L = 30 pF
③ C_L INCLUDES PROBE AND JIG CAPACITANCE

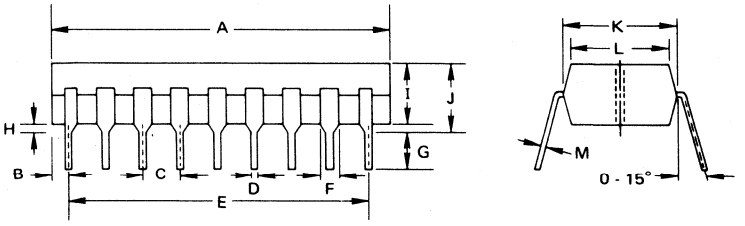
AC TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0."

PACKAGE OUTLINES

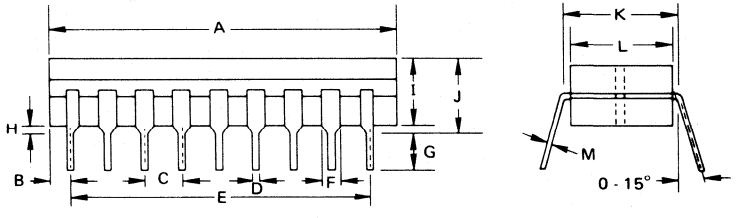
μPB8284AC



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPB8284AD



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

9

8-BIT BUS TRANSCEIVER

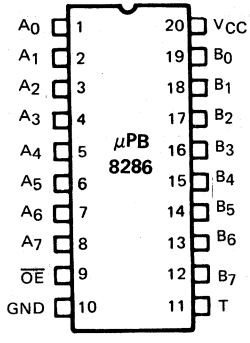
DESCRIPTION

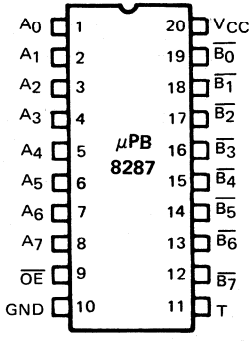
The 8286 and 8287 are octal bus transceivers used for buffering microprocessor bus lines. Being bi-directional, they are ideal for buffering the data bus lines on 8- or 16-bit microprocessors. Each B output is capable of driving 32 mA low or 5 mA high.

FEATURES

- Data Bus Buffer Driver for μCOM-8 (8080, 8085A, 780) and μCOM-16 (8086) families
- Low Input Load Current — 0.2 mA max
- High Output Drive Capability for Driving System Data Bus
- Tri-State Outputs
- 20 Pin Package with Fully Parallel 8-Bit Transceivers

PIN CONFIGURATIONS



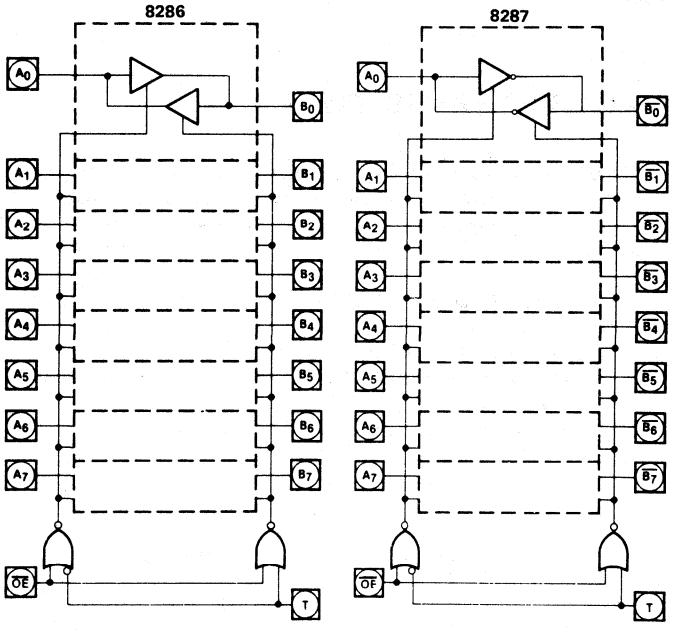


PIN NAMES

A_0-A_7	Local Bus Data
B_0-B_7	System Bus Data
$\overline{OE}$	Output Enable
T	Transmit

9

BLOCK DIAGRAMS



$\overline{OE}$	T	RESULT
0	0	B → A
0	1	A → B
1	0	A and B HIGH IMPEDANCE
1	1	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
All Output and Supply Voltages. . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

PARAMETER		SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Clamp Voltage		V_C		−1	V	$I_C = -5$ mA
Power Supply Current	− 8287	I_{CC}		130	mA	
	− 8286	I_{CC}		160	mA	
Forward Input Current		I_F		−0.2	mA	$V_F = 0.45V$
Reverse Input Current		I_R		50	μA	$V_R = 5.25V$
Output Low Voltage	− B Outputs	V_{OL}		0.45	V	$I_{OL} = 32$ mA
	− A Outputs			0.45	V	$I_{OL} = 16$ mA
Output High Voltage	− B Outputs	V_{OH}	2.4		V	$I_{OH} = -5$ mA
	− A Outputs		2.4		V	$I_{OH} = -1$ mA
Output Off Current		I_{OFF}		I_F		$V_{OFF} = 0.45V$
Output Off Current		I_{OFF}		I_R		$V_{OFF} = 5.25V$
Input Low Voltage	− A Side	V_{IL}		0.8	V	$V_{CC} = 5.0V$ ①
	− B Side	V_{IL}		0.9	V	$V_{CC} = 5.0V$ ①
Input High Voltage		V_{IH}	2.0		V	$V_{CC} = 5.0V$ ① $F = 1$ MHz
Input Capacitance	− A Side	C_{IN}		16	pF	$V_{BIAS} = 2.5V$, $V_{CC} = 5V$ $T_a = 25°C$ $F = 1$ MHz

Note: ① B Outputs – $I_{OL} = 32$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF
A Outputs – $I_{OL} = 16$ mA, $I_{OH} = -1$ mA, $C_L = 100$ pF

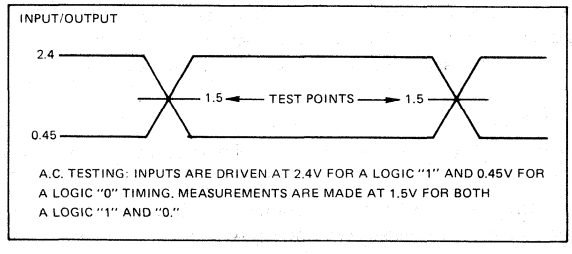
AC CHARACTERISTICS

$T_a = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

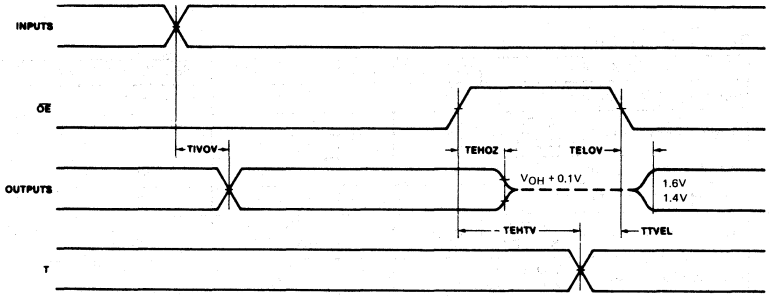
SYMBOL	PARAMETER	MIN	MAX	UNITS
TIVOV	Input to Output Delay			
	Inverting	5	22	ns
	Non-Inverting	5	30	ns
TEHTV	Transmit/Receive Hold Time	TEHOZ		ns
TTVEL	Transmit/Receive Setup	10		ns
TEHOZ	Output Disable Time	5	22	ns
TELOV	Output Enable Time	10	30	ns
TILIH, TOLOH	Input Output Rise Time		20	ns
TIHIL, TOHOL	Input Output Fall Time		12	ns

Notes: See waveforms and test load circuit.
B Outputs – $I_{OL} = 32$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF
A Outputs – $I_{OL} = 16$ mA, $I_{OH} = -1$ mA, $C_L = 100$ pF

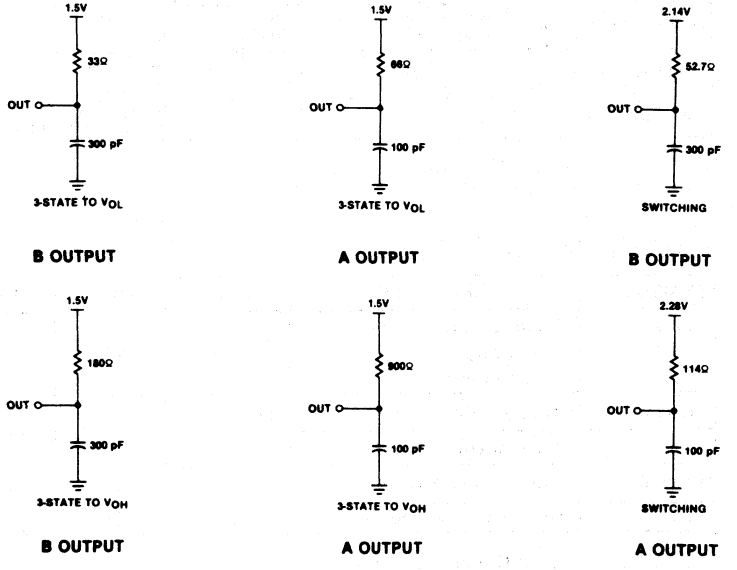
AC TESTING INPUT, OUTPUT WAVEFORM



WAVEFORMS



TEST LOAD CIRCUITS



FUNCTIONAL DESCRIPTION

MOS microprocessors like the 8080/8085A/8086 are generally capable of driving a single TTL load. This also applies to MOS memory devices. While sufficient for minimum type small systems on a single PC board, it is usually necessary to buffer the microprocessor and memory signals when a system is expanded or signals go to other PC boards.
These octal bus transceivers are designed to do the necessary buffering.

Bi-Directional Driver

Each buffered line of the octal driver consists of two separate tri-state buffers. The B side of the driver is designed to drive 32 mA and interface the system side of the bus to I/O, memory, etc. The A side is connected to the microprocessor.

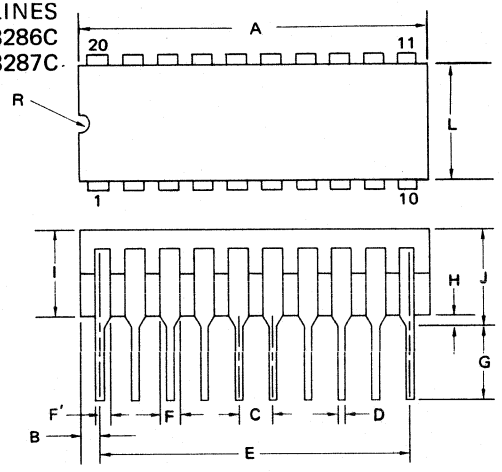
Control Gating, $\overline{OE}$, T

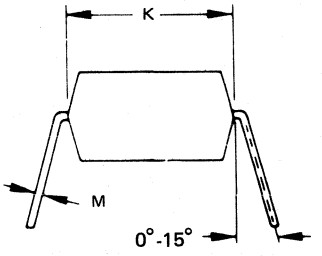
The $\overline{OE}$ (output enable) input is an active low signal used to enable the drivers selected by T on to the respective bus.

T is an input control signal used to select the direction of data through the transceivers. When T is high, data is transferred from the A_0-A_7 inputs to the B_0-B_7 outputs, and when low, data is transferred from B_0-B_7 to the A_0-A_7 outputs.

PACKAGE OUTLINES

μPB8286C
μPB8287C

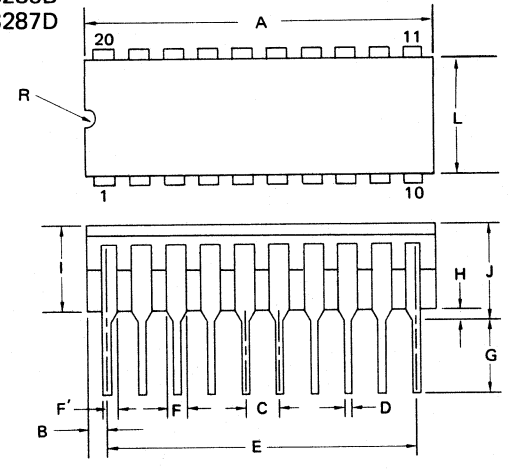


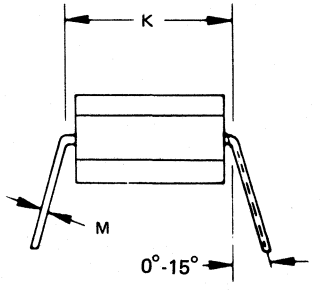


Plastic

ITEM	MILLIMETERS	INCHES
A	26.7 MAX.	1.05 MAX.
B	1.05	0.041
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	22.86	0.9
F	1.4	0.055
F'	1.1	0.043
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	3.55	0.14
J	5.08 MAX.	0.2 MAX.
K	7.62	0.3
L	6.4	0.25
M	0.25 + 0.10 - 0.05	0.01 + 0.004 -0.002
R	1.0R	0.04R

μPB8286D
μPB8287D





Cerdip

ITEM	MILLIMETERS	INCHES
A	26.7 MAX.	1.05 MAX.
B	0.7	0.028
C	2.54	0.1
D	0.46 ± 0.1	0.018 ± 0.004
E	22.86	0.9
F	1.4	0.055
F'	0.9	0.035
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.32 MAX.	0.17 MAX.
J	5.08 MAX.	0.2 MAX.
K	7.62	0.3
L	6.8	0.27
M	0.25 + 0.10 - 0.05	0.01 + 0.004 -0.002
R	0.8R	0.03R

μPD8086/8088 CPU SYSTEM BUS CONTROLLER

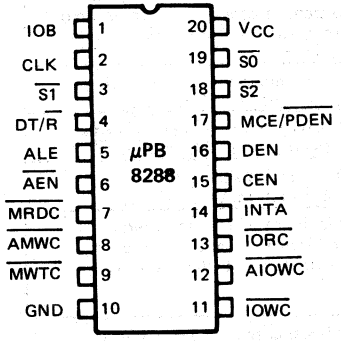
DESCRIPTION

The μPB8288 bus controller is for use in medium to large μPD8086/8088 systems. This 20-pin bipolar component provides command and control timing generation, plus bipolar drive capability and optimal system performance. It provides both Multibus™ command signals and control outputs for the microprocessor system. There is an option to use the controller with a multi-master system bus and separate I/O bus.

FEATURES

- System Controller for μPD8086/8088 Systems
- Bipolar Drive Capability
- Provides Advanced Commands
- Tri-State Output Drivers
- Can be used with an I/O Bus
- Enables Interface to One or Two Multi-Master Buses
- 20-Pin Package

PIN CONFIGURATION



PIN NAMES

S0-S2	Status Input Pins
CLK	Clock
ALE	Address Latch Enable
DEN	Data Enable
DT/R	Data Transmit/Receive
AEN	Address Enable
CEN	Command Enable
IOB	I/O Bus Mode
AIOWC	Advanced I/O Write
IOWC	I/O Write Command
IORC	I/O Read Command
AMWC	Advanced Memory Write
MWTC	Memory Write Command
MRDC	Memory Read Command
INTA	Interrupt Acknowledge
MCE/PDEN	Master Cascade/Peripheral Data Enable

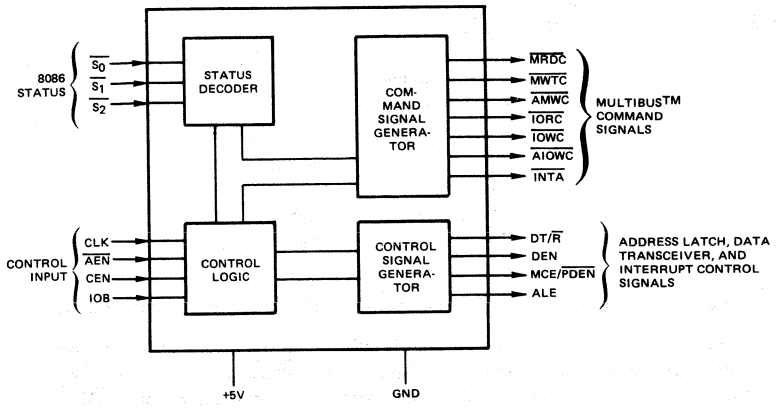
9

™ — Multibus is a trademark of Intel Corp.

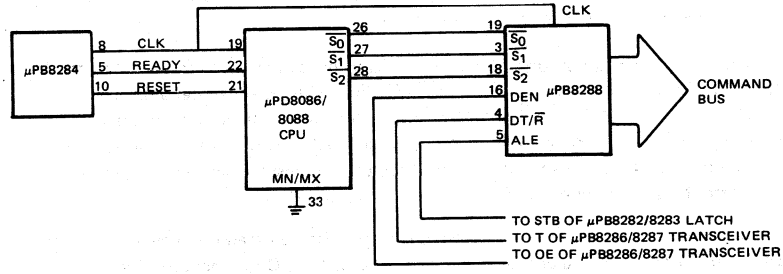
PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1	IOB	I/O Bus Mode	Sets mode of μPB8288, high for the I/O bus mode and low for the system bus mode.
2	CLK	Clock	The clock signal from the μPB8284 clock generator synchronizes the generation of command and control signals.
3, 19, 18	$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	Status Input Pins	The μPB8288 decodes these status lines from the μPB8086 to generate command and control signals. When not in use, these pins are high.
4	DT/$\overline{R}$	Data Transmit/Receive	This signal is used to control the bus transceivers in a system. A high for writing to I/O or memory and a low for reading data.
5	ALE	Address Latch Enable	This signal is used for controlling transparent D type latches (μPB8282/8283). It will strobe in the address on a high to low transition.
6	$\overline{AEN}$	Address Enable	In the I/O system bus mode, AEN enables the command outputs of the μPB8288 105 ns after it becomes active. If AEN is inactive, the command outputs are tri-stated.
7	$\overline{MRDC}$	Memory Read Command	This active low signal is for switching the data from memory to the data bus.
8	$\overline{AMWC}$	Advanced Memory Write Command	This is an advanced write command which occurs early in the machine cycle, with timing the same as the read command.
9	$\overline{MWTC}$	Memory Write Command	This is the memory write command to transfer data bus to memory, but not as early as $\overline{AMWC}$. (See timing waveforms.)
11	$\overline{IOWC}$	I/O Write Command	This command is for transferring information to I/O devices.
12	$\overline{AIOWC}$	Advanced I/O Write Command	This write command occurs earlier in the machine cycle than $\overline{IOWC}$.
13	$\overline{IORC}$	I/O Read Command	This signal enables the CPU to read data from an I/O device.
14	$\overline{INTA}$	Interrupt Acknowledge	This is to signal an interupting device to put the vector information on the data bus
15	CEN	Command Enable	This signal enables all command and control outputs. If CEN is low, these outputs are inactive.
16	DEN	Data Enable	This signal enables the data transceivers onto the bus.
17	MCE/$\overline{PDEN}$	Master Cascade Enable Peripheral Data Enable	Dual function pin system. MC/E – In the bus mode, this signal is active during an interrupt sequence to read the cascade address from the master interrupt controller onto the data bus. $\overline{PDEN}$ – In the I/O bus mode, it enables the transceivers for the I/O bus just as DEN enables bus transceivers in the system bus mode.

BLOCK DIAGRAM



CONNECTING THE BUS CONTROLLER TO THE CPU



ABSOLUTE MAXIMUM RATINGS*

OPERATING TEMPERATURE	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages ①	−0.5V to +7V
All Input Voltages ①	−1.0V to +5.5V

Note: ① With Respect to Ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9

FUNCTIONAL DESCRIPTION

The three status lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) from the μPD8086 CPU are decoded by the command logic to determine which command is to be issued. The following chart shows the decoding:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	μPD8086 State	μPB8288 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

There are two ways the command is issued depending on the mode of the μPB8288.

The I/O bus mode is enabled if the IOB pin is pulled high. In this mode, all I/O command lines are always enabled and not dependent upon $\overline{AEN}$. When the processor sends out an I/O command, the μPB8288 activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control any bus transceivers.

This mode is advantageous if I/O or peripherals dedicated to one microprocessor are in a multiprocessor system, allowing the μPB8288 to control two external buses. No waiting is required when the CPU needs access to the I/O bus, as an $\overline{AEN}$ low signal is needed to gain normal memory access.

If the IOB pin is tied to ground, the μPB8288 is in the system bus mode. In this mode, command signals are dependent upon the $\overline{AEN}$ line. Thus the command lines are activated 105 ns after the $\overline{AEN}$ line goes low. In this mode, there must be some bus arbitration logic to toggle the $\overline{AEN}$ line when the bus is free for use. Here, both memory and I/O are shared by more than one processor, over one bus, with both memory and I/O commands waiting for bus arbitration.

Among the command outputs are some advanced write commands which are initiated early in the machine cycle and can be used to prevent the CPU from entering unnecessary wait states.

The $\overline{INTA}$ signal acts as an I/O read during an interrupt cycle. This is to signal the interrupting device that its interrupt is being acknowledged, and to place the interrupt vector on the data bus.

The control outputs of the μPB8288 are used to control the bus transceivers in a system. DT/$\overline{R}$ determines the direction of the data transfer, and $\overline{DEN}$ is used to enable the outputs of the transceiver. In the IOB mode the MCE/$\overline{PDEN}$ pin acts as a dedicated data enable signal for the I/O bus.

The MCE signal is used in conjunction with an interrupt acknowledge cycle to control the cascade address when more than one interrupt controller (such as a μPD8259A) is used. If there is only one interrupt controller in a system, MCE is not used as the $\overline{INTA}$ signal gates the interrupt vector onto the processor bus. In multiple interrupt controller systems, MCE is used to gate the μPD8259A's cascade address onto the processors local bus, where ALE strobes it into the address latches. This occurs during the first $\overline{INTA}$ cycle. During the second $\overline{INTA}$ cycle the addressed slave μPD8259A gates its interrupt vector onto the processor bus.

The ALE signal occurs during each machine cycle and is used to strobe data into the address latches and to strobe the status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) into the μPB8288. ALE also occurs during a halt state to accomplish this.

The CEN (Command Enable) is used to control the command lines. If pulled high the μPB8288 functions normally and if grounded all command lines are inactive.

DC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Input Clamp Voltage	V_C		−1	V	I_C = −5 mA
Power Supply Current	I_{CC}		230	mA	
Forward Input Current	I_F		−0.7	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	V_R = V_{CC}
Output Low Voltage — Command Outputs Control Outputs	V_{OL}		0.5 0.5	V V	I_{OL} = 32 mA I_{OL} = 16 mA
Output High Voltage — Command Outputs Control Outputs	V_{OH}	2.4 2.4		V V	I_{OH} = −5 mA I_{OH} = −1 mA
Input Low Voltage	V_{IL}		0.8	V	
Input High Voltage	V_{IH}	2.0		V	
Output Off Current	I_{OFF}		100	μA	V_{OFF} = 0.4 to 5.25V

AC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	MAX	UNIT	LOADING
CLK Cycle Period	TCLCL	100		ns	
CLK Low Time	TCLCH	50		ns	
CLK High Time	TCHCL	30		ns	
Status Active Setup Time	TSVCH	35		ns	
Status Active Hold Time	TCHSV	10		ns	
Status Inactive Setup Time	TSHCL	35		ns	
Status Inactive Hold Time	TCLSH	10		ns	
Input Rise Time	T_{ILIH}		20	ns	
Input Fall Time	T_{IHIL}		12	ns	

TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNIT	LOADING
Control Active Delay	TCVNV	5	45	ns	
Control Inactive Delay	TCVNX	10	45	ns	
ALE MCE Active Delay (from CLK)	TCLLH, TCLMCH		20	ns	
ALE MCE Active Delay (from Status)	TSVLH, TSVMCH		20	ns	
ALE Inactive Delay	TCHLL	4	15	ns	
Command Active Delay	TCLML	10	35	ns	
Command Inactive Delay	TCLMH	10	35	ns	
Direction Control Active Delay	TCHDTL		50	ns	
Direction Control Inactive Delay	TCHDTH		30	ns	
Command Enable Time	TAELCH		40	ns	
Command Disable Time	TAEHCZ		40	ns	
Enable Delay Time	TAELCV	105	275	ns	
AEN to DEN	TAEVNV		25	ns	
CEN to DEN, PDEN	TCEVNV		20	ns	
CEN to Command	TCELRH		TCLML	ns	
Output Rise Time	T_{OLOH}		20	ns	
Output Fall Time	T_{OHOL}		12	ns	

$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF

Other: I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 80 pF

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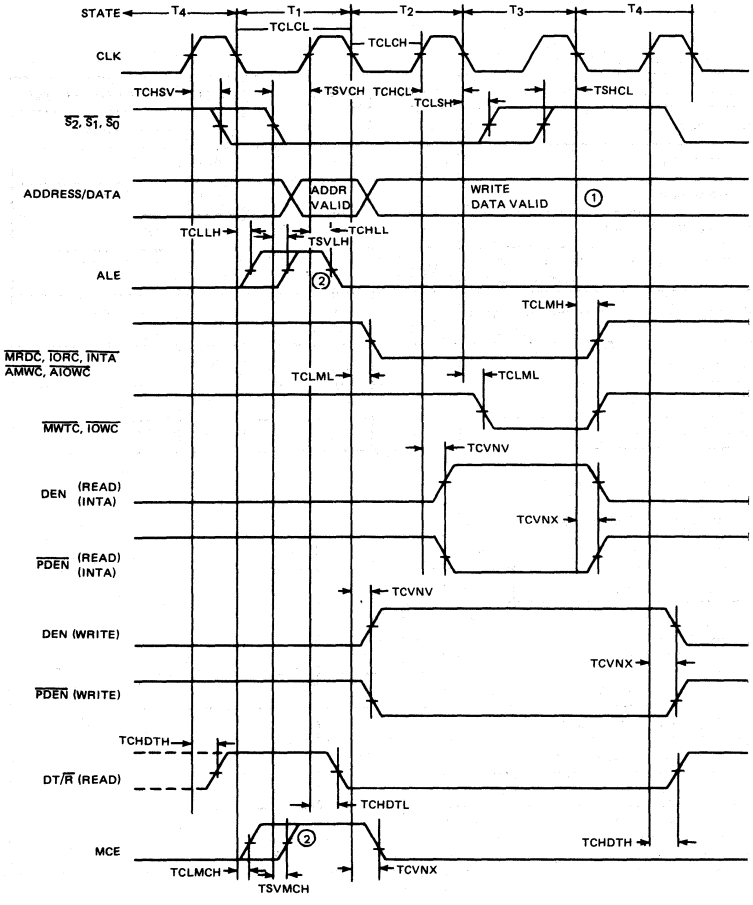
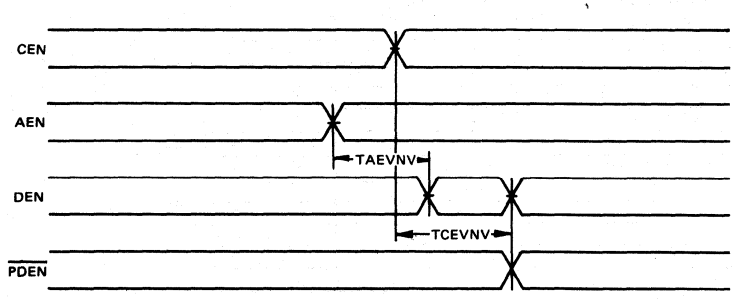
TIMING WAVEFORMS



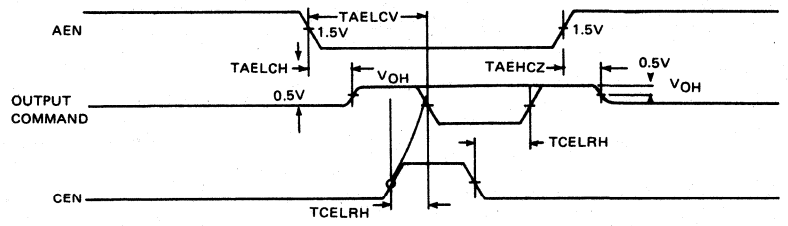
NOTES:

1. ADDRESS/DATA BUS IS SHOWN ONLY FOR REFERENCE PURPOSES.
2. LEADING EDGE OF ALE AND MCE IS DETERMINED BY THE FALLING EDGE OF CLK OR STATUS GOING ACTIVE, WHICHEVER OCCURS LAST.
3. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS SPECIFIED OTHERWISE.

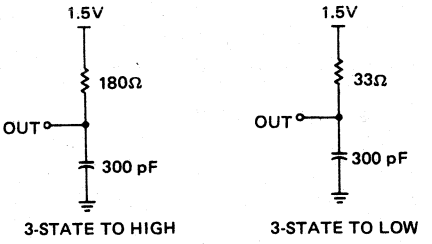
DEN, $\overline{\text{PDEN}}$ QUALIFICATION TIMING



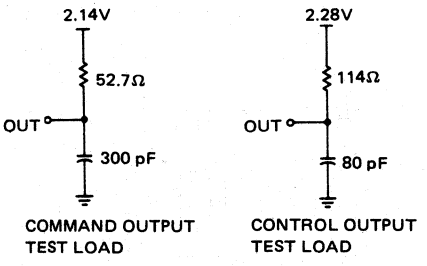
μPB8288 ADDRESS ENABLE ($\overline{AEN}$) TIMING (3-STATE ENABLE/DISABLE)



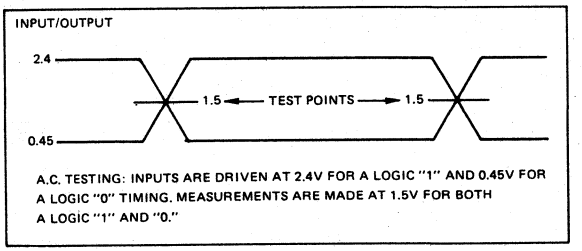
TEST LOAD CIRCUITS



3-STATE COMMAND OUTPUT TEST LOAD



AC TESTING INPUT, OUTPUT WAVEFORM



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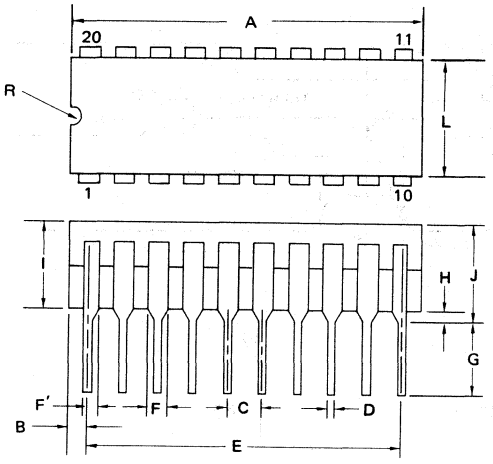
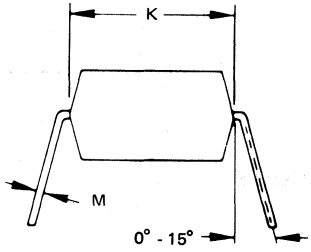
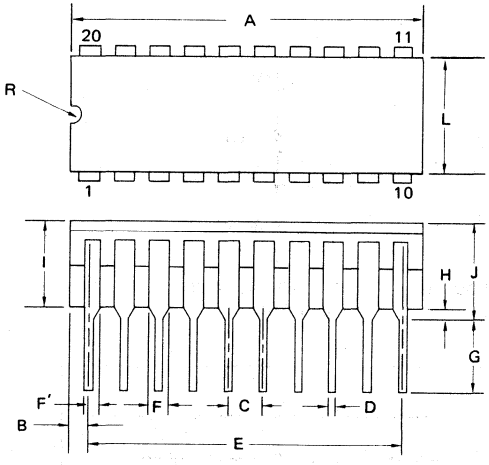
PACKAGE OUTLINES

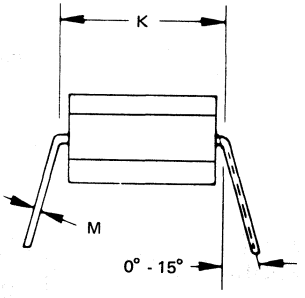




Plastic

ITEM	MILLIMETERS	INCHES
A	26.7 MAX.	1.05 MAX.
B	1.05	0.041
C	2.54	0.1
D	0.5 ± 0.1	0.02 + 0.004
E	22.86	0.9
F	1.4	0.055
F'	1.1	0.043
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	3.55	0.14
J	5.08 MAX.	0.2 MAX.
K	7.62	0.3
L	6.4	0.25
M	0.25 + 0.10 − 0.05	0.01 + 0.004 −0.002
R	1.0R	0.04R





Cerdip

ITEM	MILLIMETERS	INCHES
A	26.7 MAX.	1.05 MAX.
B	0.7	0.028
C	2.54	0.1
D	0.46 ± 0.1	0.018 ± 0.004
E	22.86	0.9
F	1.4	0.055
F'	0.9	0.035
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.32 MAX.	0.17 MAX.
J	5.08 MAX.	0.2 MAX.
K	7.62	0.3
L	6.8	0.27
M	0.25 + 0.10 − 0.05	0.01 + 0.004 −0.002
R	0.8R	0.03R

PRELIMINARY

μPB8289
BUS ARBITER

Description

The μPB8289 Bus Arbiter is used with the μPD8288 Bus Controller to interface 8086 and 8088 microprocessors to a multimaster system bus. The μPD8289 controls the μPD8288 bus controller and the bus transceivers and address latches, preventing them from accessing the system bus if the processor does not have use of the bus.

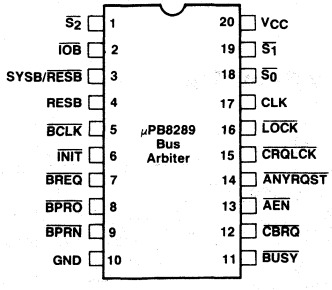
An external command sequence will cause the associated microprocessor to enter a wait state until the bus is ready. The processor remains in the wait state until the bus arbiter acquires use of the multimaster system bus. Then, the arbiter allows the bus controller, data transceivers, and address latches to access the system.

Once use of the bus has been acquired and data has been transferred, transfer acknowledge (XACK) is returned to the processor to indicate that the accessed slave device is ready. The processor may then complete its transfer cycle.

Features

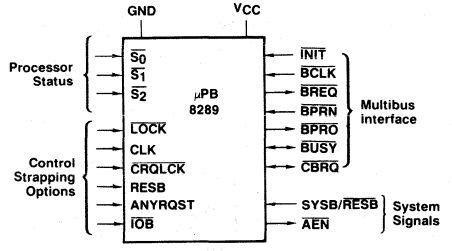
- ☐ Multimaster system bus protocol
- ☐ 8086 and 8088 processor synchronization with multimaster bus
- ☐ Simple interface with the 8288 bus controller and 8283/8282 address latches to a system bus
- ☐ Four operating modes for flexible system configuration
- ☐ Simplified interface to Multibus™ systems
- ☐ Parallel, Serial, and Rotating priority resolution
- ☐ Bipolar buffering and drive capability

Pin Configuration



TM: Multibus is a registered trademark of Intel Corporation.

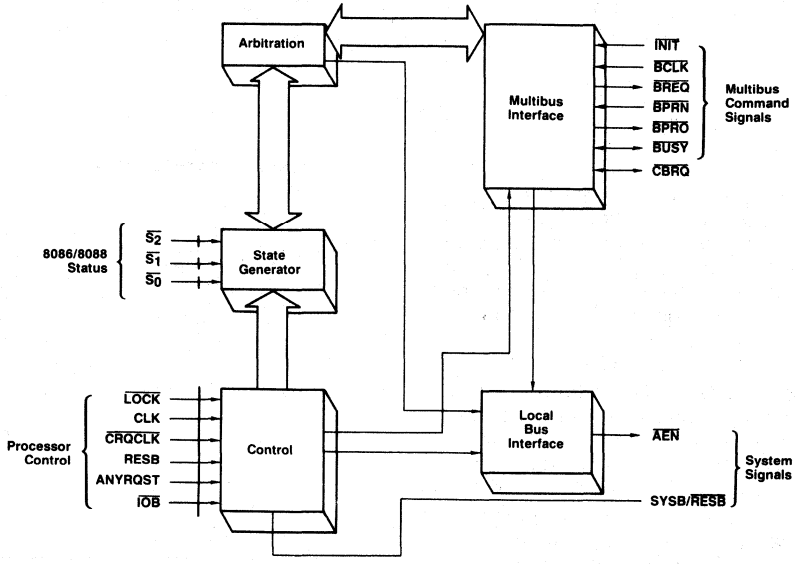
Functional Configuration



Pin Identification

Pin Number	Pin Name	Direction	Pin Functions
18, 19, 1	S0, S1, S2	IN	Status inputs from the 8086 or 8088 processor. The μPB8289 decodes them to begin bus requests and surrenders.
17	CLK	IN	Clock signal from the 8284 clock generator.
16	LOCK	IN	
15	CRQLCK	IN	Common Request Lock. Prevents the μPB8289 from surrendering the bus in response to request on the CBRQ input.
4	RESB	IN	Resident Bus Input. This signal tells the μPB8289 that there is a multimaster and resident bus. When this signal is high, the SYSB/RESB pin handles bus arbitration.
14	ANYRQST	IN	This signal allows the multimaster bus to be surrendered to a lower priority arbiter.
2	IOB	IN	I/O Bus. This signal tells the μPB8289 that there is an I/O peripheral bus and a multimaster system bus.
13	AEN	OUT	Address Enable. This output tells the 8288 bus controller, 8284 clock driver, and the processor's address latches when to tri-state their output drivers.
3	SYSB/RESB	IN	System Bus/Resident Bus. This signal determines when bus requests and surrenders are permitted in SR mode.
12	CBRQ	IN/OUT	Common Bus Request. This is an input from a lower priority arbiter requesting the bus. It is an output from arbiters that surrender the multimaster bus upon request.
6	INIT	IN	Initialize. This is an active low input that resets all bus arbiters on the multimaster bus. No arbiters have use of the bus following INIT.
5	BCLK	IN	System Bus Clock. This clock synchronizes all system bus interface signals.
7	BREQ	OUT	Bus Request. This output is used by an arbiter to request use of the multimaster system bus.
9	BPRN	IN	Bus Priority In. This signal tells the arbiter it may acquire the bus on the next falling edge of BCLK.

Block Diagram



Pin Functions (Cont.)

Pin Number	Pin Name	Direction	Pin Functions
8	$\overline{BPRO}$	OUT	Bus Priority Out. In serial priority resolving schemes, this output daisy-chains to $\overline{BPRN}$ of the next lower priority arbiter.
11	$\overline{BUSY}$	IN/OUT	Busy notifies all arbiters on the bus when the bus is available. The highest requesting arbiter seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off the bus.
20	V_{CC}	IN	+5V
10	GND	IN	Ground

Bus Master Arbitration

Higher priority masters generally acquire use of the bus when a lower priority master completes its present transfer cycle. Lower priority masters acquire the bus when no higher priority master is accessing the system bus. The ANYRQST strapping option allows the arbiter to surrender the bus to a lower priority master as if it were a higher priority master. The arbiter maintains the bus as long as no other bus masters are requesting the bus and its processor has not entered the Halt state. The arbiter does not voluntarily surrender the bus and must be forced off by a request from another bus master, unless the arbiter's processor has entered the Halt state. Additional strapping options allow for other sets of conditions.

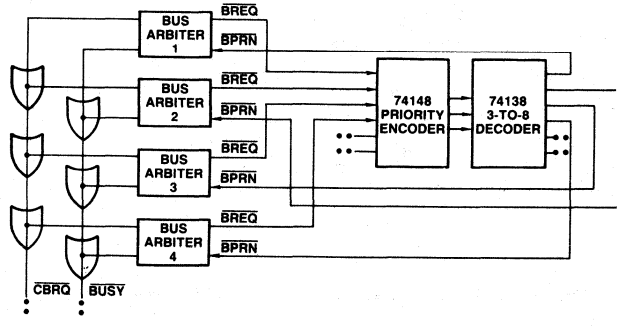
Priority Resolving Techniques

The μPB8289 provides several techniques for resolving priority between the many possible bus masters of a multimaster system bus. All of these techniques assume that one bus master will have priority over all others at any given time. You may use Parallel, Serial, or Rotating Priority Resolving.

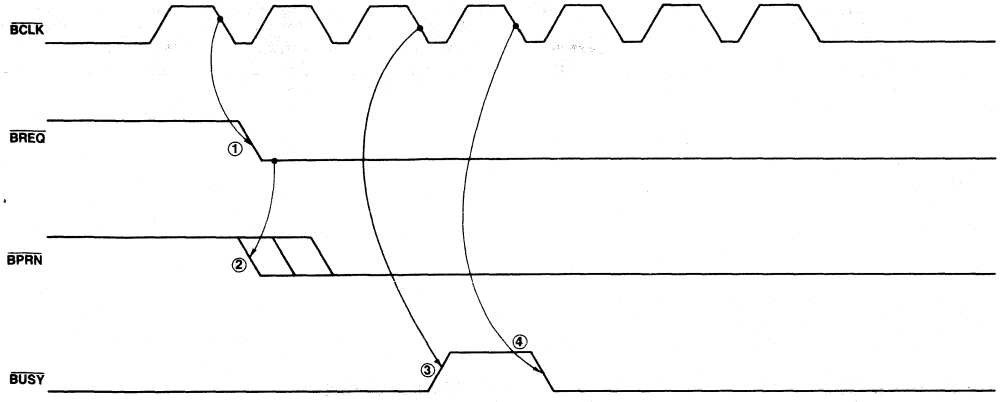
Parallel Priority Resolving

This technique uses a Bus Request line ($\overline{BREQ}$) for each arbiter on the multimaster system bus. Each $\overline{BREQ}$ line goes to a priority encoder that generates the address of the highest priority active $\overline{BREQ}$ line. This binary address is decoded to select the Bus Priority In line ($\overline{BPRN}$) that is returned to the highest priority active arbiter. The arbiter that receives priority ($\overline{BPRN}$ true) allows its bus master onto the multimaster system bus as soon as the bus becomes available. An arbiter that gets priority over another arbiter cannot immediately seize the bus, but must wait until the current bus transaction is complete. When the transaction is complete, the current occupant of the bus surrenders the bus by releasing $\overline{BUSY}$. $\overline{BUSY}$ is an active low OR tied line which goes to every arbiter on the system bus. When $\overline{BUSY}$ goes high (inactive), the priority arbiter seizes the bus and brings $\overline{BUSY}$ low to keep other arbiters off the bus. Note that all multimaster system bus transactions are synchronized to the bus clock ($\overline{BCLK}$).

Parallel Priority Resolving



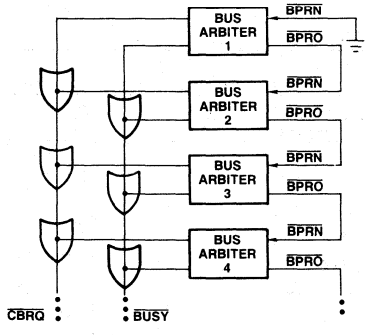
Higher Priority Arbiter Obtaining the Bus from a Lower Priority Arbiter



Notes:
① Higher priority arbiter requests the system bus.
② Attains priority.
③ Lower priority arbiter releases BUSY.
④ Higher priority arbiter then acquires the bus and pulls BUSY low.

Serial Priority Resolving

The serial priority resolving technique daisy-chains the bus arbiters together by connecting the higher priority arbiter's BPRO output to the BPRN of the next lowest priority arbiter. This eliminates the need for the priority encoder-decoder arrangement. The number of arbiters that may be daisy-chained together is a function of BCLK and the propagation delay from arbiter to arbiter. At 10 MHz, only 3 arbiters may be daisy-chained.



Rotating Priority Resolving

This technique resembles the parallel priority resolving technique except that priority is dynamically reassigned. The priority encoder is replaced by a circuit that rotates priority between arbiters to allow each arbiter an equal chance to use the system bus.

Modes of Operation

The μPB8289 has two basic operating modes: I/O Peripheral Bus mode (IOB mode), and Resident Bus mode (RESB mode). The IOB strapping option configures the μPB8289 into IOB mode and the RESB strapping option configures it to RESB mode. If both options are strapped false, the arbiter interfaces the processor to a multimaster system bus only. If both options are strapped true, the arbiter interfaces the processor to a multimaster system bus, a resident bus, and an I/O bus.

IOB Mode

IOB mode allows the processor to access both an I/O peripheral bus and a multimaster system bus. On an I/O peripheral bus, all devices on the bus, including memory, are treated as I/O devices and addressed by I/O commands. All memory commands are directed to the multimaster system bus. In IOB mode, the processor communicates with and controls peripherals over the peripheral bus and communicates with system memory over the system memory bus.

RESB Mode

RESB mode allows the processor to communicate over both a resident bus and a multimaster system bus. A resident bus can issue memory and I/O commands, but it is separate from the multimaster system bus. The resident bus has one master and is dedicated to only that master. The 8086 and 8088 can communicate with a resident bus and a multimaster system bus. The processor can access the memory and peripherals of both buses. Memory mapping selects which bus is accessed. The SYSB/RESB input on the arbiter instructs the arbiter on which bus to access. The signal connected to SYSB/RESB also enables and disables commands from one of the bus controllers.

Mode Summary

	Status Lines From 8086 or 8088 or 8089			IOB Mode Only	RESB (Mode) Only IOB = High RESB = High		IOB Mode RESB Mode IOB = Low RESB = High		Single Bus Mode IOB = High RESB = Low
	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	IOB = Low	SYSB/RESB = High	SYSB/RESB = Low	SYSB/RESB = High	SYSB/RESB = Low	
	0	0	0	x	✓	x	x	x	✓
I/O Commands	0	0	1	x	✓	x	x	x	✓
	0	1	0	x	✓	x	x	x	✓
Halt	0	1	1	x	x	x	x	x	x
	1	0	0	✓	✓	x	✓	x	✓
Memory Commands	1	0	1	✓	✓	x	✓	x	✓
	1	1	0	✓	✓	x	✓	x	✓
Idle	1	1	1	x	x	x	x	x	x

Notes:

① x = Multimaster System Bus is allowed to be surrendered.

② ✓ = Multimaster System Bus is requested.

Multimaster System Bus

Mode	Pin Strapping	Requested ①	Surrendered ②
Single Bus Multimaster Mode	$\overline{IOB}$ = High RESB = Low	When the processor's status lines go active	HLT + TI • HPBRQ†
RESB Mode Only	$\overline{IOB}$ = High RESB = High	SYSB/$\overline{RESB}$ = High 2 Active	(SYSB/$\overline{RESB}$ = Low + TI) CBRQ + HLT + HPBRQ
IOB Mode Only	$\overline{IOB}$ = Low RESB = Low	Memory Commands	(I/O Status + TI) • CBRQ + HLT + HPBRQ
IOB Mode • RESB Mode	$\overline{IOB}$ = Low RESB = High	(Memory Command) • (SYSB/$\overline{RESB}$ = High)	((I/O Status Commands) + (TI) (SYSB/$\overline{RESB}$ = Low) • CBRQ + HPBRQ† + HLT)

Notes:

① Except for HALT and Idle status.

② $\overline{LOCK}$ prevents surrender of bus to any other arbiter. $\overline{CRQLCK}$ prevents surrender of bus to a lower priority arbiter.

③ HLT = processor halt; $\overline{S_2}$–$\overline{S_0}$ = 011.

④ TI = processor idle; $\overline{S_2}$–$\overline{S_0}$ = 111.

⑤ + means OR.

⑥ • means AND.

† HPBRQ = higher priority bus request or $\overline{BPRN}$ = 1.

Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V
All Input Voltages	−1.0V to +5.5V
Power Dissipation	1.5W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

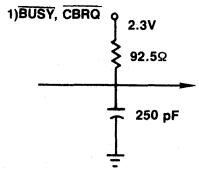
DC Characteristics

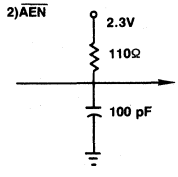
T_a = 0°C to +70°C; V_{CC} = 5V ±10%

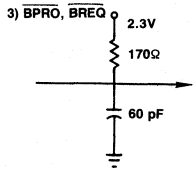
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input Clamp Voltage	V_C			−1.0	V	V_{CC} = 4.50V, I_C = −5 mA
Input Forward Current	I_F			−0.5	mA	V_{CC} = 5.50V, V_F = 0.45V
Reverse Input Leakage Current	I_R			60	μA	V_{CC} = 5.50V V_R = 5.50V
Output Low Voltage	V_{OL}					
$\overline{BUSY}$, $\overline{CBRQ}$				0.45	V	I_{OL} = 20 mA
$\overline{AEN}$				0.45	V	I_{OL} = 16 mA
$\overline{BPRO}$, $\overline{BREQ}$				0.45	V	I_{OL} = 10 mA
Output High Voltage	V_{OH}					
$\overline{BUSY}$, $\overline{CBRQ}$			Open Collector			
All Other Outputs		2.4			V	I_{OH} = 400 μA
Power Supply Current	I_{CC}			165	mA	

Capacitance

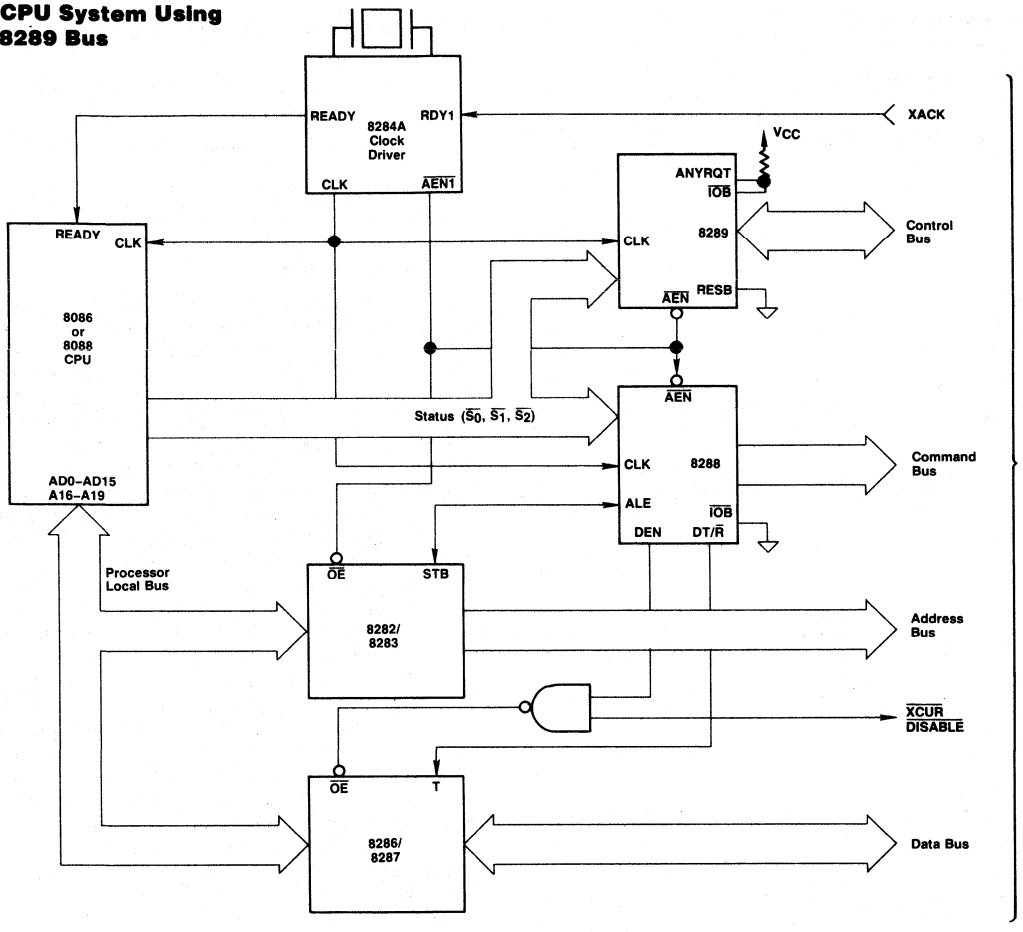
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin Status			25	pF	
Input Capacitance	Cin (Others)			12	pF	







Typical CPU System Using the μPB8289 Bus Arbiter



9

AC Characteristics
Timing Requirements

T_a = 0°C to +70°C; V_{CC} = 5V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK Cycle Period	t_{CLCL}	125			ns	
CLK Low Time	t_{CLCH}	65			ns	
CLK High Time	t_{CHCL}	35			ns	
Status Active Setup	t_{SVCH}	65		t_{CLCL}-10	ns	
Status Inactive Setup	t_{SHCL}	50		t_{CLCL}-10	ns	
Status Active Hold	t_{HVCH}	10			ns	
Status Inactive Hold	t_{HVCL}	10			ns	
$\overline{BUSY}$↑↓ Setup to $\overline{BCLK}$↓	t_{BYSBL}	20			ns	
$\overline{CBRQ}$↑↓ Setup to $\overline{BCLK}$↓	t_{CBSBL}	20			ns	
$\overline{BCLK}$ Cycle Time	t_{BLBL}	100			ns	
$\overline{BCLK}$ High Time	t_{BHCL}	30		0.65 (t_{BLBL})	ns	
$\overline{LOCK}$ Inactive Hold	t_{CLLL1}	10			ns	
$\overline{LOCK}$ Active Setup	t_{CLLL2}	40			ns	
$\overline{BPRN}$↓↑ to $\overline{BCLK}$ Setup Time	t_{PNBL}	15			ns	
SYSB/$\overline{RESB}$ Setup	t_{CLSR1}	0			ns	
SYSB/$\overline{RESB}$ Hold	t_{CLSR2}	20			ns	
Initialization Pulse Width	t_{IVIH}	3 t_{BLBL} + 3 t_{CLCL}			ns	
Input Rise Time	t_{ILIH}			20	ns	From 0.8V to 2.0V
Input Fall Time	t_{IHIL}			12	ns	From 2.0V to 0.8V

Timing Responses

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{BCLK}$ to $\overline{BREQ}$ Delay ①	t_{BLBRL}			35	ns	
$\overline{BCLK}$ to $\overline{BPRO}$ ①②	t_{BLPOH}			40	ns	
$\overline{BPRN}$↓↑ to $\overline{BPRO}$↓↑ Delay ①②	t_{PNPO}			25	ns	
$\overline{BCLK}$ to $\overline{BUSY}$ Low	t_{BLBYL}			60	ns	
$\overline{BCLK}$ to $\overline{BUSY}$ Float ③	t_{BLBYH}			35	ns	
CLK to $\overline{AEN}$ High	t_{CLAEH}			65	ns	
$\overline{BCLK}$ to $\overline{AEN}$ Low	t_{BLAEL}			40	ns	
$\overline{BCLK}$ to $\overline{CBRQ}$ Low	t_{BLCBL}			60	ns	
$\overline{BCLK}$ to $\overline{CBRQ}$ Float ③	t_{RLCRH}			35	ns	
Output Rise Time	t_{OLOH}			20	ns	From 0.8V to 2.0V
Output Fall Time	t_{OHOL}			12	ns	From 2.0V to 0.8V

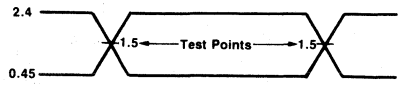
Notes:

① Denotes that the spec applies to both transitions of the signal.

② $\overline{BCLK}$ generates the first $\overline{BPRO}$. Subsequent changes of $\overline{BPRO}$ are generated through BPRON.

③ Measured at 0.5V above GND.

AC Test Condition Waveform

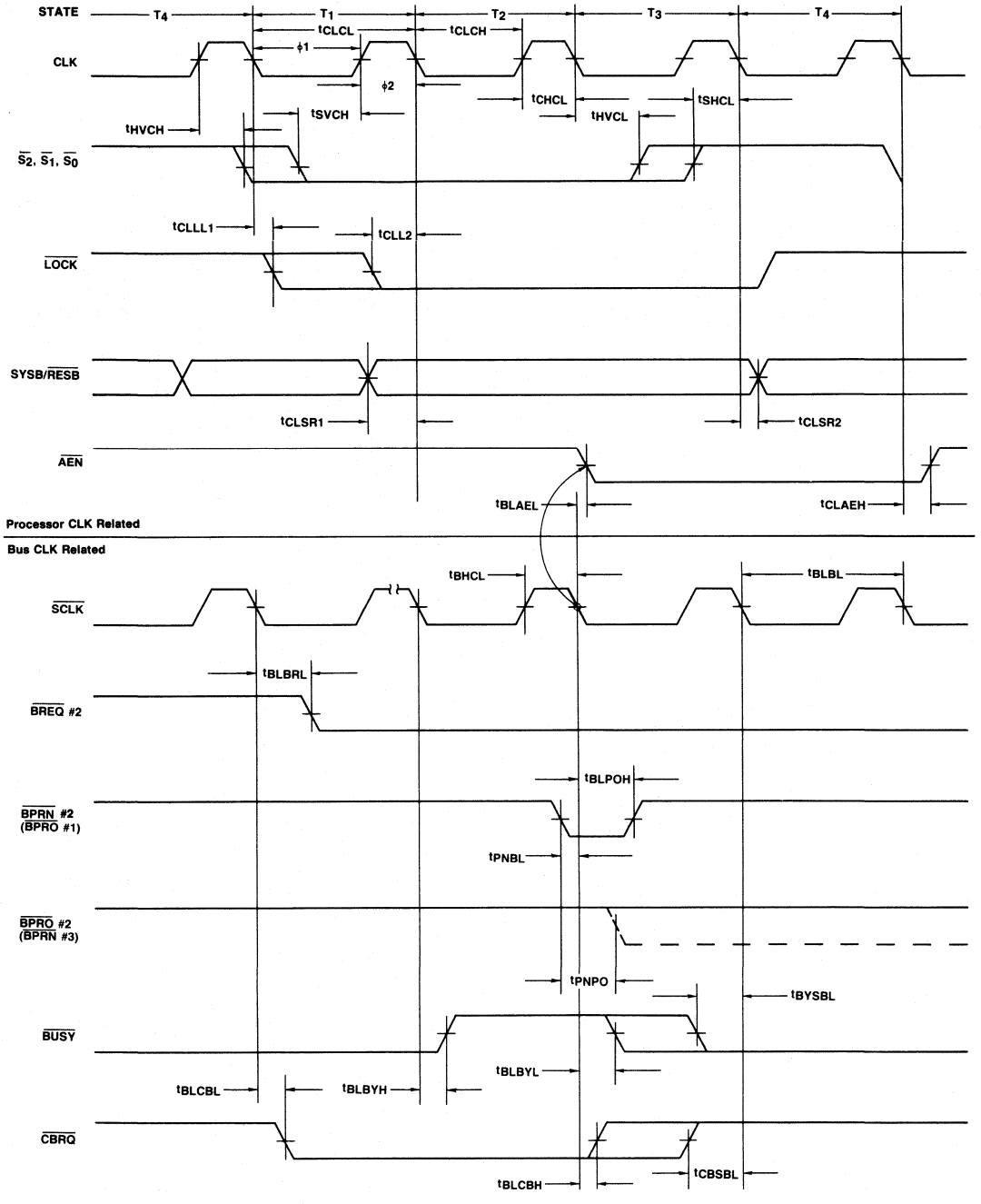


AC Testing inputs are driven at 2.4V for LOGIC 1 and 0.45V for LOGIC 0. The clock is driven at 4.3V and 0.25. Timing measurements are made at 1.5V for LOGIC 1 and 0.

Timing Waveforms

The signals related to CLK are typical processor signals and do not relate to the depicted sequence of events of the signals referenced to $\overline{BCLK}$. The signals shown related to the $\overline{BCLK}$ represent a hypothetical sequence of events for illustration. Assume three bus arbiters of priorities 1, 2, and 3 configured in the serial priority resolving scheme. Assume arbiter 1 has the bus and is holding $\overline{BUSY}$ low. Arbiter 2 detects its processor wants the bus and pulls $\overline{BREQ}$ #2 low. If $\overline{BPRN}$ #2 is high (as shown), arbiter 2 pulls $\overline{CBRQ}$ low. $\overline{CBRQ}$ signals to higher priority arbiter 1 that a lower priority arbiter wants the bus. A higher priority arbiter would be given $\overline{BPRN}$ when it makes the bus request rather than having to wait for another arbiter to release the bus through $\overline{CBRQ}$. Arbiter 1 relinquishes the multimaster system bus when it enters a state of not requiring it, by lowering its $\overline{BPRO}$ #1 (tied to $\overline{BPRN}$ #2) and releasing $\overline{BUSY}$. Arbiter 2 now sees that it has priority from $\overline{BPRN}$ #2 being low and releases $\overline{CBRQ}$. As soon as $\overline{BUSY}$ signifies the bus is available (high), arbiter 2 pulls $\overline{BUSY}$ low on the next falling edge of $\overline{BCLK}$. Note that if arbiter 2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority by lowering its $\overline{BPRO}$ #2 (TPNPO). Note also that even a higher priority aribiter which is acquiring the bus through $\overline{BPRN}$ will momentarily drop $\overline{CBRQ}$ until it has acquired the bus.

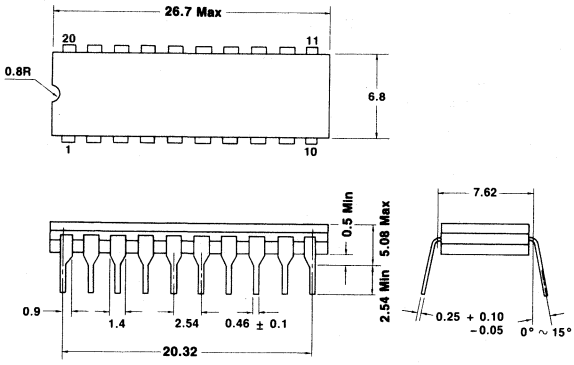
Timing Waveforms



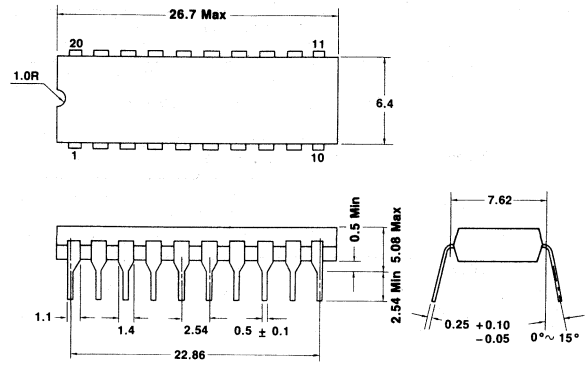
Package Outlines

μPB8289D
Cerdip

All measurements in MM



μPB8289C
Plastic



16,384-BIT ROM WITH I/O PORTS
*16,384-BIT EPROM WITH I/O PORTS

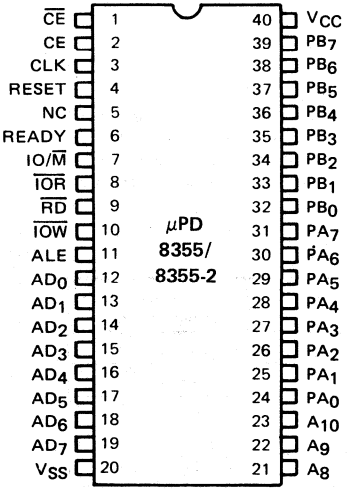
DESCRIPTION

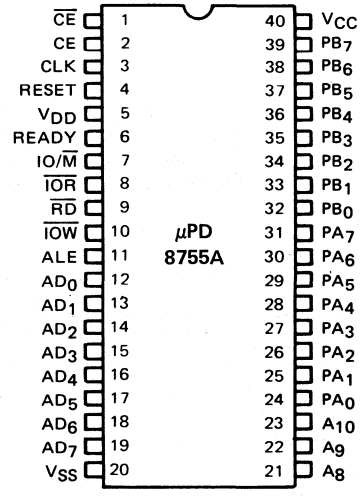
The μPD8355 and the μPD8755A are μPD8085A Family components. The μPD8355 contains 2048 x 8 bits of mask ROM and the μPD8755A contains 2048 x 8 bits of mask EPROM for program development. Both components also contain two general purpose 8-bit I/O ports. They are housed in 40 pin packages, are designed to directly interface to the μPD8085A, and are pin-for-pin compatible with each other.

FEATURES

- 2048 X 8 Bits Mask ROM (μPD8355 and μPD8355-2)
- 2048 X 8 Bits Mask EPROM (μPD8755A)
- 2 Programmable I/O Ports
- Single Power Supplies: +5V
- Directly Interfaces to the μPD8085A
- Pin for Pin Compatible
- μPD8755A: UV Erasable and Electrically Programmable
- μPD8335 and μPD8355-2 Available in Plastic Package
- μPD8755A Available in Ceramic Package

PIN CONFIGURATIONS





NC: Not Connected

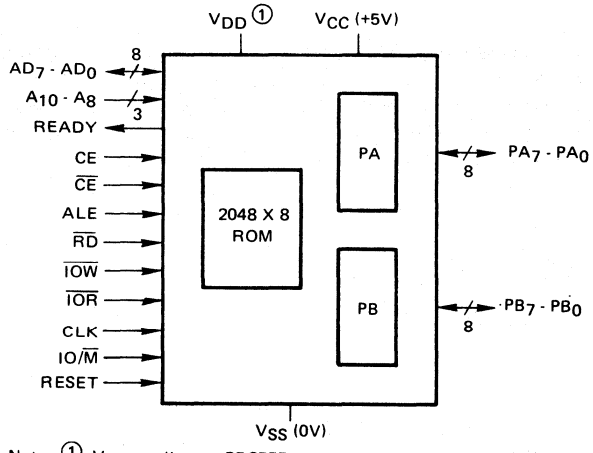
9

FUNCTIONAL DESCRIPTION

The μPD8355 and μPD8755A contain 16,384 bits of mask ROM and EPROM respectively, organized as 2048 X 8. The 2048 word memory location may be selected anywhere within the 64K memory space by using the upper 5 bits of address from the μPD8085A as a chip select.

The two general purpose I/O ports may be programmed input or output at any time. Upon power up, they will be reset to the input mode.

BLOCK DIAGRAM



Note: ① V_{DD} applies to μPD8755A only.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature (μPD8355) . . . . . 0°C to +70°C
(μPD8755A) . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin (μPD8355) . . . . . -0.5 to +7V ①
(μPD8755A) . . . . . -0.5 to +7V ①
Power Dissipation 1.5W

Note: ① With Respect to Ground

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	V_{CC} = 5.0V ①
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	V_{CC} = 5.0V ①
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Input Leakage	I_{IL}			10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LO}			±10	μA	0.45V ≤V_{OUT} ≤V_{CC}
V_{CC} Supply Current	I_{CC}			180	mA	

Note: ① These conditions apply to μPD8355 only.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1,2	$\overline{CE}$, CE	Chip Enables	Enable Chip activity for memory or I/O
3	CLK	Clock Input	Used to Synchronize Ready
4	Reset	Reset Input	Resets PA and PB to all inputs
5 ①	NC	Not Connected	
5 ②	V_{DD}	Programming Voltage	Used as a programming voltage, tied to +5V normally
6	Ready	Ready Output	A tri-state output which is active during data direction register loading
7	IO/$\overline{M}$	I/O or Memory Indicator	An input signal which is used to indicate I/O or memory activity
8	IOR	I/O Read	I/O Read Strobe In
9	$\overline{RD}$	Memory Read	Memory Read Strobe In
10	$\overline{IOW}$	I/O Write	I/O Write Strobe In
11	ALE	Address Low Enable	Indicates information on Address/Data lines is valid
12-19	AD_0-AD_7	Low Address/Data Bus	Multiplexed Low Address and Data Bus
20	V_{SS}	Ground	Ground Reference
21-23	A_8-A_{10}	High Address	High Address inputs for ROM reading
24-31	PA_0-PA_7	Port A	General Purpose I/O Port
32-39	PB_0-PB_7	Port B	General Purpose I/O Port
40	V_{CC}	5V Input	Power Supply

Notes: ① μPD8355
② μPD8755A

I/O PORTS

I/O port activity is controlled by performing I/O reads and writes to selected I/O port numbers. Any activity to and from the μPD8355 requires the chip enables to be active. This can be accomplished with no external decoding for multiple devices by utilizing the upper address lines for chip selects. ① Port activity is controlled by the following I/O addresses:

AD_1	AD_0	PORT SELECTED	FUNCTION
0	0	A	Read or Write PA
0	1	B	Read or Write PB
1	0	A	Write PA Data Direction
1	1	B	Write PB Data Direction

Since the data direction registers for PA and PB are each 8-bits, any pin on PA or PB may be programmed as input or output (0 = in, 1 = out).

Note: ① During ALE time the data/address lines are duplicated on A_{15}-A_8.

9

AC CHARACTERISTICS

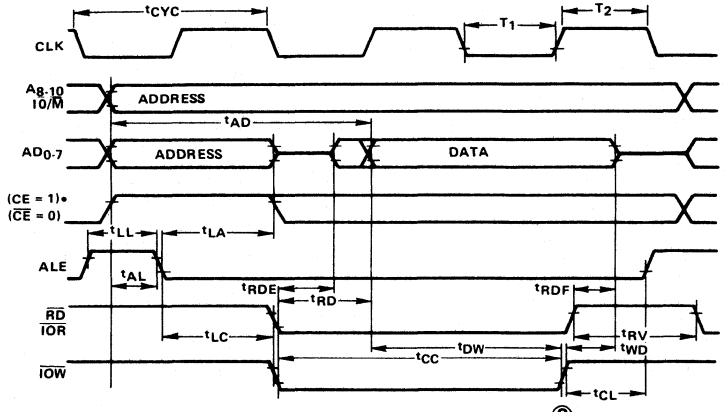
T_a = 0°C to 70°C; V_{CC} = 5V ± 5%

Symbol	Parameter	8355 Min.	8355 Max.	8355-2 Min.	8355-2 Max.	Unit	Test Conditions
t_{CYC}	Clock Cycle Time	320		200		ns	
T_1	CLK Pulse Width	80		40		ns	C_{LOAD} = 150 pF
T_2	CLK Pulse Width	120		70		ns	
t_f, t_r	CLK Rise and Fall Time		30		30	ns	
t_{AL}	Address to Latch Set Up Time	50		30		ns	
t_{LA}	Address Hold Time after Latch	80		30		ns	
t_{LC}	Latch to READ/WRITE Control	100		40		ns	
t_{RD}	Valid Data Out Dealy from READ Control		170		140	ns	
t_{AD}	Address Stable to Data Out Valid		400		330	ns	
t_{LL}	Latch Enable Width	100		70		ns	
t_{RDF}	Data Bus Float after READ	0	100	0	85	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns	150 pF Load
t_{CC}	READ/WRITE Control Width	250		200		ns	
t_{DW}	Data in to Write Set Up Time	150		150		ns	
t_{WD}	Data in Hold Time After WRITE	10		10		ns	
t_{WP}	WRITE to Port Output		400		400	ns	
t_{PR}	Port Input Set Up Time	50		50		ns	
t_{RP}	Port Input Hold Time	50		50		ns	
t_{RYH}	READY HOLD Time	0	160	0	160	ns	
t_{ARY}	ADDRESS (CE) to READY		160		160	ns	
t_{RV}	Recovery Time Between Controls	300		200		ns	
t_{RDE}	READ Control to Data Bus Enable	10		10		ns	

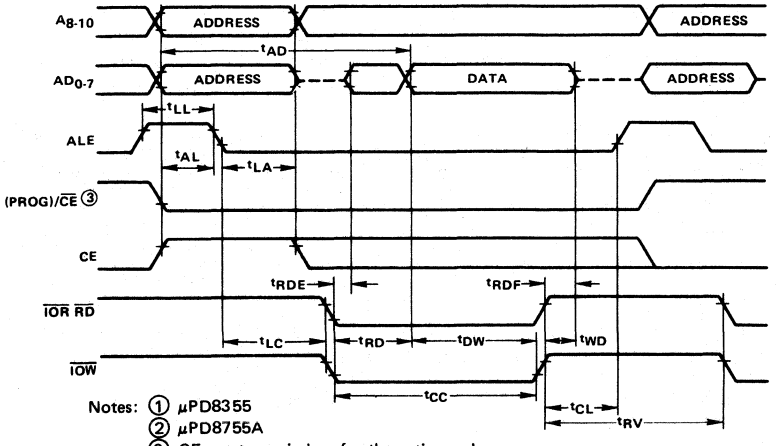
Notes: 30 ns for μPD8755A
C_{LOAD} = 150 pF

TIMING WAVEFORMS

ROM READ, I/O READ AND WRITE ①



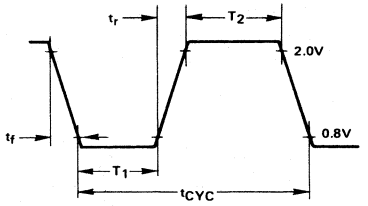
PROM READ, I/O READ AND WRITE ②



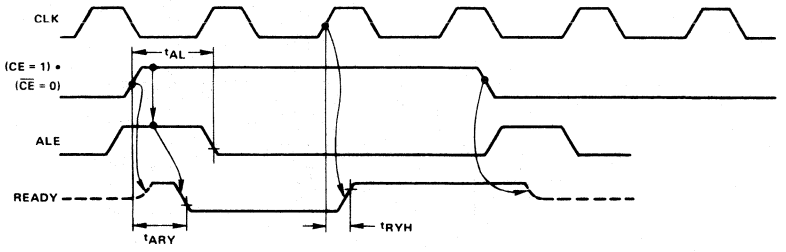
Notes: ① μPD8355
② μPD8755A
③ CE must remain low for the entire cycle

TIMING WAVEFORMS (CONT.)

CLOCK

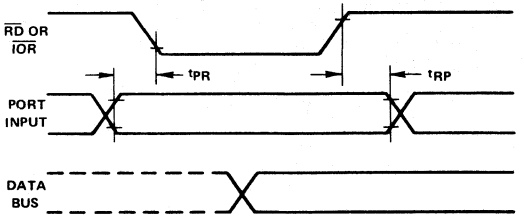


WAIT STATE TIMING (READY = 0)

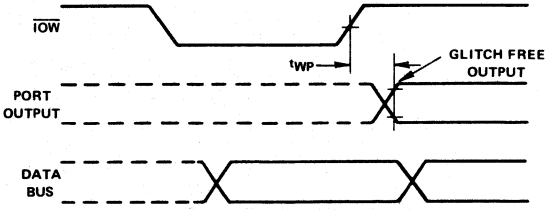


I/O PORT

INPUT MODE:



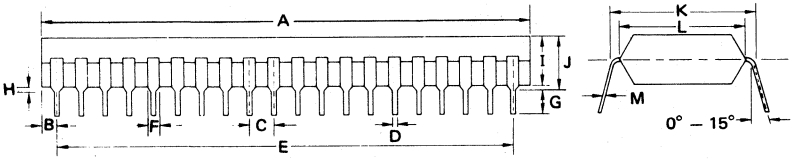
OUTPUT MODE:



EPROM PROGRAMMING μPD8755A

Erasure of the μPD8755A occurs when exposed to ultraviolet light sources of wavelengths less than 4000 Å. It is recommended, if the device is exposed to room fluorescent lighting or direct sunlight, that opaque labels be placed over the window to prevent exposure. To erase, expose the device to ultraviolet light at 2537 Å at a minimum of 15 W-sec/cm^2 (intensity X expose time). After erasure, all bits are in the logic 1 state. Logic 0's must be selectively programmed into the desired locations. It is recommended that NEC's PROM programmer be used for this application.

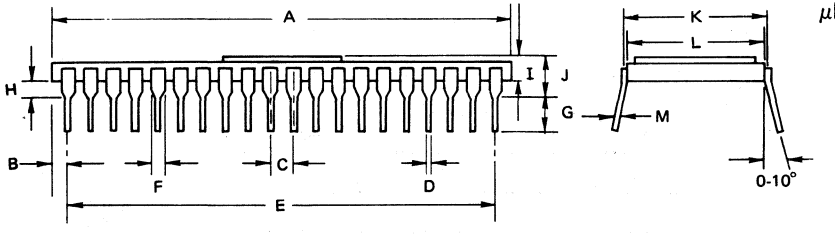
PACKAGE OUTLINES
μPD8355C



PLASTIC

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

μPD8755AD



CERAMIC

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

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